STACKED TECHNOLOGIES INC

ST9D232M64SBG5
ST9D232M72SBG5
ST9D232M80SBG5
ST9D264M64SBG5
ST9D264M72SBG5
ST9D264M80SBG5

2 - 5.0 Gb, DDR2, 32M/64M x 64/72/80 Integrated Memory Module (HiMOD)

FAST, LOW POWER, HIGH DENSITY, WIDE WORD MEMORY

FEATURES

- DDR2 25mm2 Module [HiMOD]:
  - 32M-64M words
  - x64, x72, x80 word widths
- High performance:
  - 400, 533, 667, 800 Mbps
  - TEMPERATURE:
    - C (0°C to 70°C)
    - I (-40°C to 85°C)
    - E (-40°C to 105°C)
    - M(-55°C to 125°C)
- Low power:
  - 1.8V supply
  - 2.4 Watts max
- Space saving footprint
  - 25mm x 25mm, 16 x 16 matrix w/ 255 balls, 1.27mm pitch
  - 1.7mm low profile height
- Thermally enhanced, Impedance matched, integrated packaging
- Differential data strobe
- 4n-bit prefetch architecture
- 4 (32Gb) & 8 (64Gb) internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals.
- Programmable CAS latency (CL): 3, 4, 5 and 6
- Fixed burst length (BL) of 8 and burst chop (BC) of 4
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self/Auto Refresh modes
  - 64ms 8192 - cycle refresh
- Output Driver Calibration
- Adjustable drive strength

Benefits

- Reduced I/O (46%)
- Reduced trace lengths due to the highly integrated, impedance matched packaging
- Thermally enhanced packaging technology allow silicon integration without performance degradation due to power dissipation (heat)
- High TCE organic laminate interposer for improved glass stability over a wide operating temperature
- Suitability of use in High Reliability applications requiring Mil-temp, non-hermetic device operation
- RoHS - compliant

*Note: This product and/or its specifications are subject to change without notice. Latest document should be retrieved from STACKED prior to your design consideration.

L9D2xxMxxSBG5 Product Offerings:

Part Number:	Density:	Depth:	Word Widths:
ST9D232M64SBG5	2.0Gb	32M	x 64
ST9D232M72SBG5	2.2Gb	32M	x 72
ST9D232M80SBG5	2.5Gb	32M	x 80
ST9D264M64SBG5	4.0Gb	64M	x 64
ST9D264M72SBG5	4.5Gb	64M	x 72
ST9D264M80SBG5	5.0Gb	64M	x 80

L9D2xxMxxSBG5 Available Timings:

	Clock:	Cycle Time:	Data Rate:
DDR2-800	400MHz	2.5ns	800Mbs
DDR2-667	333MHz	3.0ns	667Mbs
DDR2-533	267MHz	3.75ns	533Mbs
DDR2-400	200MHz	5.0ns	400Mbs

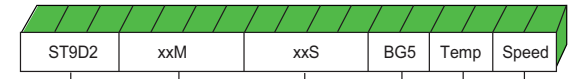
HiMOD

integrated module products

FEATURES

Figure 3 - DDR2 Part Numbers

Sample Part Number: ST9D2xxMxxSBG5



STACKED DDR2 Integrated Module

Word = 32M 64M

Wordwidth = x64 x72 x80

S= Single Channel

25 x 25 x 1.7mm 255 Ball Array

CLK	Core Frequency MHz	Data Rate Mbs
50	200	400
38	267	533
3	333	667
25	400	800

Temperature	Code
Commercial (0°C to 70°C)	C
Industrial (-40°C to 85°C)	I
Extended (-40°C to 105°C)	E
Military (-55°C to 125°C)	M

Note: Not all options can be combined. Please see our Part Catalog for available offerings.

FEATURES

Table 2: Addressing

LDI iMOD Addressing	
Configuration	[8 Meg x 4(8) banks x 16] x 4(5) iMOD
Refresh Count	8K
ROW Addressing	8K (A[12:0])
Back Addressing	4 (BA[1:0]) 8 (BA[2:0])
Column Addressing	1K (A[9:0])

Table 3: Key Parameters

LDI Part Number	Speed Grade	$^{t}CK_{AVG}$	Data Rate [Mbps]			
			CL=3	CL=4	CL=5	CL=6
ST9D2xxMxxSBG5[C, I, E, M]25	25	2.5ns	400	533	667	800
ST9D2xxMxxSBG5[C, I, E, M]3	3	3.0ns	400	533	667	
ST9D2xxMxxSBG5[C, I, E, M]38	38	3.75ns	400	533		
ST9D2xxMxxSBG5[C, I, E, M]50	50	5.0ns	400			

C = ***Commercial***: Commercial class integrated component, fully across 0°C to +70°C

I = ***Industrial***: Industrial class integrated component, fully across -40°C to +85°C

E = ***Extended***: Extended class integrated component, operable across -40°C to +105°C

M = ***Mil-Temp***: Mil-Temperature only class integrated component, operable across -55°C to +125°C

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BALL /SIGNAL LOCATION DIAGRAM:

FIGURE 1A - 32M X 64 PINOUT TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	VSS	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	DM0	VDD	DM1	DQS7	DQS0	DQS1	BA0	BA1	DQS2	DQS3	Vref	DM2	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	DQS6	DQS7\	DQS0\	DQS1\	DNU	DQS3\	DQS2\	RAS1\	WE1\	VSS	DM3	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	DQS6\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	RFU	RFU	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	RFU	NC	NC	DQS4\	DQS5\	DQS4	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	DM7	VDD	WE3\	DM6	RFU	VDD	RFU	RFU	RFU	RFU	NC	DM5	VSS	DM4	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	RFU	RFU	RFU	RFU	RFU	RFU	RFU	DQS5	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	RFU	RFU	RFU	RFU	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	RFU	RFU	RFU	RFU	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	RFU	RFU	RFU	RFU	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core)	V+ (Core Power)	UNPOPULATED	Address	CNTRL
GND (I/O)	V+ (I/O Power)	NC	DNU	RFU
VSSDL	VDDL	DATA (I/O)	REF Level	

NOTE: Connect N5 to VDD through 1K resistor; Connect K6 to GND through 1K resistor

BALL /SIGNAL LOCATION DIAGRAM:

FIGURE 1B - 32M X 72 PINOUT TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	VSS	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	DM0	VDD	DM1	DQS7	DQS0	DQS1	BA0	BA1	DQS2	DQS3	Vref	DM2	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	DQS6	DQS7\	DQS0\	DQS1\	DNU	DQS3\	DQS2\	RAS1\	WE1\	VSS	DM3	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	DQS6\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	DQS8	RFU	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	DQS8\	NC	NC	DQS4\	DQS5\	DQS4	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	DM7	VDD	WE3\	DM6	CKE4	NC	CLK4	CAS4\	WE4\	RAS4\	CS4\	DM5	VSS	DM4	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	RFU	CLK4\	RFU	RFU	DQ71	DQ70	DM8	DQS5	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	RFU	RFU	DQ69	DQ68	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	RFU	RFU	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	RFU	RFU	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core) | V+ (Core Power) | UNPOPULATED | Address | CNTRL

GND (I/O) | V+ (I/O Power) | NC | DNU | RFU

VSSDL | VDDL | DATA (I/O) | REF Level

NOTE: Connect N5 to VDD through 1K resistor; Connect K6 to GND through 1K resistor

BALL /SIGNAL LOCATION DIAGRAM:

FIGURE 1C - 32M X 80 PINOUT TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ1	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	VSS	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	DM0	VDD	DM1	DQS9	DQS0	DQS1	BA0	BA1	DQS2	DQS3	Vref	DM2	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	DQS8	DQS9\	DQS0\	DQS1\	DNU	DQS3\	DQS2\	RAS1\	WE1\	VSS	DM3	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	DQS8\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	DQS6	DQS7\	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	DQS6\	NC	NC	DQS4\	DQS5\	DQS4	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	DM7	VDD	WE3\	DM6	CKE4	DM9	CLK4	CAS4\	WE4\	RAS4\	CS4\	DM5	VSS	DM4	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	DQS7	CLK4\	DQ73	DQ72	DQ71	DQ70	DM8	DQS5	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	DQ75	DQ74	DQ69	DQ68	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	DQ77	DQ76	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	DQ79	DQ78	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core) | V+ (Core Power) | UNPOPULATED | Address | CNTRL

GND (I/O) | V+ (I/O Power) | NC | DNU

VSSDL | VDDL | DATA (I/O) | REF Level

BALL /SIGNAL LOCATION DIAGRAM:

Figure 1D- 64M X 64 Pinout Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	BA2	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	LDM0	VDD	UDM0	UDQS3	LDQS0	UDQS0	BA0	BA1	LDQS1	UDQS1	Vref	LDM1	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	LDQS3	UDQS3\	LDQS0\	UDQS0\	DNU	UDQS1\	LDQS1\	RAS1\	WE1\	VSS	UDM1	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	LDQS3\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	RFU	RFU	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	RFU	NC	NC	LDQS2\	UDQS2\	LDQS2	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	UDM3	VDD	WE3\	LDM3	RFU	VDD	RFU	RFU	RFU	RFU	NC	UDM2	VSS	LDM2	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	RFU	RFU	RFU	RFU	RFU	RFU	RFU	UDQS2	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	RFU	RFU	RFU	RFU	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	RFU	RFU	RFU	RFU	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	RFU	RFU	RFU	RFU	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core)	V+ (Core Power)	UNPOPULATED	Address	CNTRL
GND (I/O)	V+ (I/O Power)	NC	DNU	RFU
VSSDL	VDDL	DATA (I/O)	REF Level	

NOTE: Connect N5 to VDD through 1K resistor; Connect K6 to GND through 1K resistor

BALL /SIGNAL LOCATION DIAGRAM:

Figure 1E- 64M X 72 Pinout Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	BA2	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	LDM0	VDD	UDM0	UDQS3	LDQS0	UDQS0	BA0	BA1	LDQS1	UDQS1	Vref	LDM1	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	LDQS3	UDQS3\	LDQS0\	UDQS0\	DNU	UDQS1\	LDQS1\	RAS1\	WE1\	VSS	UDM1	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	LDQS3\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	LDQS4	RFU	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	LDQS4\	NC	NC	LDQS2\	UDQS2\	LDQS2	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	UDM3	VDD	WE3\	LDM3	CKE4	VDD	CLK4	CAS4\	WE4\	RAS4\	CS4\	UDM2	VSS	LDM2	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	RFU	CLK4\	RFU	RFU	DQ71	DQ70	LDM4	UDQS2	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	RFU	RFU	DQ69	DQ68	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	RFU	RFU	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	RFU	RFU	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core)	V+ (Core Power)	UNPOPULATED	Address	CNTRL
GND (I/O)	V+ (I/O Power)	NC	DNU	RFU
VSSDL	VDDL	DATA (I/O)	REF Level	

NOTE: Connect N5 to VDD through 1K resistor; Connect K6 to GND through 1K resistor

BALL /SIGNAL LOCATION DIAGRAM:

FIGURE 1F- SDRAM : DDR2 PINOUT TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A		DQ0	DQ14	DQ15	VSS	VSS	A9	A10	A11	A8	VDDQ	VDDQ	DQ16	DQ17	DQ31	VSS	A
B	DQ1	DQ2	DQ12	DQ13	VSS	VSS	A0	A7	A6	A1	VDD	VDD	DQ18	DQ19	DQ29	DQ30	B
C	DQ3	DQ4	DQ10	DQ11	VDD	VDD	A2	A5	A4	A3	VSS	VSS	DQ20	DQ21	DQ27	DQ28	C
D	DQ6	DQ5	DQ8	DQ9	VDDQ	VDDQ	A12	NC	BA2	NC	VSS	VSS	DQ22	DQ23	DQ26	DQ25	D
E	DQ7	LDM0	VDD	UDM0	UDQS3	LDQS0	UDQS0	BA0	BA1	LDQS1	UDQS1	Vref	LDM1	VSS	NC	DQ24	E
F	CAS0\	WE0\	VDD	CLK0	LDQS3	UDQS3\	LDQS0\	UDQS0\	DNU	UDQS1\	LDQS1\	RAS1\	WE1\	VSS	UDM1	CLK1	F
G	CS0\	RAS0\	VDD	CKE0	CLK0\	LDQS3\	VSSQ	VSSQ	VSSQ	VSSQ	NC	CAS1\	CS1\	VSS	CLK1\	CKE1	G
H	VSS	VSS	VDD	VDDQ	VSSDL	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDDL	VSS	VSS	VDDQ	VDD	H
J	VSS	VSS	VDD	VDDQ	VSS	NC	VSSQ	VSSQ	VSSQ	VSSQ	NC	VDD	VSS	VSS	VDDQ	VDD	J
K	CLK3\	CKE3	VDD	CS3\	LDQS4	UDQS4\	VSSQ	VSSQ	VSSQ	VSSQ	DNU	CLK2\	CKE2	VSS	RAS2\	CS2\	K
L	NC	CLK3	VDD	CAS3\	RAS3\	ODT	LDQS4\	NC	NC	LDQS2\	UDQS2\	LDQS2	CLK2	VSS	WE2\	CAS2\	L
M	DQ56	UDM3	VDD	WE3\	LDM3	CKE4	UDM4	CLK4	CAS4\	WE4\	RAS4\	CS4\	UDM2	VSS	LDM2	DQ39	M
N	DQ57	DQ58	DQ55	DQ54	UDQS4	CLK4\	DQ73	DQ72	DQ71	DQ70	LDM4	UDQS2	DQ41	DQ40	DQ37	DQ38	N
P	DQ60	DQ59	DQ53	DQ52	VSS	VSS	DQ75	DQ74	DQ69	DQ68	VDD	VDD	DQ43	DQ42	DQ36	DQ35	P
R	DQ62	DQ61	DQ51	DQ50	VDD	VDD	DQ77	DQ76	DQ67	DQ66	VSS	VSS	DQ45	DQ44	DQ34	DQ33	R
T	VSS	DQ63	DQ49	DQ48	VDDQ	VDDQ	DQ79	DQ78	DQ65	DQ64	VSS	VSS	DQ47	DQ46	DQ32	VDD	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

GND (Core)	V+ (Core Power)	UNPOPULATED	Address	CNTRL
GND (I/O)	V+ (I/O Power)	NC	DNU	
VSSDL	VDDL	DATA (I/O)	REF Level	

Table 1: Pin/Ball Locations and Descriptions

Ball Assignments	Symbol	Type	Description
L6	ODT	CNTL Input	On-Die Termination: Registered High enables on data bus termination
F4, G5, F16, G15 L13, K12, L2, K1 M8, N6	CLK0, CLK0\, CLK1, CK1\ CLK2, CLK2\, CLK3, CLK3\ CLK4, CLK4\	CNTL Input	Differential input clocks, one set for each x16bits
G4, G16, K13 K2, M6	CKE0, CKE1, CKE2 CKE3, CKE4	CNTL Input	Clock enable which activates all on silicon clocking circuit
G1, G13, K16 K4, M12	CS0\, CS1\, CS2\ CS3\,CS4\	CNTL Input	Chip Selects, one for each 16 bits of the data bus width
G2, F12, K15 L5, M11	RAS0\, RAS1\, RAS2\ RAS3\, RAS4\	CNTL Input	Command input which along with CAS\, WE\ and CS\ define operations
F1, G12, L16 L4, M9	CAS0\, CAS1\, CAS2\ CAS3\, CAS4\	CNTL Input	Command input which along with RAS\, WE\ and CS\ define operations
F2, F13, L15 M4, M10	WE0\, WE1\, WE2\ WE3\, WE4\	CNTL Input	Command input which along with RAS\, CAS\ and CS\ define operations
E2, E4, E13, F15,M15, M13, M5, M2, N11 M7	DM0, DM1, DM2, DM3, DM4, DM5 DM6, DM7, DM8 DM9	CNTL Input	One Data Mask for each 8 bits of word
E6, E7, E10, E11, L12, N12, F5, E5, K5, N5	DQS0, DQS1 DQS2, DQS3 DQS4, DQS5, DQS6, DQS7 DQS8, DQS9	CNTL Input	Data Strobe input for each 8 bit byte of word Differential input of DQSx, only used when Differential DQS mode is enabled
F7, F8, F11, F10, L10, L11, G6, F6, L7, K6	DQS0\, DQS1\ DQS2\, DQS3\ DQS4\, DQS5\ DQS6\, DQS7\ DQS8\, DQS9\	CNTL Input CNTL Input	Data Strobe input for lower byte of each x16 word Differential input of DQSx\, only used when Differential DQS mode is enabled
B8, B10, C8, C10 C9, C8, B9, B8 A10, A7, A8, A9, D7	A0, A1, A2, A3 A4, A5, A6, A7 A8, A9, A10, A11, A12	Input	Array Address inputs providing ROW addresses for Active commands, and the column address and auto precharge bit (A10) for READ/WRITE commands
D8, D9, D10	RFU	Future Input	Future Address/Bank Address inputs
E8, E9, [D9]	BA0, BA1, [BA2]	Input	Bank Address inputs. BA2 on 4, 4.5, 5Gb only
E12	Vref	Supply	SSTL_1.8 Voltage Reference
B11,B12,C5,C6,E3,F3, G3,H3,H16,J3,J12, J16,K3,L3,M3,P11,P12, R5,R6,T16	VDD	Supply	Power Supply
A11,A12,D5,D6,H4,H15, J4, J15, T5, T6	VDDQ	Supply	I/O Power Supply
A5,A6,A16,B5,B6,C11, C12,D11,D12,E14,F14,G14, H1,H2,H13,H14, J1,J2,J5,J13,J14,K14, L14,M14,P5,P6,R11	Vss	Supply	Ground return

Table 1: Pin/Ball Locations and Descriptions Continued

Ball Assignments	Symbol	Type	Description
R12,T1,T11,T12 G7,G8,G9,G10,H7,H8, H9,H10,J7,J8,J9,J10, K7,K8,K9,K10	VssQ	Supply	I/O Ground return
H5	VSSDL	Supply	DLL Power
H12	VDDL	Supply	DLL Ground
A0,B1,B2,C1	D0, D1, D2, D3	Input/Output	Data bidirectional input/Output pins
C2,D2,D1,E7	D4, D5, D6, D7		
D3,D4,C3,C4	D8, D9, D10, D11		
B3,B4,A3,A4	D12, D13, D14, D15		
A13,A14,B13,B14	D16, D17, D18, D19		
C13,C14,D13,D14	D20, D21, D22, D23		
E16,D16,D15,C15	D24, D25, D26, D27		
C16,B15,B16,A15	D28, D29, D30, D31		
T15,R16,R15,P16	D32, D33, D34, D35		
P15,N16,N15,M16	D36, D37, D38, D39		
N14,N13,P14,P13	D40, D41, D42, D43		
R14,R13,T14,T13	D44, D45, D46, D47		
T4,T3,R4,R3	D48, D49, D50, D51		
P4,P3,N4,N3	D52, D53, D54, D55		
M1,N1,N2,P2	D56, D57, D58, D59		
P1,R2,R1,T2	D60, D61, D62, D63		
T10,T9,R10,R9	D64, D65, D66, D67		
P10,P9,N10,N9	D68, D69, D70, D71		
N8,N7,P8,P7	D72,D73,D74,D75		
R8,R7,T8,T7	D76,D77,D78,D79		
E15,G11,H6,H11,J6, J11,L1,L8,L9	NC		No connection
F9,K11	DO NOT USE		RESERVED FOR SPECIAL CONSIDERATION PINS
A1	unpopulated		Unpopulated ball matrix location (location registration aid)

Figure 2A - 32M X 64 Functional Block Diagram

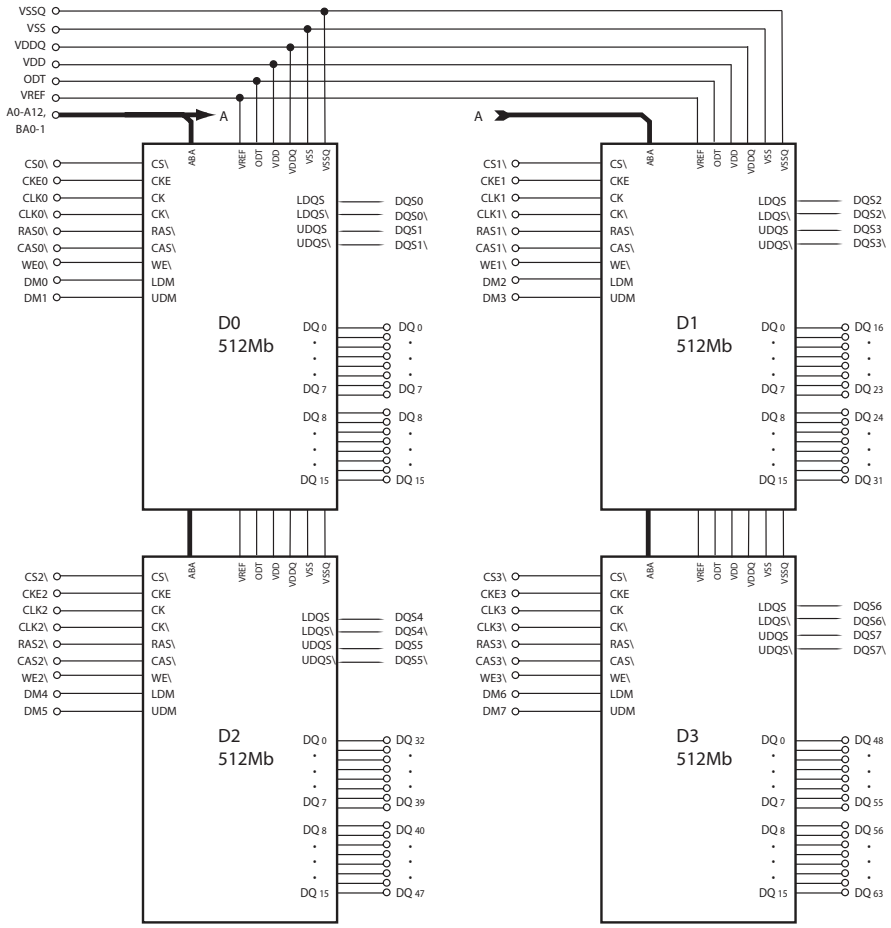
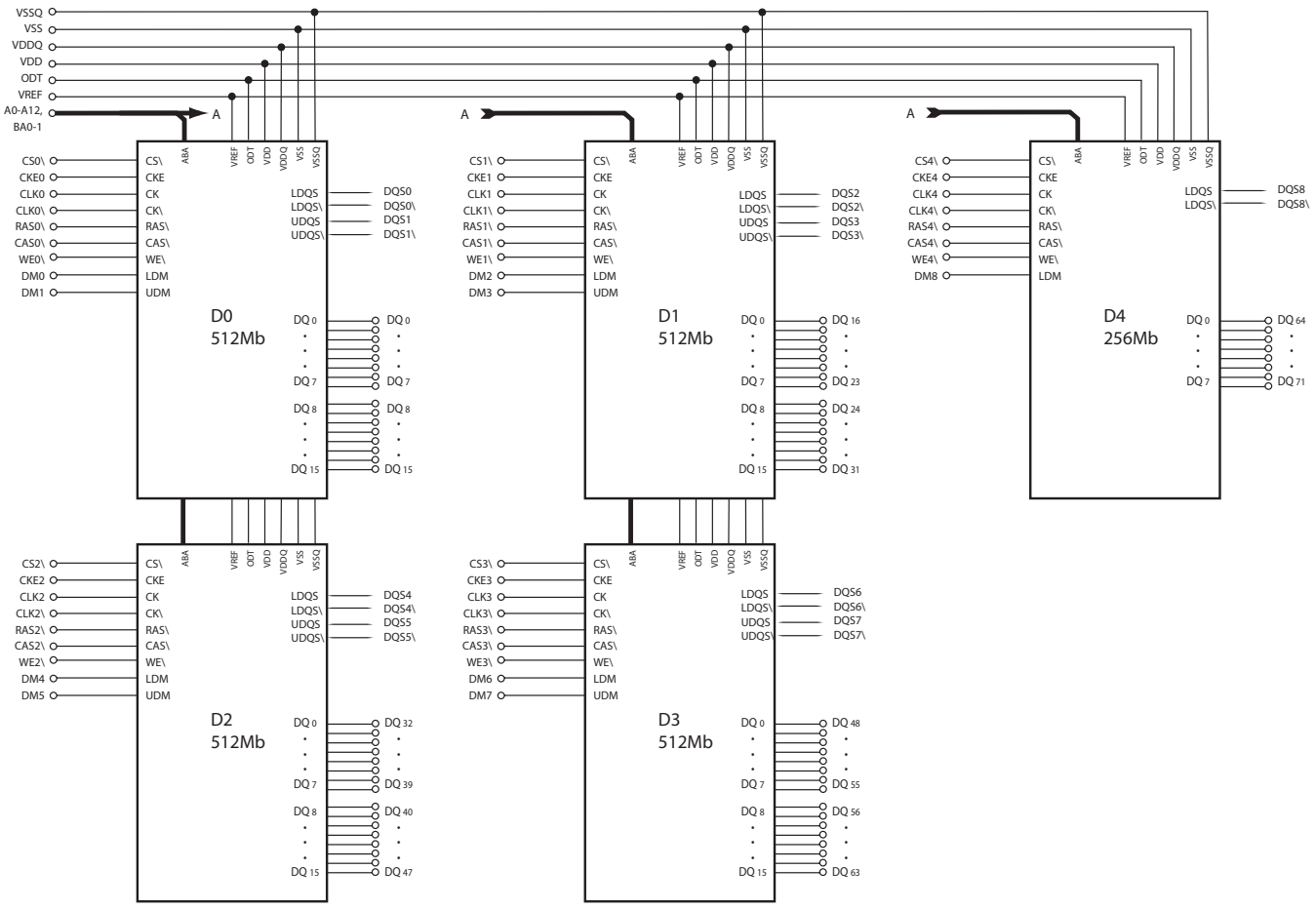


Figure 2B - 32M X 72 Functional Block Diagram



1.

Figure 2C - 32M X 80 Functional Block Diagram

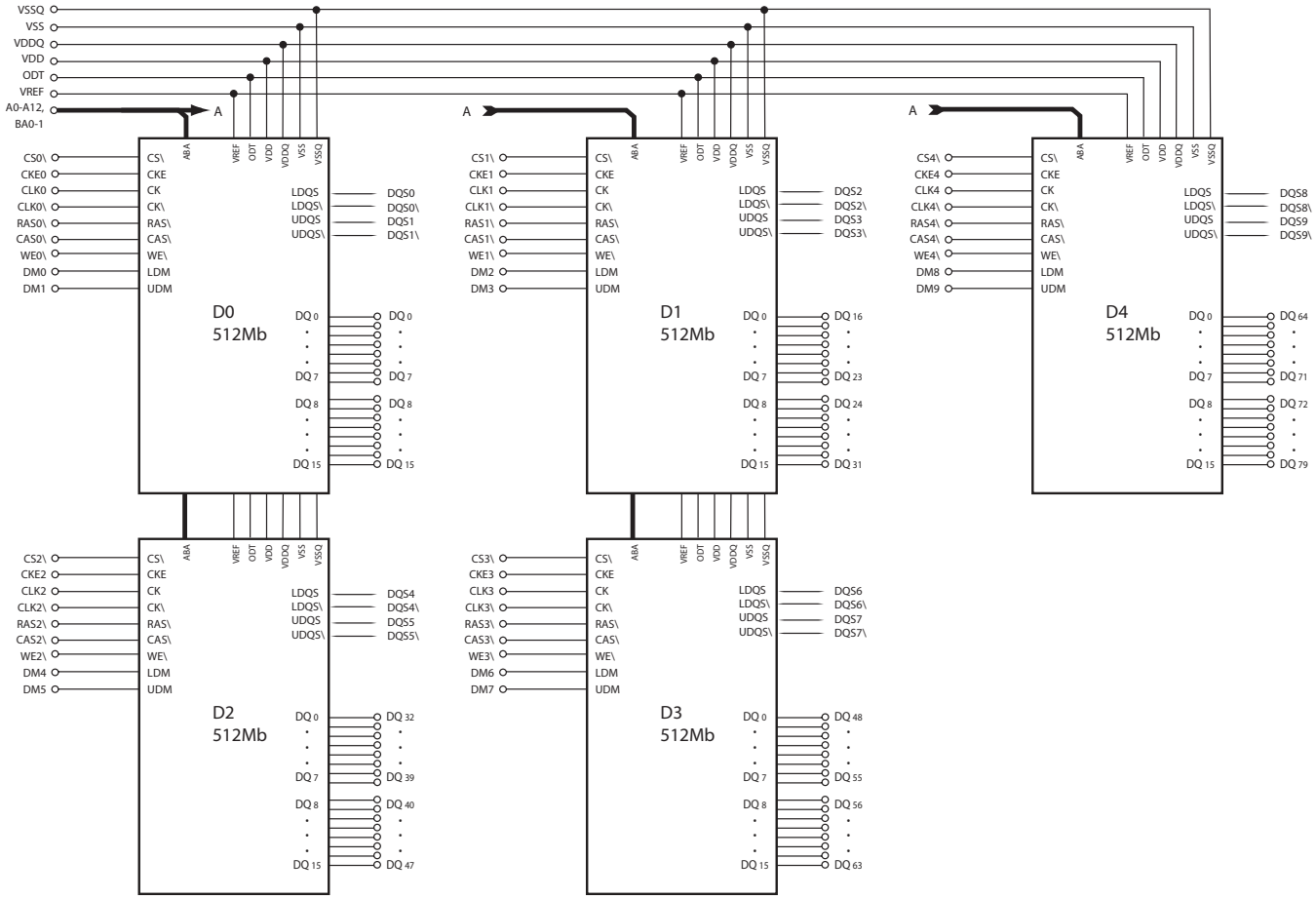


Figure 2D - 64M X 64 Functional Block Diagram

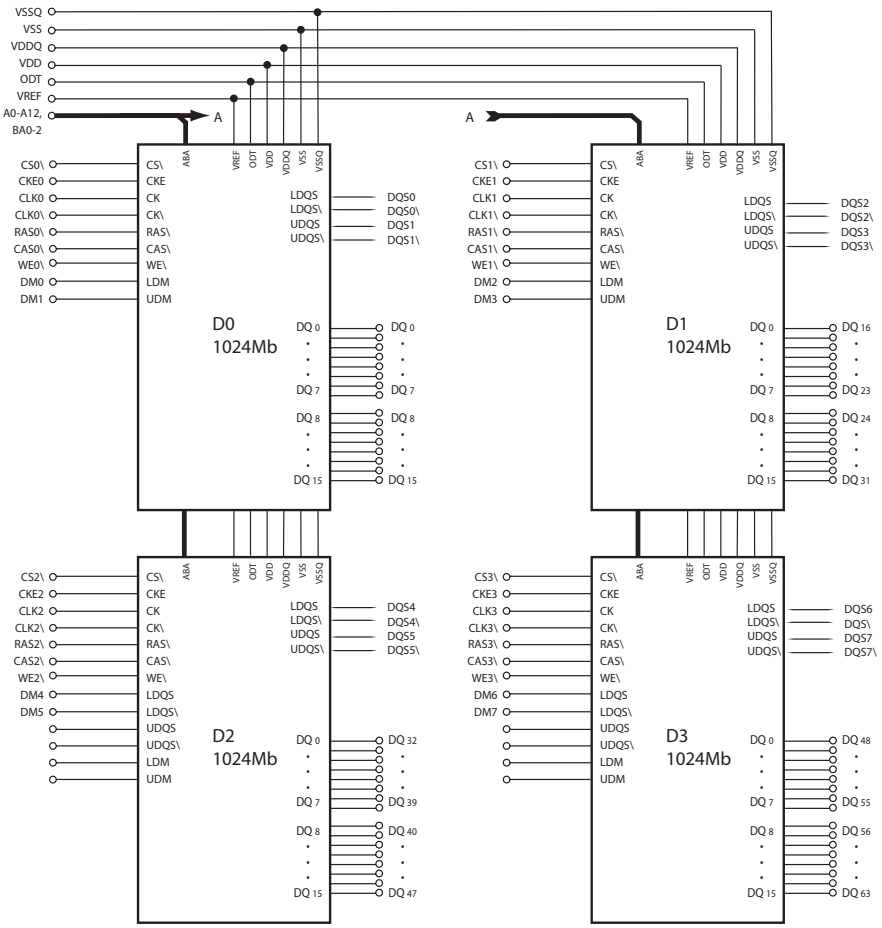


Figure 2E - 64M X 72 Functional Block Diagram

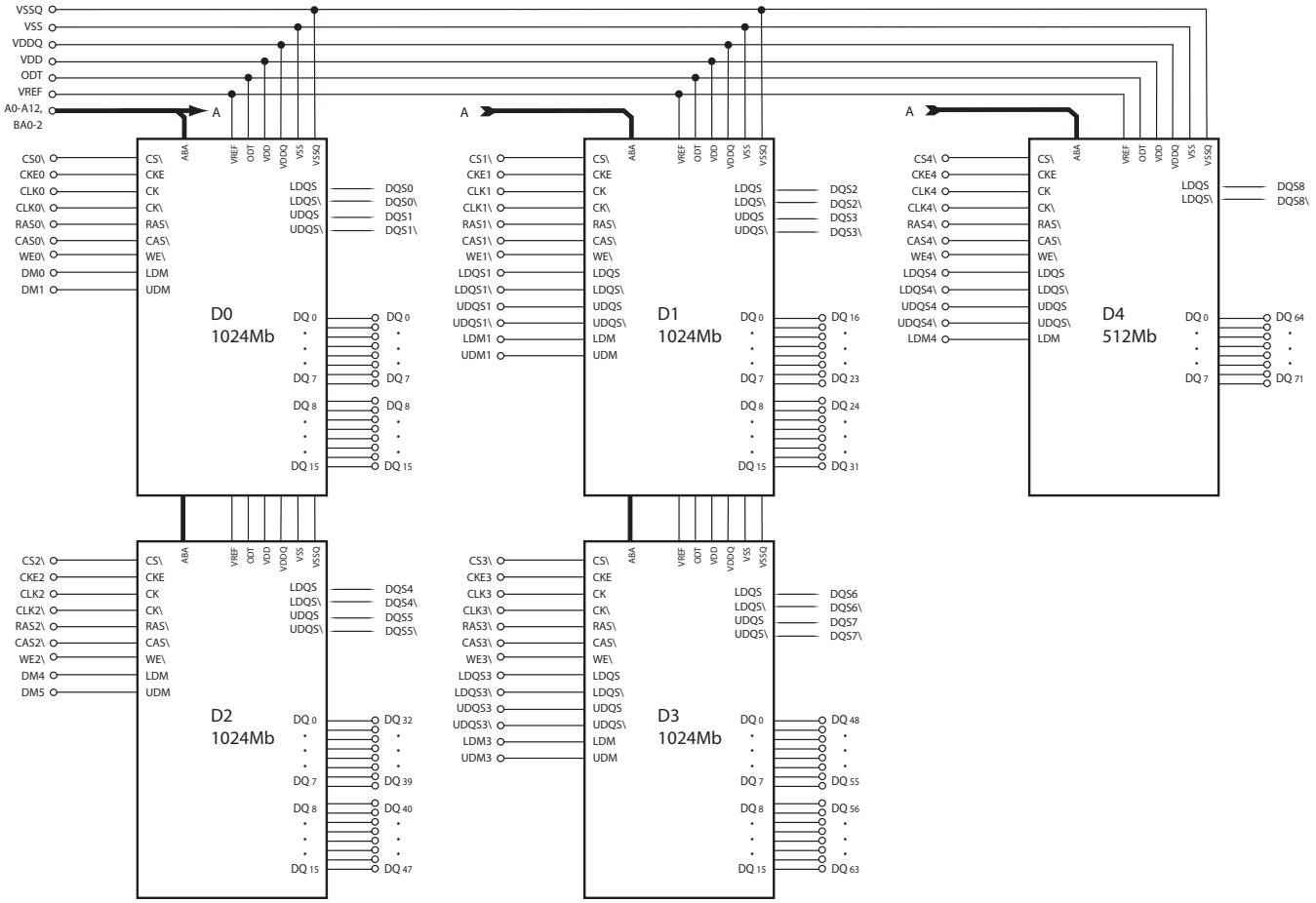


Figure 2F - 64M X 80 Functional Block Diagram

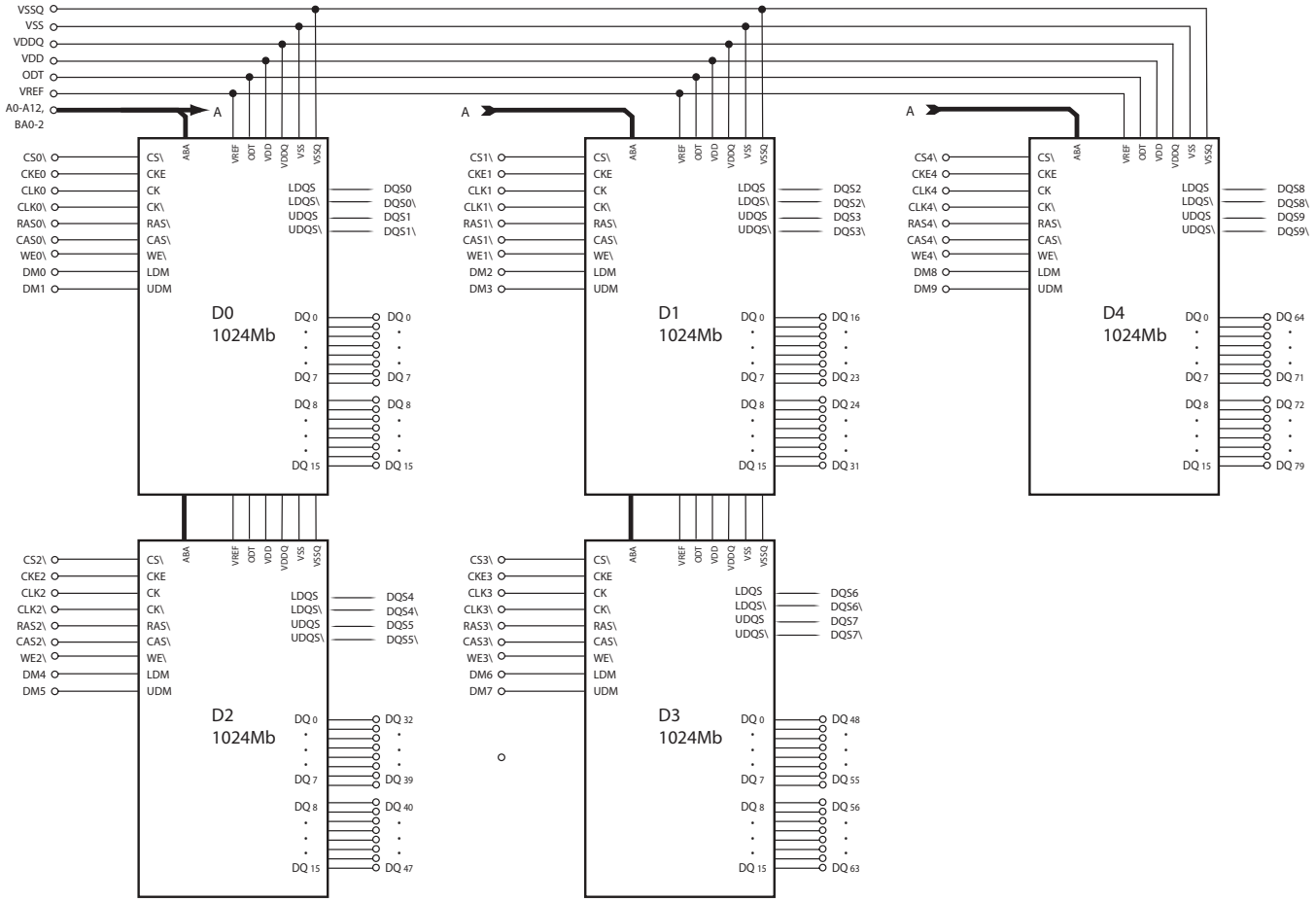


Figure 2G - 32 Meg x 16 Internal Die Configuration Functional Block Dia-

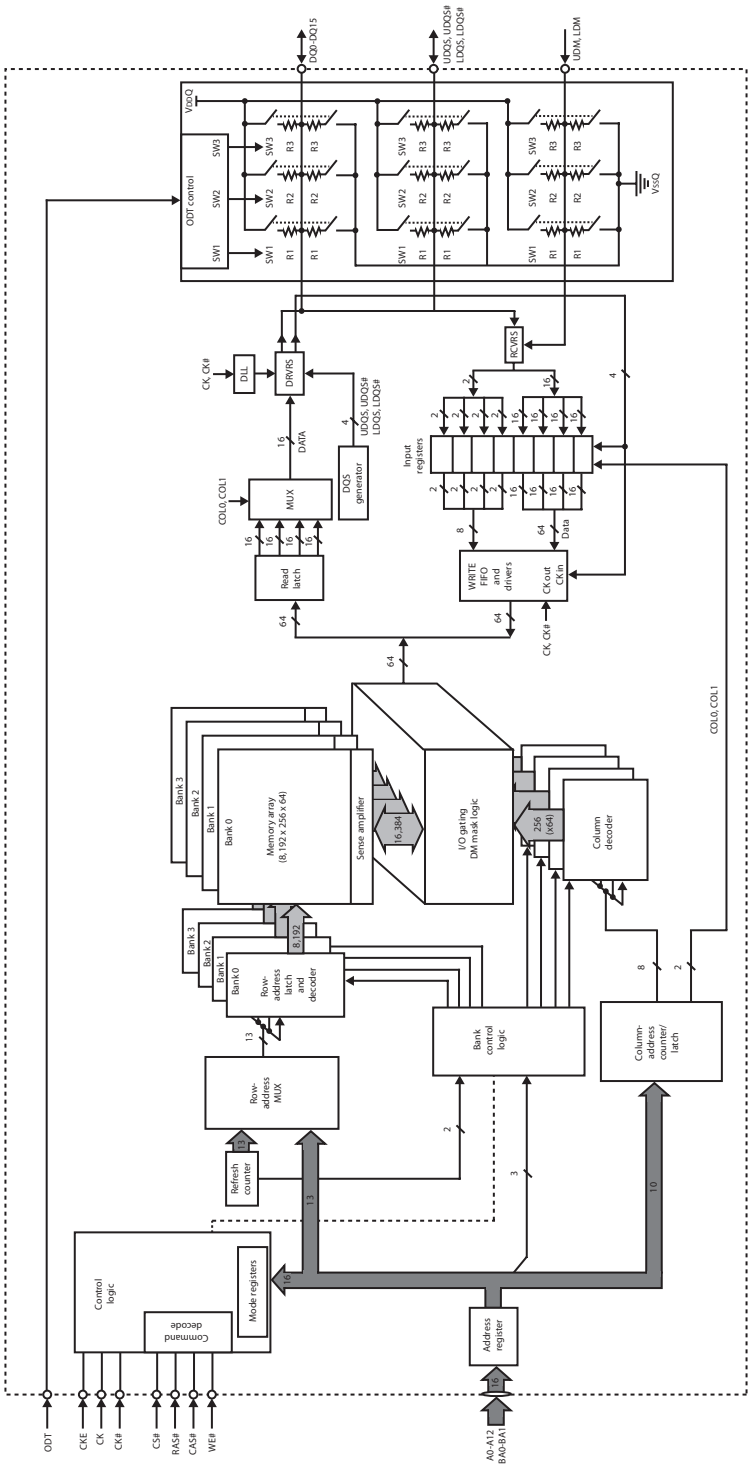


Figure 2H - 64 Meg x 16 Internal Die Configuration Functional Block Dia-

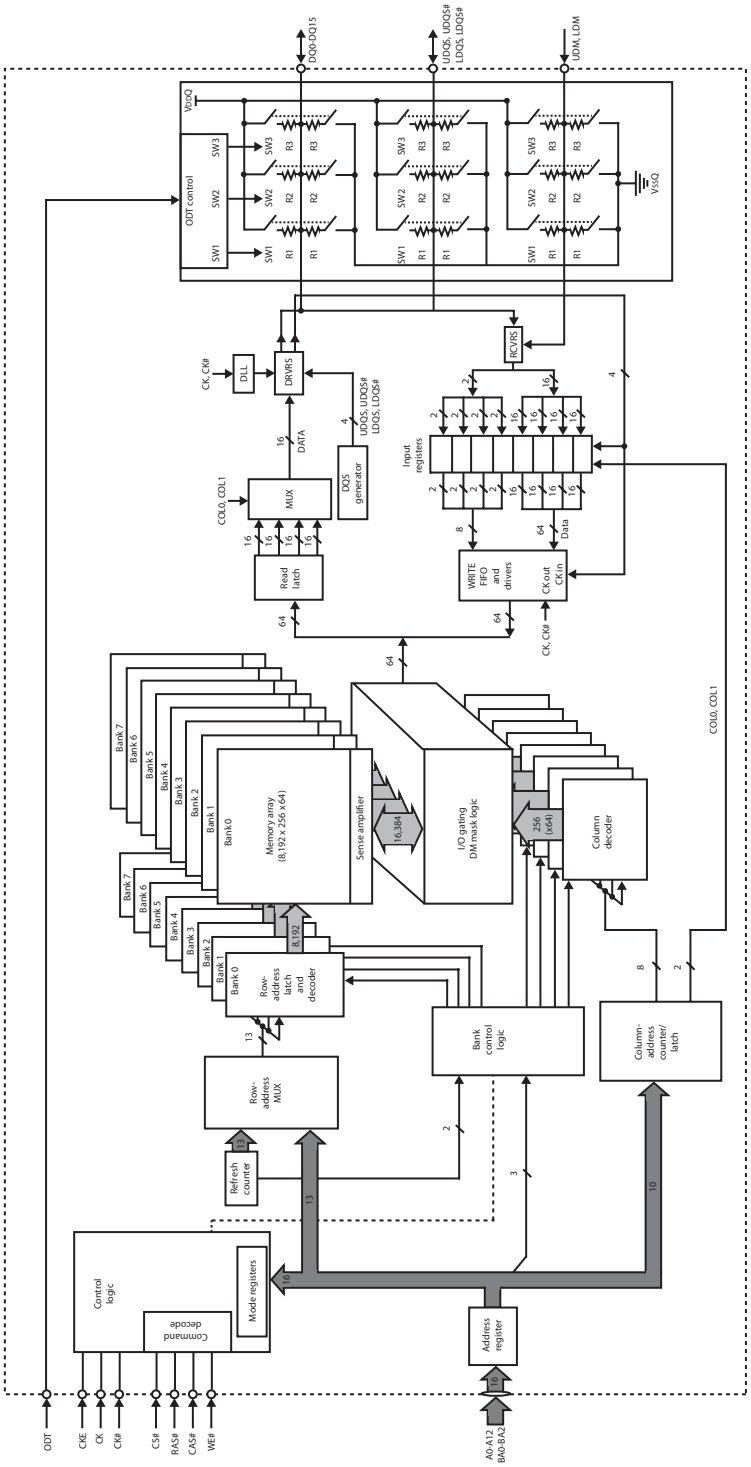


Figure 2I - 64 Meg x 8 Internal Die Configuration Functional Block Dia-

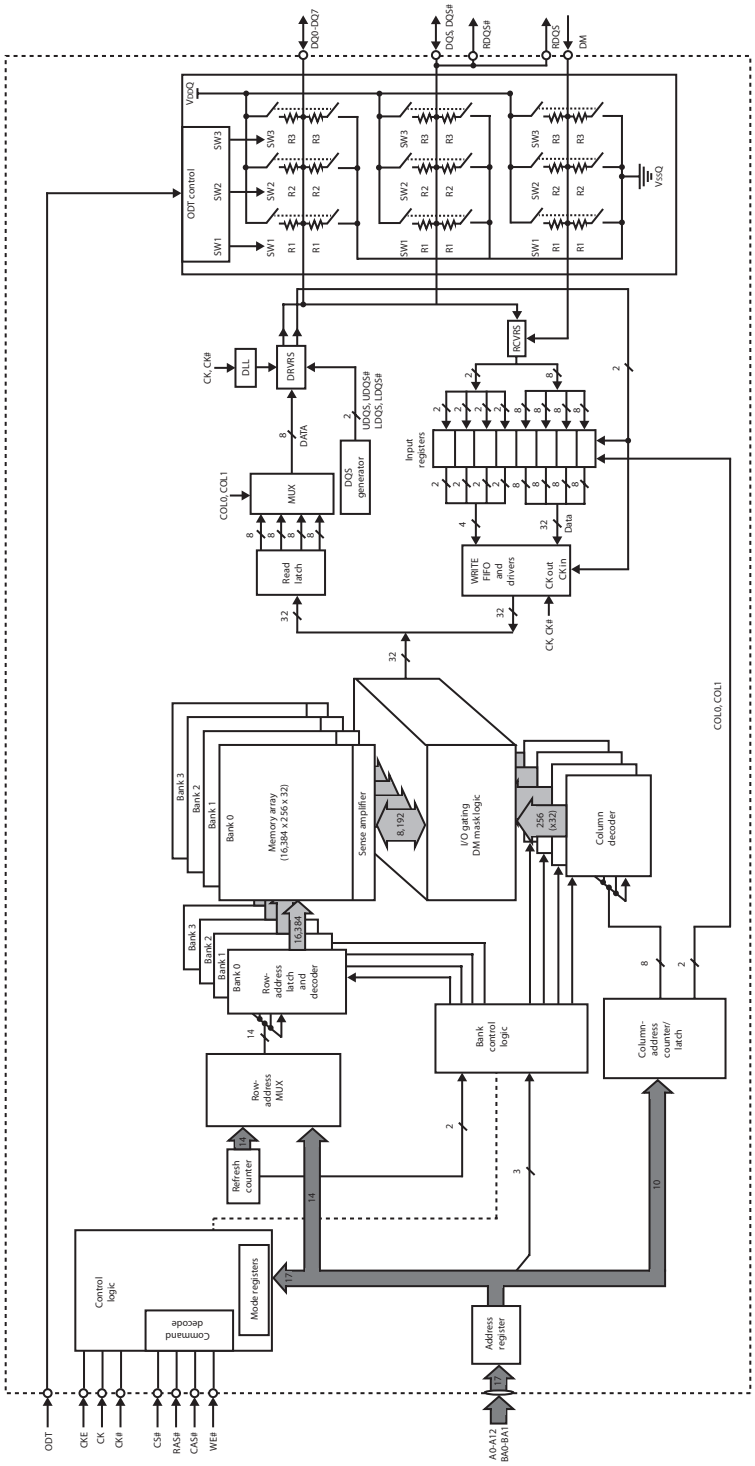
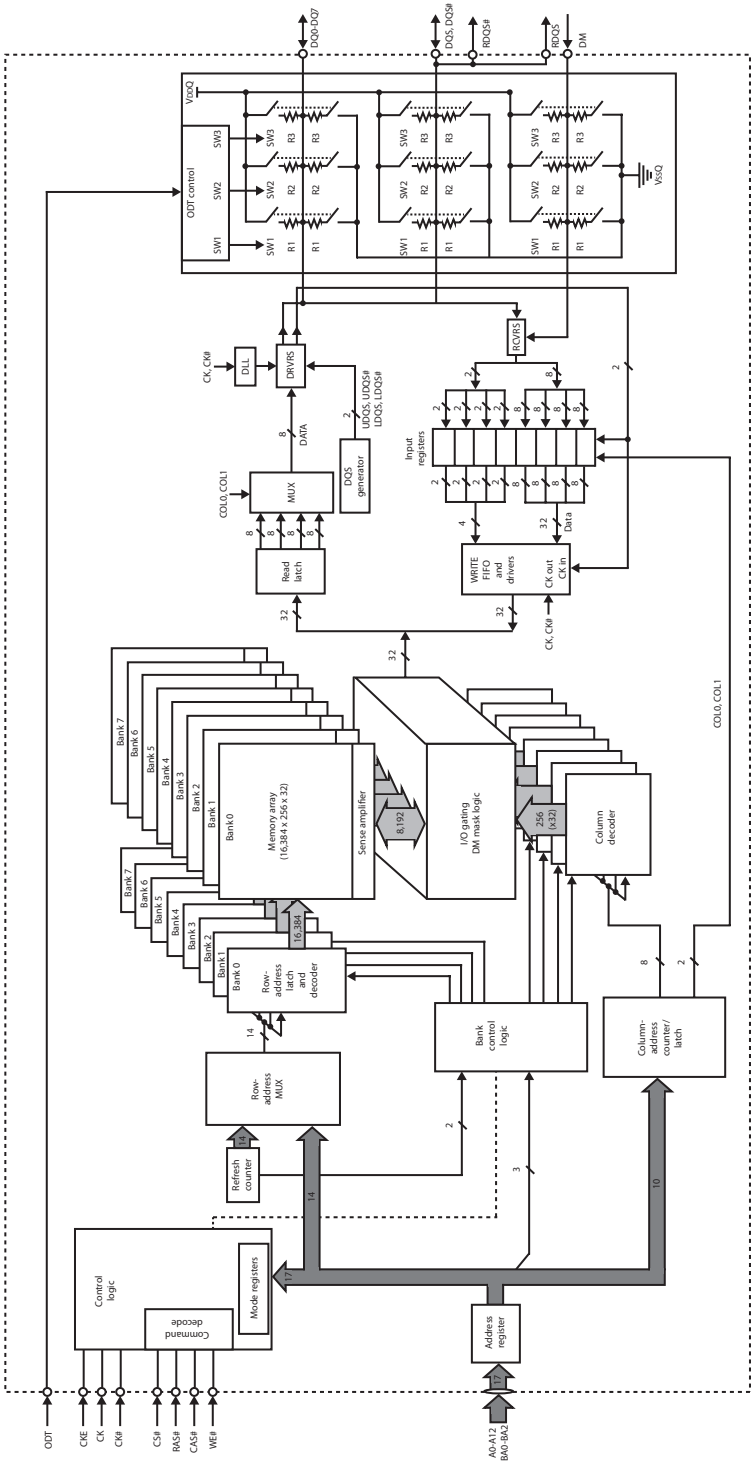


Figure 2J - 128 Meg x 8 Internal Die Configuration Functional Block Dia-



GENERAL DESCRIPTION

The STACKED DDR2 HiMOD famliy encompasses 6 devices with memory denisities of 2.0-5.0Gb. This DDR2 module family are packaged in a 25mm x 25mm – 255 ball, PBGA with a 1.27mm ball pitch. The module is a high speed CMOS random-access memory device consisting of 4(5) monolythic silicon circuits each containing 512M(1024M) bits. Each chip is internally configured as an 4(8) bank SDRAM. Each of the chips 131,217,728 bit banks is organized as 8,192 rows by 1024 columns by 16bits. Each of the 4(5) Silicon devices contained in module, equates to one 16 bit word or two 8 bit bytes, with each BYTE containing Data Mask and Data Strobes. The module's control structure is defined with each of the internal silicon die having CS\, CKE, CLK,CLK\, RAS\, CAS\ and WE as well as the Data Mask and Strobe control bus for the I/O. These controls are DQSx, DQSx\, and DMx.

FUNCTIONAL DESCRIPTION

This module uses the double-data-rate (DDR) architecture to achieve high-speed operation. The double-data-rate architecture is a 4n-prefetch architecture with an interface designed to transfer two data words per clock cycle via the I/O pins. A single READ or WRITE access for the 5.0Gb DDR2 iMOD effectively consists of a single 4n-bit wide, one clock cycle transfer.

A bidirectional data strobe, one per upper and lower byte (DQSx,DQSx\ ), is transmitted externally, along with data, for use in data capture at the end-point receiver. Data Strobes are transmitted by the DDR SDRAM during READ operations and by the memory controller during WRITE operations. Each strobe controls each of one bytes contained within each of the (5) silicon chips contained in the module.

The module is operated from a differential clock (CLKx, CLKx\); the crossing of CLKx going HIGH and CLKx\ going LOW will be referred to as the positive edge of CLK. Commands (address and control signals) are registered at every positive edge of CLK. Input data is registered on both edges of DQSx, and output data is referenced to both edges of DQSx, as well as to both edges of CLK. READ and WRITE accesses to the DDR2 memory are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The module provides for programmable READ or WRITE burst lengths of (4) four or (8) eight locations. DDR2 SDRAMs support for interrupting a BURST READ of eight with another READ or BURST WRITE of eight, then another WRITE. An AUTO PRECHARGE function may be enabled to provide SELF-TIMED row PRECHARGE that is initiated at the end of the burst access.

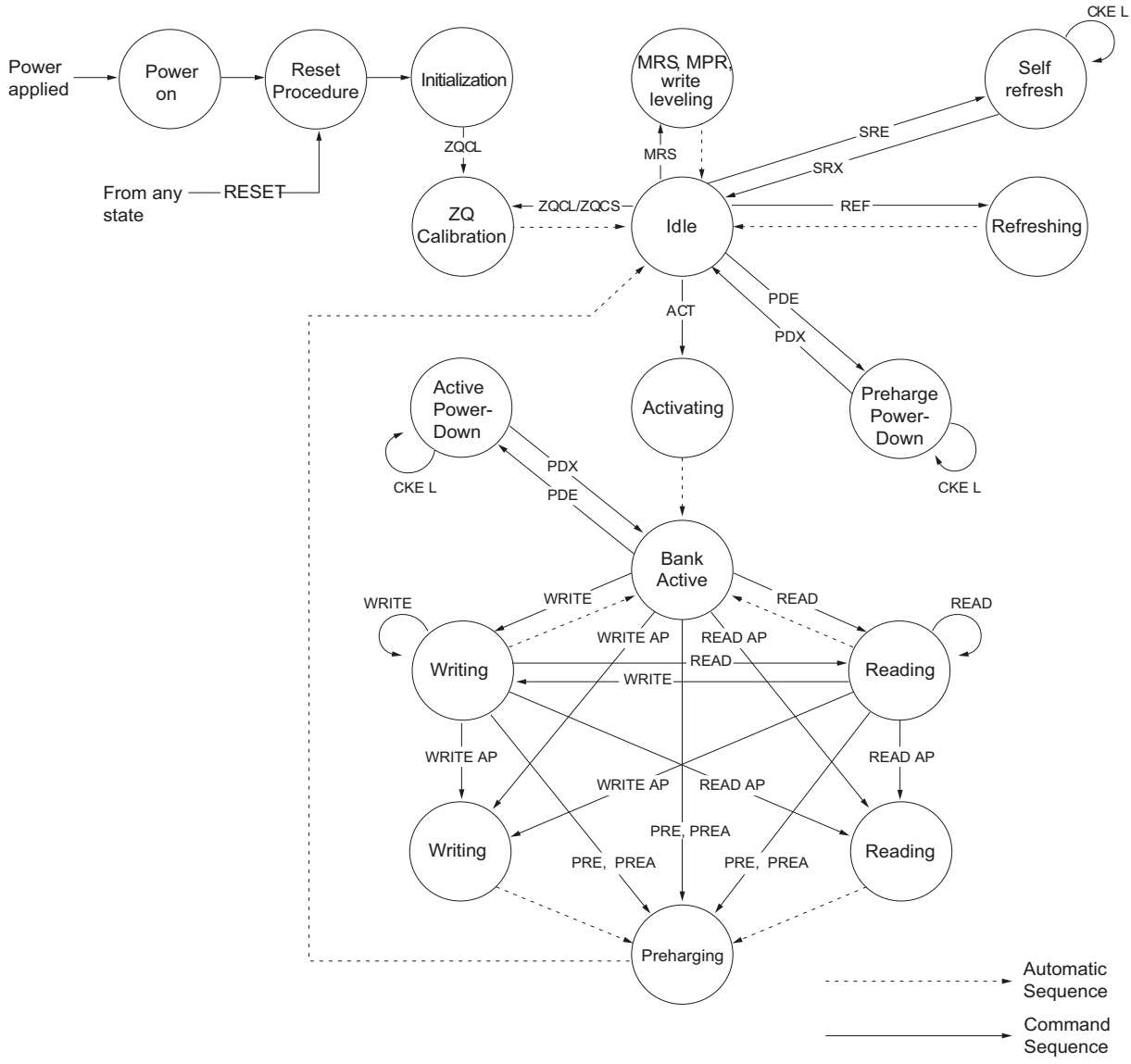
The pipelined, multi-banked architecture of the architecture allows for concurrent operations, therefore providing high effective bandwidth, by hiding row PRECHARGE and activation time.

GENERAL NOTES

- The functionality and the timing listed in this ST9D2xxGxxBG5 datasheet are for the DLL-enabled mode of operation.
- Throughout the datasheet, the various figures and text refer to DQ0-DQxx as "DQ". The DQ term is to be interpreted as any or all of the "80 [72] [64]" DQ lines present in this product definition.
- Inference to complete functionality is described throughout this document. Any page or discussion within a page may have been simplified to convey "the" topic and may not be inclusive of all requirements.

STATE DIAGRAM

Figure 4 - Simplified State Diagram

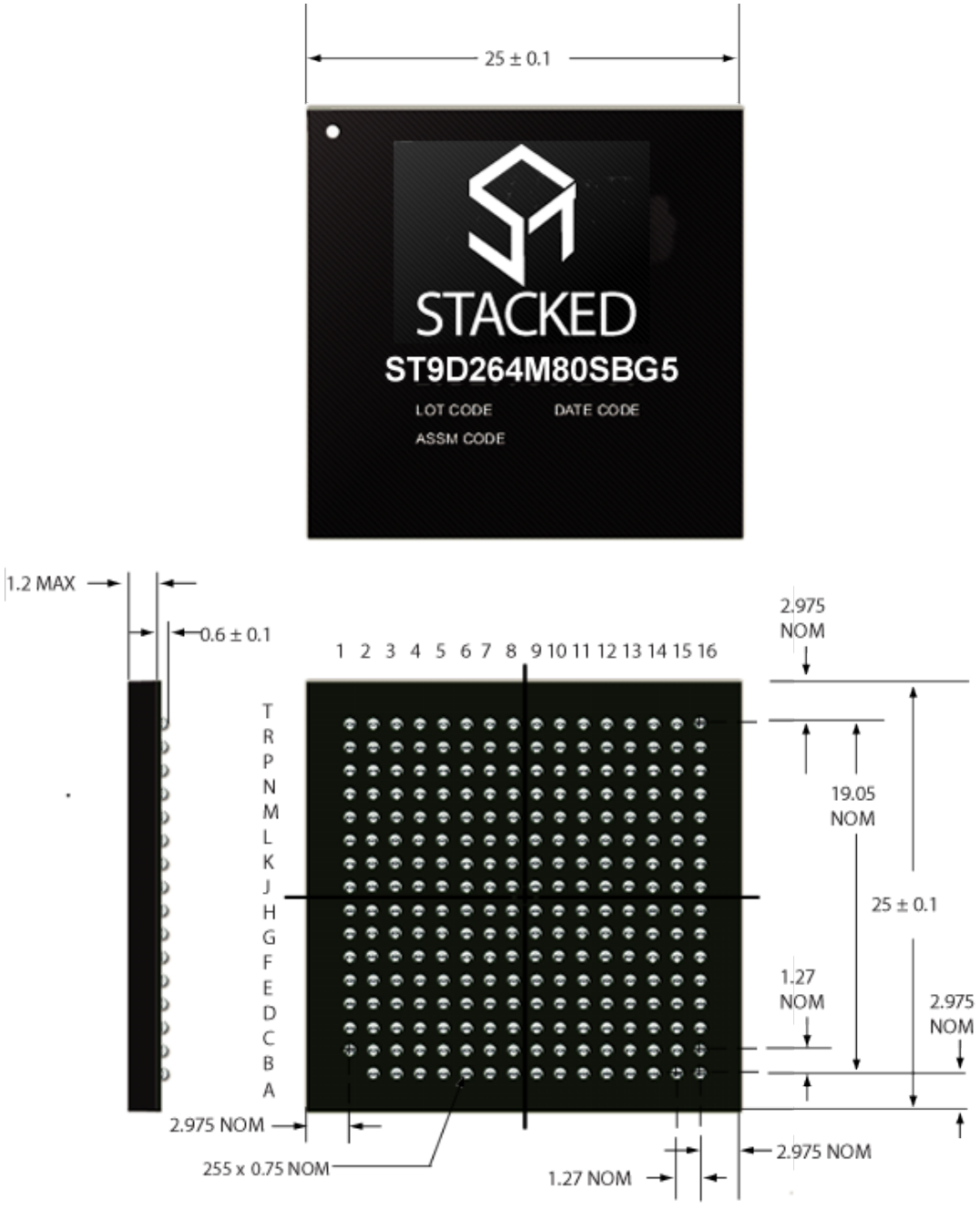


ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE

PREA=PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry

SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

Figure 5 - Mechanical Drawing



Note: All dimensions in mm

Table 4: Absolute Maximum DC Ratings

Symbol	Parameter		MIN	MAX	UNIT
V_{DD}	Voltage on V_{DD} pin relative to V_{ss}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{ss}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55.0	125.0	°C
T_{CASE}	Device Operating Temperature		-55.0	125.0	°C
I_I	Input Leakage current; Any input 0V< V_{IN}<V_{DD}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	CMD/ADR, RAS\, CAS\, WE\, CS\, CKE	-25.0	25.0	µA
		CK, CK\	-10.0	10.0	µA
		DM	-5	5	µA
I_{OZ}			-5	5	µA
I_{VREF}			-18	18	µA

Table 5: Recommended DC Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Reference Voltage	$V_{REF(DC)}$	0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
I/O Termination Voltage	V_{TT}	$V_{REF(DC)}$ - 0.04	$V_{REF(DC)}$	$V_{REF(DC)}$ + 0.04	V

NOTES:

1. LDI's DDR2, 255PBGA iMOD internally ties V_{DD} and V_{DDQ} together as well as V_{ss} and V_{ssQ}.

2. V_{REF} is expected to equal V_{DD}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-Peak variations in the DC level of the same, Peak-to-Peak noise (non-common mode) on V_{REF} may not exceed ± 1 percent of the DC value. Peak-to Peak AC noise on V_{REF} may not exceed ± 2 percent of V_{REF}(DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.

3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

Table 6: Input, Input/Output Capacitance

Parameter	Symbol	MIN	TYP	MAX	UNITS	NOTES
Input capacitance: CKx and CKx\	C_{CK}	3.5	4.0	5.0	pF	1
Input capacitance: Ax, BAx, ODT	C_I	20	25	30	pF	1
Input/Output capacitance: DQx, LDQSx, LDQSx\, UDQSx, UDQSx\, LDMx, UDMx, CSx\, RASx\, CASx\, WEx\, CKEx	C_{IO}	6.5	7	8	pF	1

NOTES:

1. This parameter is sampled. V_{DD} = +1.8V ± 0.1V, $V_{DD}Q$=V_{DD} (internally tied), V_{REF} = Vss, f=100MHz, Tc=25°C
   V_{OUT}(DC) = V_{DD}/2, Vout (peak-to-peak)=0.1V. xDMx input is grouped with IO-balls, reflecting the fact that they are matched in loading.

2. The capacitance per ball group will not differ by more than this maximum amount for any given iMOD device.

Table 7: General IDD Parameters

IDD Parameters	25 800Mbps	3 667Mbps	38 533Mbps	50 400Mbps	UNITS
CL (I_{DD})	6	5	4	3	^tCK
^tRCD (I_{DD})	15	15	15	15	ns
^tRC (I_{DD})	60	60	60	55	ns
tRRD (I_{DD})	10	10	10	10	ns
^tCK (I_{DD})	2.5	3	3.75	5	ns
^tRAS (I_{DD})	45	45	45	40	ns
^tRP (I_{DD})	70000	70000	70000	70000	ns
^tRFC (I_{DD})	127.5	127.5	127.5	127.5	ns
^tFAW (I_{DD})	Defined by pattern in Table 8 below				ns

Table 8: IDD7 Timing Patterns (4 - Bank interleave READ Operation)

Speed Grade	IDD7 Timing Patterns
25	A_0 RA_0 D D A_1 RA_1 D D A_2 RA_2 D D A_3 RA_3 D D D D D D D D D
3	A_0 RA_0 D D A_1 RA_1 D D A_2 RA_2 D D A_3 RA_3 D D D D D D
37	A_0 RA_0 D A_1 RA_1 D A_2 RA_2 D A_3 RA_3 D D D A_4 RA_4 D A_5 RA_5 D
5	A_0 RA_0 A_1 RA_1 A_2 RA_2 A_3 RA_3 D D A_4 RA_4 A_5 RA_5 A_6 RA_6 A_7 RA_7 D D

Table 9: DDR2 IDD Specifications and Conditions

Parameter	Symbol	800Mbps 25	667Mbps 3	533Mbps 38	400Mbps 50	UNITS
Operating Current: One bank active-precharge tCL=tCK(IDD), tRC=tRC(IDD), tRAS=tRAS MIN(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus switching, Data bus switching	IDD0	400	375	375	375	mA
Operating Current: One bank active-READ-precharge current IOUT=0ma; BL=4, CL=CL(IDD), AL=0; tCK = tCK(IDD), tRCtRC(IDD), tRAS=tRAS MIN(IDD), tRCD=tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus is switching; Data bus is switching	IDD1	475	450	450	450	mA
Precharge POWER-DOWN current All banks idle; tCK-tCK(IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	35	35	35	35	mA
Precharge quiet STANDBY current All banks idle; tCK=tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	130	130	130	130	mA
Precharge STANDBY current All banks idle; tCK-=tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	150	130	130	130	mA
Active POWER-DOWN current MRS[12]=0	IDD3P	100	75	30	30	mA
MRS[12]=1		50	50	10	10	
Active STANDBY current All banks open; tCK=tCK(IDD), tRAS MAX(IDD), tRP=tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	175	160	160	160	mA
Operating Burst WRITE current All banks open, continuous burst writes; BL=4, CL=CL(IDD), tRP=tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	800	675	675	675	mA
Operating Burst READ current All banks open, continuous burst READS, Iout=0mA; BL=4, CL=CL(IDD), AL=0; tCL=tCK(IDD), tRAS=tRAS MAX(IDD), tRP=tRP(IDD); CKE is HIGH, CS\ is HIGH btw. valid commands; Address and Data bus inputs switching	IDD4R	750	625	625	625	mA
Burst REFRESH current tCK=tCK(IDD); refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH btw. valid commands; Other control, Address and Data bus inputs are switching	IDD5	750	725	725	725	mA
Self REFRESH current CK and CK\ at 0V; CKE ≤ 0.2V; Other control, address and data inputs are floating	IDD6	35	35	35	35	mA
	IDD6L	25	25	25	25	
Operating bank Interleave READ current 1xtCK(IDD); tCK=tCK(IDD), tRC=tRC(IDD), tRRD=tRRD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7	1300	1150	1150	1150	mA

Table 10: AC Timing Specifications

	Parameter		Symbol	[I] 25 400MHz/ 800Mbps MIN	[I] 25 400MHz/ 800Mbps MAX	[I, E, M] 3 333MHz/ 667Mbps MIN	[I, E, M] 3 333MHz/ 667Mbps MAX	[I, E, M] 38 267MHz/ 533Mbps MIN	[I, E, M] 38 267MHz/ 533Mbps MAX	[I, E, M] 50 200MHz/ 400Mbps MIN	[I, E, M] 50 200MHz/ 400Mbps MAX	UNITS	NOTES
CLOCK	Clock Cycle Time	CL=6	$^tCK_{AVG}$	2.5	8							ns	6-9
		CL=5	$^tCK_{AVG}$	3	8	3	8						
		CL=4	$^tCK_{AVG}$	3.75	8	3.75	8	3.75	8	5	8		
		CL=3	$^tCK_{AVG}$							5	3		
	Clock High Time		$^tCH_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^tCK	10
	Clock Low Time		$^tCL_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52		
	Half Clock Period		^tHP	MIN = Lesser of ^tCH and ^tCL, MAX = n/a								ps	11
	Absolute ^tCK		$^tCK_{(abs)}$	MIN = ^tCK (AVG) MIN + ^tJITPER (MIN), MAX = ^tCK (AVG) MAX + ^tJITPER (MAX)								ps	
	Absolute ^tCK high-level width		$^tCH_{(abs)}$	MIN = ^tCK (AVG) MIN x ^tCH (AVG) MIN + ^tJITPER (MIN) MAX = ^tCK (AVG) MAX x ^tCH (AVG) MAX + ^tJITDTY (MAX)								ps	
	Absolute ^tCK low-level width		$^tCL_{(abs)}$	MIN = ^tCK (AVG) MIN x ^tCH (AVG) MIN + ^tJITPER (MIN) MAX = ^tCK (AVG) MAX x ^tCH (AVG) MAX + ^tJITDTY (MAX)								ps	
Clock Jitter	Clock Jitter - Period		^tJITPER	-100	100	-125	125	-125	125	-125	125	ps	12
	Clock Jitter - Half Period		^tJITDTY	-100	100	-125	125	-125	125	-150	150	ps	13
	Clock Jitter - Cycle to Cycle		^tJITCC	200		250	250	250				ps	14
	Cumulative Jitter error, 2 cycles		$^tERR2PER$	-150	150	-175	175	-175	175	-175	175	ps	
	Cumulative Jitter error, 3 cycles		$^tERR3PER$	-175	175	-225	225	-225	225	-225	225	ps	15
	Cumulative Jitter error, 4 cycles		$^tERR4PER$	-200	200	-250	250	-250	250	-250	250	ps	15
	Cumulative Jitter error, 6-10 cycles		$^tERR10PER$	-300	300	-350	350	-350	350	-350	350	ps	15,16
	Cumulative Jitter error, 11-50 cycles		$^tERR50PER$	-450	450	-450	450	-450	450	-450	450	ps	15
Data Strobe-Out	DQS output access time from CK/CK\		^tDQSCK	-350	350	-400	400	-450	450	-500	500	ps	19
	DQS READ preamble		^tRPRE	MIN = 0.9 x ^tCK, MAX = 1.1 x ^tCK								^tCK	17-19
	DQS READ postamble		^tRPST	MIN = 0.9 x ^tCK, MAX = 1.1 x ^tCK								^tCK	17-20
	DQS Low-Z window from CK/CK\		$^tLZ1$	MIN = ^tAC (MIN), MAX = ^tAC (MAX)								ps	19,21,22
Data Strobe-In	Positive DQS latching edge to assoc. Clock edge		^tDQSS	MIN = -0.25 x ^tCK, MAX = +0.25 x ^tCK								^tCK	18
	DQS input-high pulse width		^tDQSH	MIN =0.35 x ^tCK, MAX = n/a								^tCK	18
	DQS input-low pulse width		^tDQSL	MIN =0.35 x ^tCK, MAX = n/a								^tCK	18
	DQS falling edge to CK rising - setup time		^tDSS	MIN =0.2 x ^tCK, MAX = n/a								^tCK	18
	DQS falling edge from CK rising - hold time		^tDSH	MIN =0.2 x ^tCK, MAX = n/a								^tCK	18
	WRITE preamble setup time		^tWPRES	MIN =0, MAX = n/a								ps	23,24
	DQS WRITE preamble		^tWPRE	MIN =0.35 x ^tCK, MAX = n/a								^tCK	18
	DQS WRITE postamble		^tWPST	MIN =0.4 x ^tCK, MAX = 0.6 x ^tCK								^tCK	18,25
	WRITE command to first DQS latching transition		-	MIN = WL - ^tDQSS, MAX = WL + ^tDQSS								^tCK	
Data-Out	DQ output access time from CK/CK\		^tAC	-400	400	-450	450	-500	500	-600	600	ps	19
	DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	-	200	-	240	-	300	-	350	ps	26,27
	DQ hold from next DQS strobe		^tQHS	-	300	-	340	-	400	-	450	ps	28
	DQ-DQS, Hold, DQS to first DQ to go non valid, per access		^tQH	MIN = ^tHP - ^tQHS, MAX = n/a								ps	26-28
	Data-out High-Z window from CK/CK\		^tHZ	MIN = n/a, MAX = ^tAC (MAX)								ps	19,21,29
	DQ Low-Z window from CK/CK\		$^tLZ2$	MIN = 2 x ^tAC (MIN), MAX = ^tAC (MAX)								ps	19,21,22
	Data valid output window (DVW)		^tDVW	MIN = ^tQH - ^tDQSQ, MAX = n/a								ps	26,27
Data-In	DQ and DM input setup time relative to DQS		^tDS_B	50	-	100	-	100	-	150	-	ps	26,30,31
	DQ and DM input hold time relative to DQS		^tDH_B	125	-	175	-	225	-	275	-	ps	26,30,31
	DQ and DM input setup time relative to DQS		^tDS_A	250	-	300	-	350	-	400	-	ps	26,30,31
	DQ and DM input hold time relative to DQS		^tDH_A	250	-	300	-	350	-	400	-	ps	26,30,31
	DQ and DM input pulse width (for each input)		^tDIPW	MIN = 0.35 x ^tCK, MAX = n/a								^tCK	18,32

Table 10: AC Timing Specifications Continued

	Parameter	Symbol	[I] 25 400MHz/ 800Mbps MIN	[I] 25 400MHz/ 800Mbps MAX	[I, E, M] 3 333MHz/ 667Mbps MIN	[I, E, M] 3 333MHz/ 667Mbps MAX	[I, E, M] 38 267MHz/ 533Mbps MIN	[I, E, M] 38 267MHz/ 533Mbps MAX	[I, E, M] 50 200MHz/ 400Mbps MIN	[I, E, M] 50 200MHz/ 400Mbps MAX	UNITS	NOTES
COMMAND AND ADDRESS	Address and Control input pulse width for each input	^tIPW	0.6	-	0.6	-	0.6	-	0.6	-	^tCK	18,34
	Address and Control input setup time	^tIS_B	175	-	200	-	250	-	350	-	ps	31,33
	Address and Control input hold time	^tIH_B	250	-	275	-	375	-	475	-	ps	31,33
	Address and Control input setup time	^tIS_A	375	-	400	-	500	-	600	-	ps	31,33
	Address and Control input hold time	^tIH_A	375	-	400	-	500	-	600	-	ps	31,33
	CAS\ to CAS\ command delay	^tCCD	2	-	2	-	2	-	2	-	^tCK	18
	ACTIVE to ACTIVE command (same bank)	^tRC	55	-	55	-	55	-	55	-	ns	18,34
	ACTIVE bank a to ACTIVE bank b Command	^tRRD	10	-	10	-	10	-	10	-	^tCK	18,37
	ACTIVE to READ or WRITE delay	^tRCD	15	-	15	-	15	-	15	-	ns	18
	8 - Bank activate period	^tFAW	45	-	50	-	50	-	50	-	ns	18,38
	ACTIVE to PRECHARGE	^tRAS	40	70000	40	70000	40	70000	40	70000	ns	18,34,35
	Internal READ to PRECHARGE command delay	^tRTP	7.5	-	7.5	-	7.5	-	7.5	-	ns	18,37,39
	WRITE recovery time	^tWR	15	-	15	-	15	-	15	-	ns	18,37
	Auto PRECHARGE WRITE recovery + PRECHARGE time	^tDAL	MIN = ^tWR + ^tRP, MAX = n/a								ns	40
	Internal WRITE to READ command delay	^tWTR	7.5	-	7.5	-	7.5	-	10	-	ns	18,37
	PRECHARGE command period	^tRP	15	-	15	-	15	-	15	-	ns	18,36
	PRECHARGE ALL command period	^tRPA	17.5	-	18	-	18.75	-	20	-	ns	18
	LOAD MODE, command Cycle time	^tMRD	2	-	2	-	2	-	2	-	^tCK	42
REFRESH	CKE LOW to CK, CK\ uncertainty	^tDELAY	MIN limit = ^tIS + ^tCK + ^tIH, MAX limit = n/a								ns	18,41
	REFRESH to ACTIVE or REFRESH to REFRESH command interval	^tRFC	127.5	-	127.5	-	127.5	-	127.5	-	ns	18,41
	Average periodic REFRESH interval [industrial temp]	$^tREF[I]$	-	7.8	-	7.8	-	7.8	-	7.8	µs	18,41
	Average periodic REFRESH interval [extended temp]	$^tREF[E]$	-	3.9	-	3.9	-	3.9	-	3.9	µs	18,41
	Average periodic REFRESH interval [military temp]	$^tREF[M]$	-	3.9	-	3.9	-	3.9	-	3.9	µs	18,41
S. REFRESH	Exit SELF REFRESH to NON READ command	^tXSNR	MIN limit = ^tRFC (MIN) + 10, MAX limit = n/a								ns	
	Exit SELF REFRESH to READ command	^tXSRD	MIN limit = 200, MAX limit = n/a								^tCK	18
	Exit SELF REFRESH timing reference	^tISXR	MIN limit = ^tIS, MAX limit = n/a								ps	33,43
ODT	ODT turn-on delay	^tAOND	2								^tCK	18
	ODT turn-on delay	^tAON	^tAC(MIN)	^tAC(MAX) + 600	^tAC(MIN)	^tAC(MAX) + 700	^tAC(MIN)	^tAC(MAX) + 1000	^tAC(MIN)	^tAC(MAX) + 1000	ps	19,46
	ODT turn-off delay	^tAOPD	2.5								^tCK	18,45
	ODT turn-off delay	^tAOF	MIN limit = ^tAC (MIN), MAX limit = ^tAC (MAX) + 600								ps	47,48
	ODT turn-on (power-down mode)	^tAONPD	MIN limit = ^tAC (MIN) + 2000, MAX limit = 2 x ^tCK + ^tAC (MAX) + 1000								ps	
	ODT turn-off (power-down mode)	^tAOFPD	MIN limit = ^tAC (MIN) + 2000, MAX limit = 2.5 x ^tCK + ^tAC (MAX) + 1000								ps	
	ODT to power-down entry latency	^tANPD	3	-	3	-	3	-	3	-	^tCK	18
	ODT to power-down exit latency	^tAXPD	10	-	8	-	8	-	8	-	^tCK	18
	ODT enable from MRS command	^tMOD	12	-	12	-	12	-	12	-	ns	18
PWR-DN	Exit active POWER-DOWN to READ command, MR[12]=0	^tXARD	2	-	2	-	2	-	2	-	^tCK	18
	Exit active POWER-DOWN to READ command, MR[12]=1	^tXARD	8-AL	-	7-AL	-	6-AL	-	6-AL	-	^tCK	18
	Exit PRECHARGE POWER-DOWN to any non READ	^tXP	2	-	2	-	2	-	2	-	^tCK	18
	CKE Min. HIGH/LOW time	^vCKE	3	-	3	-	3	-	3	-	^tCK	18,44

Notes

1. All voltages are referenced to Vss.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the operation of the device are warranted for the full voltage range specified. ODT is disabled for all measurements that are not ODT specific.
3. Outputs measured with equivalent load
4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.0V in the test environment, and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between VIL(AC) and VIH(AC). Slew rates other than 1.0V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard.
6. CK and CK\ input slew rate is referenced at 1V/ns (2V/ns if measured differentially)
7. Operating frequency is only allowed to change during SELF REFRESH mode, PRECHARGE POWERDOWN mode, or SYSTEM RESET condition. SSC allows for small deviations in operating frequency, provided the SSC guidelines are satisfied.
8. The Clock's ^{t}CK (AVG) is the average clock over any 200 consecutive clocks and ^{t}CK(AVG) MIN is the smallest clock rate allowed (except for a deviation due to allowed clock jitter). Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
9. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range of 20-60kHz with an additional on percent ^{t}CK(AVG); however, the spread spectrum may not use a clock rate below ^{t}CK(AVG)MIN or above ^{t}CK(AVG) MAX.
10. MIN (^{t}CL, ^{t}CH)refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; ^{t}CH(AVG) and ^{t}CL(AVG) must be met with or without clock jitter and with or without duty cycle jitter. ^{t}CH(AVG) and ^{t}CL(AVG) are the average of any 200 consecutive CK falling edges. ^{t}CH limits may be exceeded if the duty cycle jitter is small enough that the absolute half period limits (^{t}CH[ABS], ^{t}CL[ABS])are not violated.
11. ^{t}HP(MIN) is the lesser of ^{t}CL and tCH actually applied to the device CK and CK\ inputs; thus, ^{t}HP(MIN) ≥ the lesser of ^{t}CL(ABS) MIN and ^{t}CH(ABS) MIN.
12. The period jitter (^{t}JITPER) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than those noted the Table titled "DLL LOCKED".
13. Half-period jitter (^{t}JITDTY) applies to either the high pulse of clock or the low pulse of the clock; however, the two cumulatively can not exceed ^{t}JITPER.
14. Cycle-to-cycle jitter (^{t}JITcc) is the amount of the clock period that can deviate from one cycle to the next. JEDEC specifies tighter jitter numbers during DLL Locking time. During DLL lock time, the jitter values should be 20 percent less than those noted in the table named "DLL LOCKED".
15. The cumulative jitter error (^{t}ERRNPER), where n is 2,3,4,5,6-10, or 11-50 is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
16. JEDEC specifies using ^{t}ERR6-10PER when derating clock-related output timing (see notes 19 and 48). LDI requires less derating on it's iMOD by allowing ^{t}ERR5PER to be used.
17. This parameter is not referenced to a specific voltage level but is specified when the device is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
18. Inputs to the module must be aligned to the associated clock, that is, the actual clock that latches it in. However, the input timing (in ns) references to the ^{t}CK(AVG) when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the ^{t}CK(AVG) rather than ^{t}CK:^{t}IPW, ^{t}DIPW, ^{t}DQSS, ^{t}DQSH, ^{t}DQSL, tDSS, ^{t}DSH, ^{t}WPST, and ^{t}WPRE.
19. Output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock hitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting ^{t}ERR5PER (MAX): ^{t}AC(MIN), ^{t}DQSCK(MIN), ^{t}LZDQS(MIN), ^{t}LZDQ(MIN), ^{t}AON(MIN); while the following parameters are required to be derated by subtracting ^{t}ERR5PER(MIN): ^{t}AC(MAX), ^{t}DQSCK(MAX), ^{t}HZ(MAX), ^{t}LZDQS(MAX), ^{t}LZDQ(MAX), ^{t}AON(MAX). The parameter ^{t}RPRE(MIN) is derated by subtracting ^{t}JITPER(MAX), while ^{t}RPRE(MAX) is derated by subtracting ^{t}JITPER(MIN). The parameter ^{t}RPST(MIN) is derated by subtracting ^{t}JITDTY(MAX), while ^{t}RPST(MAX) is derated by subtracting ^{t}JITDTY(MIN). Output timings that require tERR5per derating can be observed to have offsets relative to the clock; however, the total window will not degrade.
20. When DQS is used single-ended, the minimum limit is reduced by 100ps.
21. ^{t}HZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is not longer driving (^{t}HZ) or begins driving (^{t}LZ).
22. ^{t}LZ(MIN) will prevail over a ^{t}DQSCK(MIN) + ^{t}RPRE(MAX) condition.
23. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
24. It is recommended that DQs be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from HIGH-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
25. The intent of the "DON'T CARE" state after completion of the postamble is that the DQS driven signal should either be HIGH, LOW, or HIGH-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above VIH[DC]MIN), then it must not transition LOW (below VIH[DC]) prior to ^{t}DQSH(MIN).
26. Referenced to each output group:DQS0 /LDQS0\ with DQ0-7, DQS1, DQS1\ with DQ0-15, DQS2 /LDQS2\ with DQ16-23, DQS3 / DQS3\ with DQ24-31, DQS4 / DQS4\ with DQ32-39, DQS5 / DQS5\ with DQ40-47, DQS6 / DQS6\ with DQ48-55, DQS7 / DQS7\ with DQ56-63, DQS8 / DQS8\ with DQ64-71 and DQS9 / DQS9\ with DQ72-79.
27. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH=^{t}HP-^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
28. ^{t}QH = ^{t}HP-^{t}QHS; the worst case ^{t}Qh would be the lesser of ^{t}CL(ABS) MAX or

Notes Continued

^{t}CH(ABS) MAX times ^{t}CK(ABS) MIN-^{t}QHS. Minimizing the amount of ^{t}CH (AVG) offset and value of ^{t}JITPER will provide a larger ^{t}QH, which in turn will provide a larger valid data out window.

29. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK(MAX) + ^{t}RPST(MAX) condition.

30. The values listed are for the differential DQSx, DQSx\, strobes with a differential slew rate of 2V/ns (1V/ns for each single ended signal. There are two sets of values listed: ^{t}DSa, ^{t}DHa and ^{t}DSb, ^{t}DHb. The "a" values (for reference only) are equivalent to the baseline values of the "b" at VREF when the slew rate is 2V/ns, differentially. The baseline values, ^{t}DSb, ^{t}DHb are the JEDEC defined values, referenced from the logic trip points. ^{t}DSb is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal, while ^{t}DHb is referenced from VIL(DC) for a rising signal and VIH(DC) for a falling signal. If the differential DQS slew rate is not equal to 2V/ns, then the baseline values must be derated by adding the values from Table 28 and Table 29. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended and the baseline values must be derated using Table 30. Single-ended DQS data timing is referenced at DQS crossing VREF. The correct timing values for a single-ended DQS strobe are listed in Table 31-33. Listed values are already derated for slew rate variation and converted from baseline values to VREF values.

31. VIL/VIH DDR2 overshoot/undershoot. See AC Overshoot/Undershoot Specification.

32. For each input signal - not the group collectively.

33. There are two sets of values listed for command/address: ^{t}ISa, ^{t}IHa and ^{t}ISb, ^{t}IHb. The "a" values (for reference only) are equivalent to the baseline values of the "b" signals at VREF when the slew rate is 1V/ns. The baseline values "b" are the JEDEC-defined values, referenced form the logic trip points. ^{t}ISb is referenced from VIH(AC) for a rising signal and VIL(AC) for a falling signal. If the command/address slew rate is not equal to 1V/ns, then the baseline values must be derated by adding the value w from Table 26 and Table 27.

34. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^{t}WR during auto precharge.

35. READs and WRITEs with AUTO PRECHARGE are allowed to be issued before ^{t}RAS(MIN) is satisfied because the ^{t}RAS lockout feature is supported in the DDR2 SDRAM architecture.

36. When a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks open.

37. This parameter i has a two clock minimum requirement at any ^{t}CK

38. The ^{t}FAW(MIN) parameter applies to all 8-bank DDR2 devices. No more than 4-bank ACTIVATE commands may be issued in a given ^{t}FAW(MIN)period. ^{t}RRD(MIN) restriction still applies.

39. The minimum internal READ-to-PRECHARGE time. This is the time from which the last 4-bit prefetch begins, to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when ^{t}RTP/(2 x ^{t}CK)>1, such as frequencies faster than 533MHz, when ^{t}RTP = 7.5ns. If ^{t}RTP/(2 x ^{t}CK) ≤ 1, then equation AL + BL/2 applies. ^{t}RAS (MIN) has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.

40. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK). Each of these terms, if not already an integer, should be rounded up to the next integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR9-MR11. For example, -38 at ^{t}CK=3.75ns with ^{t}WR programmed to four clocks would have ^{t}DAL=4 + (15ns/3.75ns)clocks = 4 + (4) clocks = 8 clocks.

41. The refresh period is 64ms Industrial (-40-85°C), 32ms Extended (-40-105°C) and Mil-Temp (-55-125°C). This equates to a refresh rate of 7.8µs Industrial, 3.9µs Extended and 3.9µs Mil-Temp. To ensure all rows of all banks are properly refreshed, 8192 commands must be issued every 64 or 32ms. The JEDEC ^{t}RFC MAX of 70000ns is not required as bursting of AUTO REFRESH commands is allowed.

42. ^{t}DELAY is calculated from ^{t}IS +^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to ^{t}CK, CK\ being removed in a system RESET condition (see RESET).

43. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during SELF REFRESH exit.

44. ^{t}CKE(MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 x ^{t}CK + ^{t}IH.

45. The half-clock of tAOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of the half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5-0.03, or 2.47, for ^{t}AOF(MIN) and 2.5 +0.03, or 2.53, for ^{t}AOF(MAX).

46. ODT turn-on time, ^{t}AON(MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON(MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.

47. ODT turn-off time ^{t}AOF(MIN) is when the device starts to turn off ODT resistance. ODT turn-off time ^{t}AOF(MAX) is when the bus is in HIGH-Z. Both are measured from ^{t}AOFD.

48. Half-Clock output parameters must be derated by the actual tERR5per and ^{t}JITDTY when input clock jitter is present; this will result in each parameter becoming larger. The parameter ^{t}AOF(MIN) is required to be derated by subtracting both tERR5per (MAX) and ^{t}ERR5per (MIN) and ^{t}JITDTY(MIN).

Table 11: ODT Electrical Characteristics

Parameter/Condition	Symbol	MIN	TYP	MAX	UNITS	NOTES
RTT effective impedance value for 75 Ω setting EMR (A6, A2) = 0,1	RTT (eff)	60	75	90	Ω	1,2
RTT effective impedance value for 150 Ω setting EMR (A6, A2) = 1,0	RTT (eff)	120	150	180	Ω	1,2
RTT effective impedance value for 50 Ω setting EMR (A6, A2) = 1, 1	RTT (eff)	40	50	60	Ω	1,2
Deviation of VM with respect to VDDQ/2	ΔVM	-6	-	6	%	3

NOTES:

1. RTT(eff) and RTT2(eff) are determined by separately applying VIH(AC) and VIL(DC) to the ball being tested, and then measuring current, I(VIH)[AC]), and I(VIL)[AC]), respectively.
2. Minimum I(industrial), E(extended) and M(Mil-Temp) are derated by six percent when the devices operate between -40°C and 0°C and 10 percent when the devices operated between -55°C and 0°C
3. Measure voltage (VM) at tested ball with no load:

$$\Delta VM = \left[\frac{2 \times VM}{VDDQ} - 1 \right] \times 100$$

Table 12: Input DC Logic Levels

Parameter/Condition	Symbol	MIN	MAX	UNITS	
Input HIGH (logic 1) voltage	VIH (DC)	VREF (DC) + 125	VDDQ	mV	
Input LOW (logic 0) voltage	VIH (DC)	-300	VREF (DC) - 125	mV	

NOTES: VDDQ + 300mv allowed provided 1.9V is not exceeded

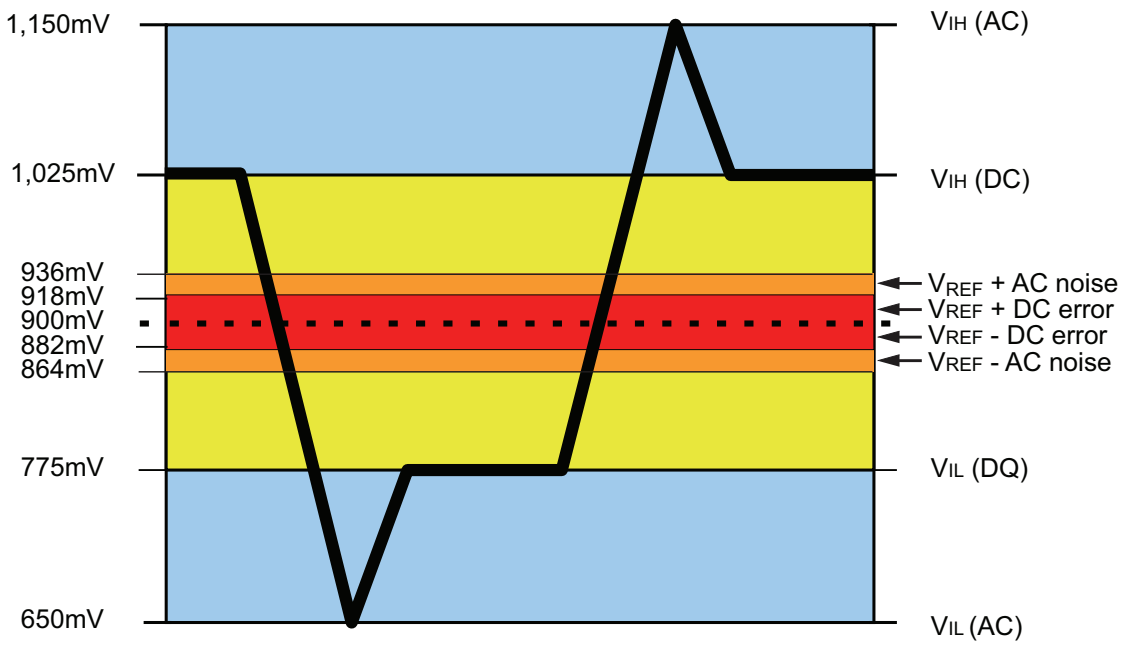
Table 13: Input AC Logic Levels

Parameter/Condition	Symbol	MIN	MAX	UNITS	
Input HIGH (logic 1) voltage (5/38)	VIH (AC)	VREF (DC) + 250	VDDQ	mV	
Input HIGH (logic 1) voltage (3/25)	VIH (AC)	VREF (DC) + 250	VDDQ	mV	
Input LOW (logic 0) voltage (5/38)	VIL(AC)	-300	VREF (DC) - 250	mV	
Input LOW (logic 0) voltage (3/25)	VIL (AC)	-300	VREF (DC) - 250	mV	

NOTES: VDDQ + 300mv allowed provided 1.9V is not exceeded

OPERATING CONDITIONS

Figure 6 - Single Ended Input Signal Levels



Note: 1. Numbers in diagram reflect nominal DDR2-400/DDR2-533 values.

Table 14: Differential Input Logic Level

Parameter/Condition	Symbol	MIN	MAX	UNITS	NOTES
DC input signal Voltage	V_{IN} (DC)	-300	$V_{DD}Q$	mV	1,6
DC differential input Voltage	V_{ID} (DC)	250	$V_{DD}Q$	mV	2,6
AC differential input Voltage	V_{ID} (AC)	500	$V_{DD}Q$	mV	3,6
AC differential cross-point Voltage	V_{IX} (AC)	0.5 x $V_{DD}Q$ - 175	0.5 x $V_{DD}Q$ + 175	mV	4
Input midpoint Voltage	V_{MP} (DC)	850	950	mV	5

NOTES:

1. V_{IN}(DC) specifies the allowable DC execution of each input of differential pair such as CKx, CKx\, DQSx, DQSx\.

2. V_{ID}(DC) specifies the input differential voltage [VTR-VCP] required for switching, where input (such as CKx\, DQSx, DQSx\) level. The minimum value is equal to V_{IH}(DC) - V_{IL}(DC). Differential input signal levels are show in Figure 16.

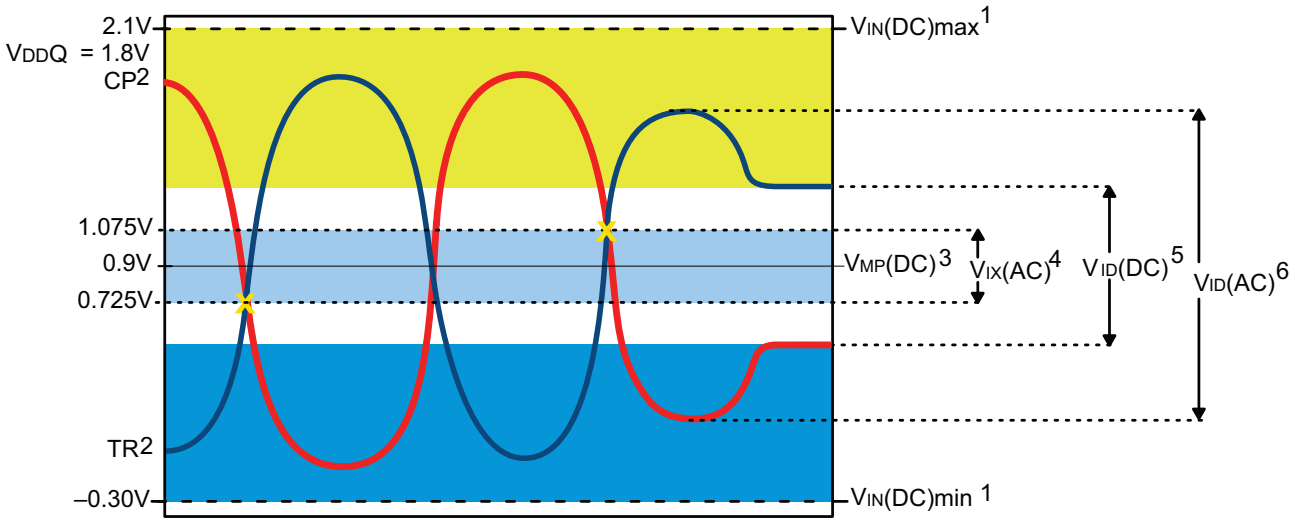
3. V_{ID}(AC) specifies the input differential voltage [VTR-VCP] required for switching, where VTR is the true input (such as CKx, DQSx, level. The minimum value is equal to V_{IH}(DC) is equal to V_{IH}(AC)-V_{IL}(AC), as shown in Table 9.

4. The typical value of V_{IX}(AC) is expected to be about 0.5 x $V_{DD}Q$ of the transmitting device and V_{IX}(AC) is expected to track variations in $V_{DD}Q$. V_{IX}(AC) indicates the voltage at which differential input signals must cross, as shown in Figure 18.

5. V_{MP}(DC) specifies the input differential common mode voltage (VTR-VCP)/2 where VTR is the true input (CKx, DQSx) level and VCP is the complementary input (CKx\, DQSx\)

6. $V_{DD}Q$ + 300mv allowed provided 1.9V is not exceeded.

Figure 7 - Differential Input Signal Levels



Notes:

1. TR and CP may not be more positive than VDDQ + 0.3 V or more negative than VXX - 0.3V.
2. TR represents the CK, DQS; CPrepresents CK#, DQS# and RDQS# signals.
3. This provides a minimum of 850mV to a maximum of 950mV and is expected to be VDDQ/2.
4. TR and CP must cross in this region.
5. TR and CP must meet at least VID(DC)min when static and is centered around VMP(DC).
6. TR and CP must have a minimum 500mV peak-to-peak swing.
7. Numbers in diagram reflect nominal values (VDDQ = 1.8V).

Table 15: Differential AC Output Parameters

Parameter	Symbol	MIN	MAX	UNITS	NOTES
AC differential cross-point Voltage	V_{OX} (AC)	0.50 x $V_{DD}Q$ - 125	0.50 x $V_{DD}Q$ + 125	mV	1,6
AC differential Voltage swing	V_{swing}	1	-	mV	

NOTES:

1. The typical value of V_{OX}(AC) is expected to be about 0.5 x $V_{DD}Q$ of the transmitting device and V_{OX}(AC) is expected to track variations in $V_{DD}Q$. V_{OX}(AC) indicates the voltage at which differential output signals must cross.

Figure 8 - Differential Output Signal Levels

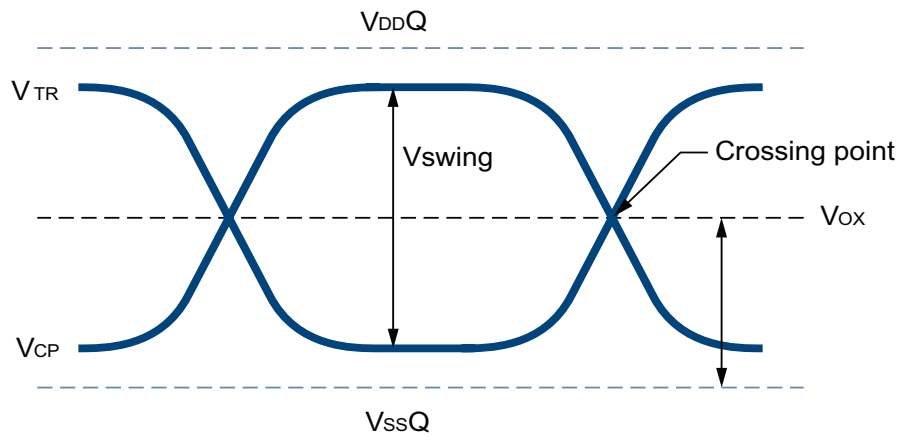


Table 16: Output DC Current Drive

Parameter/Condition	Symbol	VALUE	UNITS	NOTES
Output MIN source DC current	I_{OH}	-13.4	V_{DD} (DC)	mV
Output MIN sink DC current	I_{OL}	13.4	V_{REF} (DC) - 125	mV

NOTES:

1. For I_{OH}(DC); $V_{DD}Q$ = 1.7V, V_{OUT}= 1,420mV, (V_{OUT} - $V_{DD}Q$/I_{OH}must be less than 21Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$-280mV.
2. For I_{OL}(DC); $V_{DD}Q$ = 1.7V, V_{OUT}= 280mV, Vout/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}
4. The values of I_{OH}(DC) and I_{OL}(DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH}(MIN) plus a noise margin and V_{IL}(MAX) minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

Table 17: Output Characteristics

Parameter	MIN	TYP	MAX	UNITS	NOTES
Output Impedance	See Output Driver Characteristics			Ω	1,2
Pull-up and pull-down mismatch	0	-	4	Ω	1,2,3
Output slew rate	1.5	-	5	V/ns	1,4,5,6

NOTES:

1. Absolute specifications: 0°C ≤ TC ≤ +85°C; VDDQ = + 1.8V, VDD = +1.8V ± 0.1V
2. Impedance measurement conditions for output source DC current: VDDQ = 1.7V; out = 1,420mV; (VOUT - VDDQ)/lOH must be less than 23.4Ω for values of Vout between VDDQ and VDDQ - 280mV. The impedance measurement condition for output sink DC current: VDDQ = 1.7V; Vout = 280mV; Vout/lol must be less than 23.4Ω for values of VOUT between 0V and 280mV
3. Mismatch is and absolute value between pull-up and pull-down; both are measured at the same temperature and voltage
4. Output slew rate for falling and rising edges is measured between VTT - 250mV and VTT + 250mV for single-ended signals. For differential signals (DQSx, DQSx\), output slew rate is measured between DQSx - DQSx\ = +500mV. Output slew rate is guaranteed by design but is not necessarily tested on each device
5. The absolute value of the slew rate as measured from VIL(DC) MAX to VIH(DC) MIN is equal to or greater than the slew rate as measured from VIL(AC) MAX to VIH(AC) MIN. This is guaranteed by design.
6. All devices, INDUSTRIAL, EXTENDED and MIL-TEMP devices require an additional 0.4V/ns in the MAX limit when Tc is between -55°C and 0°C

Figure 9 - Output Slew Rate Load

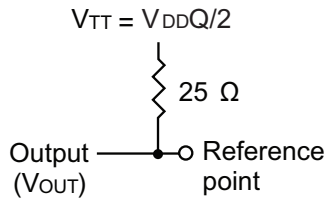


Figure 10 - Full Strength Pull Down Characteristics

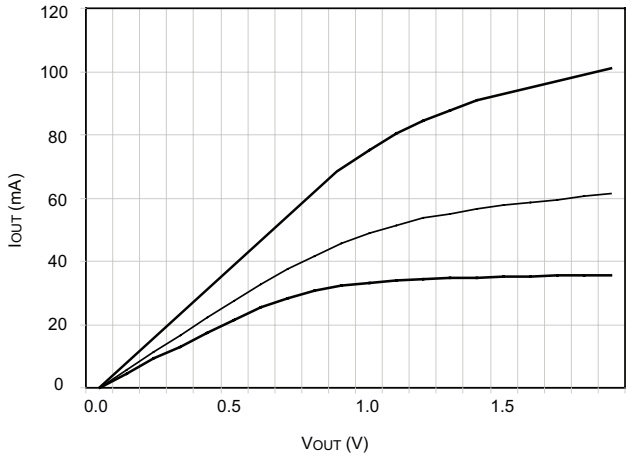


Table 18: Full Strength Pull-Down Current (mA)

Voltage (V)	MIN	TYP	MAX	UNITS	
0.0	0.00	0.00	0.00	mA	
0.1	4.30	5.63	7.95	mA	
0.2	8.60	11.30	15.90	mA	
0.3	12.90	16.52	23.85	mA	
0.4	16.90	22.19	31.80	mA	
0.5	20.40	27.59	39.75	mA	
0.6	23.28	32.39	47.70	mA	
0.7	25.44	36.45	55.55	mA	
0.8	26.79	40.38	62.95	mA	
0.9	27.67	44.01	69.55	mA	
1.0	28.38	47.01	75.35	mA	
1.1	28.96	49.63	80.35	mA	
1.2	29.46	51.71	84.55	mA	
1.3	29.90	53.32	87.95	mA	
1.4	30.29	54.90	90.70	mA	
1.5	30.65	56.03	93.00	mA	
1.6	30.98	57.07	95.05	mA	
1.7	31.31	58.16	97.05	mA	
1.8	31.64	59.27	99.05	mA	
1.9	31.96	60.35	101.05	mA	

Figure 11 - Full Strength Pull Up Characteristics

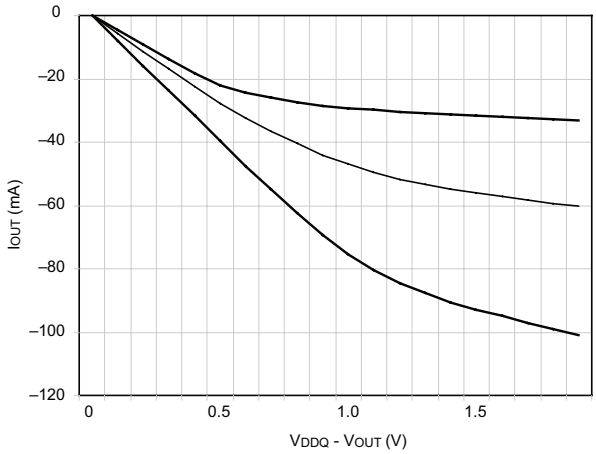


Table 19: Full Strength Pull-Up Current (mA)

Voltage (V)	MIN	TYP	MAX	UNITS
0.0	0.00	0.00	0.00	mA
0.1	-4.30	5.63	-7.95	mA
0.2	-8.60	-11.30	-15.90	mA
0.3	-12.90	-16.52	-23.85	mA
0.4	-16.90	-22.19	-31.80	mA
0.5	-20.40	-27.59	-39.75	mA
0.6	-23.28	-32.39	-47.70	mA
0.7	-25.44	-36.45	-55.55	mA
0.8	-26.79	-40.38	-62.95	mA
0.9	-27.67	-44.01	-69.55	mA
1.0	-28.38	-47.01	-75.35	mA
1.1	-28.96	-49.63	-80.35	mA
1.2	-29.46	-51.71	-84.55	mA
1.3	-29.90	-53.32	-87.95	mA
1.4	-30.29	-54.90	-90.70	mA
1.5	-30.65	-56.03	-93.00	mA
1.6	-30.98	-57.07	-95.05	mA
1.7	-31.31	-58.16	-97.05	mA
1.8	-31.64	-59.27	-99.05	mA
1.9	-31.96	-60.35	-101.05	mA

Figure 12 - Reduced Strength Pull Down Characteristics

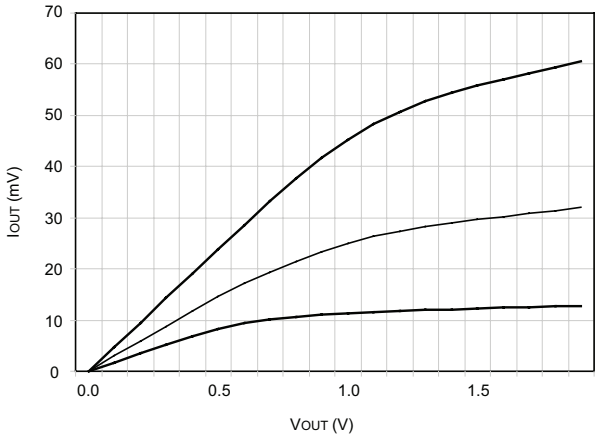


Table 20: Reduced Strength Pull-Down Current (mA)

Voltage (V)	MIN	TYP	MAX	UNITS	
0.0	0.00	0.00	0.00	mA	
0.1	1.72	2.98	4.77	mA	
0.2	3.44	5.99	9.54	mA	
0.3	5.16	8.75	14.31	mA	
0.4	6.76	11.76	19.08	mA	
0.5	8.16	14.62	23.85	mA	
0.6	9.31	17.17	28.62	mA	
0.7	10.18	19.32	33.33	mA	
0.8	10.72	21.40	37.77	mA	
0.9	11.07	23.23	41.73	mA	
1.0	11.35	24.92	45.21	mA	
1.1	11.58	26.30	48.21	mA	
1.2	11.78	27.41	50.73	mA	
1.3	11.96	28.26	52.77	mA	
1.4	12.12	29.10	54.42	mA	
1.5	12.26	29.70	55.80	mA	
1.6	12.39	30.25	57.03	mA	
1.7	12.52	30.82	28.23	mA	
1.8	12.66	31.41	59.43	mA	
1.9	12.78	31.98	60.63	mA	

Figure 13 - Reduced Strength Pull Up Characteristics

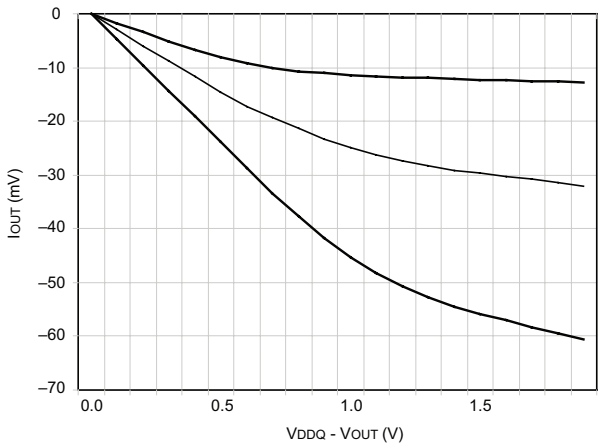


Table 21: Reduced Strength Pull-Up Current (mA)

Voltage (V)	MIN	TYP	MAX	UNITS	
0.0	0.00	0.00	0.00	mA	
0.1	-1.72	-2.98	-4.77	mA	
0.2	-3.44	-5.99	-9.54	mA	
0.3	-5.16	-8.75	-14.31	mA	
0.4	-6.76	-11.76	-19.08	mA	
0.5	-8.16	-14.62	-23.85	mA	
0.6	-9.31	-17.17	-28.62	mA	
0.7	-10.18	-19.32	-33.33	mA	
0.8	-10.72	-21.40	-37.77	mA	
0.9	-11.07	-23.23	-41.73	mA	
1.0	-11.35	-24.92	-45.21	mA	
1.1	-11.58	-26.30	-48.21	mA	
1.2	-11.78	-27.41	-50.73	mA	
1.3	-11.96	-28.26	-52.77	mA	
1.4	-12.12	-29.10	-54.42	mA	
1.5	-12.26	-29.70	-55.80	mA	
1.6	-12.39	-30.25	-57.03	mA	
1.7	-12.52	-30.82	-58.23	mA	
1.8	-12.66	-31.41	-59.43	mA	
1.9	-12.78	-31.98	-60.63	mA	

Table 22: Input Clamp Characteristics

Voltage (V) Across Clamp	MIN Power Clamp Current	MIN Ground Clamp Current	UNITS
0.0	0.00	0.00	mA
0.1	0.00	0.00	mA
0.2	0.00	0.00	mA
0.3	0.00	0.00	mA
0.4	0.00	0.00	mA
0.5	0.00	0.00	mA
0.6	0.00	0.00	mA
0.7	0.00	0.00	mA
0.8	0.10	0.10	mA
0.9	1.00	1.00	mA
1.0	2.50	2.50	mA
1.1	4.70	4.70	mA
1.2	6.80	6.80	mA
1.3	9.10	9.10	mA
1.4	11.00	11.00	mA
1.5	13.50	13.50	mA
1.6	16.00	16.00	mA
1.7	18.20	18.20	mA
1.8	21.00	21.00	mA

Figure 14 - Input Clamp Characteristics

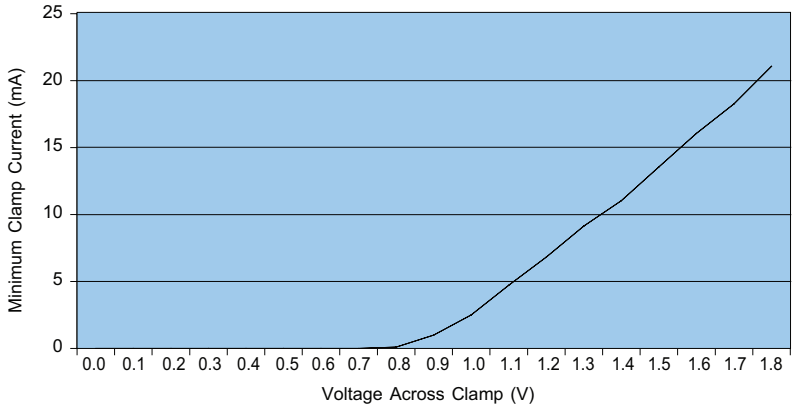


Table 23: Address and Controls Pins

Parameter	25	SPECIFICATIONS 3	37	5	UNITS
Maximum peak amplitude for overshoot area (see Figure 15)	0.50	0.50	0.50	0.50	V
Maximum peak amplitude allowed for undershoot area (see Figure 16)	0.50	0.50	0.50	0.50	V
Maximum overshoot area above V_{DD} (see Figure 15)	0.66	0.80	1.00	1.33	V/ns
Maximum undershoot area below V_{ss} (see Figure 16)	0.66	0.80	1.00	1.33	V/ns

Table 24: Clock, Data, Strobe, and Mask Pins

Parameter	25	SPECIFICATIONS 3	37	5	UNITS
Maximum peak amplitude for overshoot area (see Figure 15)	0.50	0.50	0.50	0.50	V
Maximum peak amplitude allowed for undershoot area (see Figure 16)	0.50	0.50	0.50	0.50	V
Maximum overshoot area above $V_{DD}Q$ (see Figure 15)	0.23	0.23	0.28	0.38	V/ns
Maximum undershoot area below $V_{ss}Q$ (see Figure 16)	0.23	0.23	0.28	0.38	V/ns

Figure 15 & 16: Overshoot/Undershoot Specifications

Figure 15: Overshoot

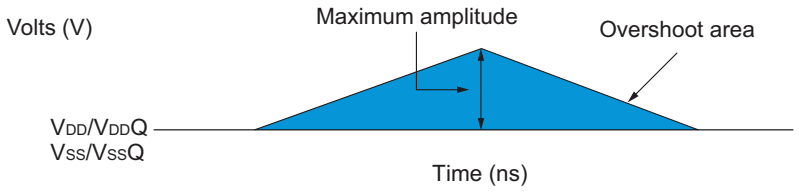


Figure 16: Undershoot

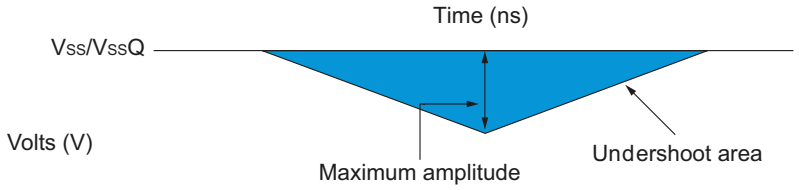


Table 25: AC Input Test Conditions

Parameter/Condition	Symbol	MIN	MAX	UNITS	NOTES
Input setup timing measurement reference level address balls bank address balls, CS\, RAS\, CAS\, WE\, ODT, DM, UDM, LDM, and CKE	V_{RS}	See Note 2			1,2,3,4
Input hold timing measurement reference level address balls bank address balls, CS\, RAS\, CAS\, WE\, ODT, DM, UDM, LDM, and CKE	V_{RH}	See Note 5			1,3,4,5
Input timing measurement reference level (single-ended) UDQSx, LDQSx	V_{REF}(DC)	V_{DD}Q x 0.49	V_{DD}Q x 0.51	V	1 3,4,6
Input timing measurement reference level (differential) CK, CK\, UDQSx, UDQSx\, LDQSx, LDQSx\	V_{RD}	V_{IX}(AC)		V	1,3,7,8,9

NOTES:

1. All voltages referenced to Vss
2. Input waveform setup timing (^{t}ISb) is referenced from the input signal crossing at the V_{IH}(AC) level for a rising signal and V_{IL}(AC) for a falling signal applied to the device under test, as shown in Figure 36.
3. See Input Slew Rate Derating
4. The slew rate for single-ended inputs is measured from DC level to AC level, V_{IL}(DC) to V_{IH}(AC) on the rising edge and V_{IL}(AC) to V_{IH}(DC) on the falling edge. For signals referenced to V_{REF}, the valid intersection is where the "tangent" line intersects V_{REF}, as shown in Figure 29, 31, 33 and 35.
5. Input waveform hold (^{t}IHb) timing is referenced from the input signal crossing at the V_{IL}(DC)level for a rising signal and V_{IH}(DC) for a falling signal applied to the device under test, as shown in Figure 36.
6. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when single-ended data strobe is enabled is referenced from the crossing of DQS, DQS\, or through the V_{REF} level applied to the device under test, as shown in Figure 38.
7. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when differential data strobe is enabled is referenced from the cross-point of DQSxDQSx\, as shown in Figure 37.
8. Input waveform timing is referenced to the crossing point level (Vix) of two input signals (Vtr and Vcp) applied to the device under test, where Vtr is the true input signal and Vcp is the complementary input signal, as shown in Figure 39.
9. The slew rate for differentially ended inputs is measured from twice the DC level to twice the AC level: 2 x V_{IL}(DC) to 2 x V_{IH}(AC) on the falling edge, for example, the CK/CK\ would be -250mV to +500mV for CK rising edge and would be +250mV to -500mV for CK falling edge.

Input Slew Rate Derating

For all input signals, the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the datasheet ^{t}IS (base) and ^{t}IH (base) value to the Δ^{t}IS and Δ^{t}IH derating value, respectively. Set-up and hold times are based on measurements at the device. Note that address and control pins present the capacitance of multiple die to the system. This capacitance is less than the equivalent number of discrete devices due to the higher level of die integration; however, it must be accounted for when driving these pins. Slew rates on these pins will be slower than pins with only one die load unless measures are made to increase the strength of the signal driver and lower the trace impedance proportionally on signals connecting to multiple internal die.

^{t}IS, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. Setup nominal slew rate (^{t}IS) for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX.

If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC) to AC region, " use the nominal slew rate for the derating value. If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC) to AC region", the slew rate of a tangent line to the actual signal from the AC level to DC level is used for the derating value.

^{t}IH, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). ^{t}IH, nominal slew rate for a falling signal, is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC).

If the actual signal is always later than the nominal slew rate line between shaded "DC to VREF(DC) region," use the nominal slew rate for the derating value.

If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region, " the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value.

Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached VIH[AC]/VIL[AC] at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC).

For slew rates in between the values listed Table 26 and Table 27, the derating values may be obtained by linear interpolation.

Table 26: DDR2-400/533 Setup and Hold Time Derating Values (^{t}IS/^{t}IH)

CMD/ADDR Slew Rate V/ns	CK, CK\ Differential Slew Rate						UNITS
	2.0V/ns		1.5V/ns		1.0V/ns		
	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	Δ^{t}IS	Δ^{t}IH	
4.00	187	94	217	124	247	154	ps
3.50	179	89	209	119	239	149	ps
3.00	167	83	197	113	227	143	ps
2.50	150	75	180	105	210	135	ps
2.00	125	45	155	75	185	105	ps
1.50	83	21	113	51	143	81	ps
1.00	0	0	30	30	60	60	ps
0.90	-11	-14	19	16	46	46	ps
0.80	-25	-31	5	-1	29	29	ps
0.70	-43	-54	-13	-24	6	6	ps
0.60	-67	-83	-37	-53	-23	-23	ps
0.50	-110	-125	-80	-95	-65	-65	ps
0.40	-175	-188	-145	-158	-128	-128	ps
0.30	-285	-292	-255	-262	-232	-232	ps
0.25	-350	-375	-320	-345	-315	-315	ps
0.20	-525	-500	-495	-470	-440	-440	ps
0.15	-800	-708	-770	-678	-648	-648	ps
0.10	-1450	-1125	-1420	-1095	-1065	-1065	ps

Table 27: DDR2-667/800 Setup and Hold Time Derating Values (t_{IS}/t_{IH})

CMD/ADDR Slew Rate V/ns	CK, CK\ Differential Slew Rate						UNITS
	2.0V/ns		1.5V/ns		1.0V/ns		
	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	
4.00	150	94	180	124	210	154	ps
3.50	143	89	173	119	203	149	ps
3.00	133	83	163	113	193	143	ps
2.50	120	75	150	105	180	135	ps
2.00	100	45	140	75	160	105	ps
1.50	67	21	97	51	127	81	ps
1.00	0	0	30	30	60	60	ps
0.90	-5	-14	25	16	55	46	ps
0.80	-13	-31	17	-1	47	29	ps
0.70	-22	-54	8	-24	38	6	ps
0.60	-34	-83	-4	-53	36	-23	ps
0.50	-60	-125	-30	-95	0	-65	ps
0.40	-100	-188	-70	-158	-40	-128	ps
0.30	-168	-292	-138	-262	-108	-232	ps
0.25	-200	-375	-170	-345	-140	-315	ps
0.20	-325	-500	-295	-470	-265	-440	ps
0.15	-517	-708	-487	-678	-457	-648	ps
0.10	-1000	-1125	-970	-1095	-940	-1065	ps

Figure 17 - Nominal Slew Rate for tIS

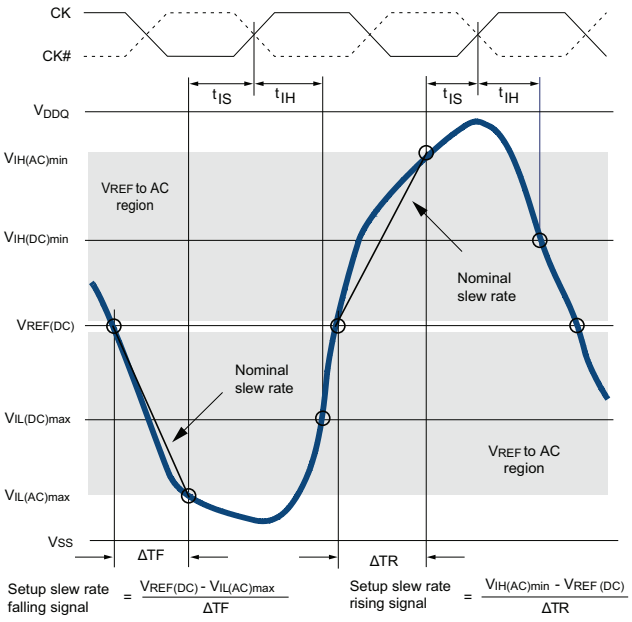


Figure 18 - Tangent Line for tIS

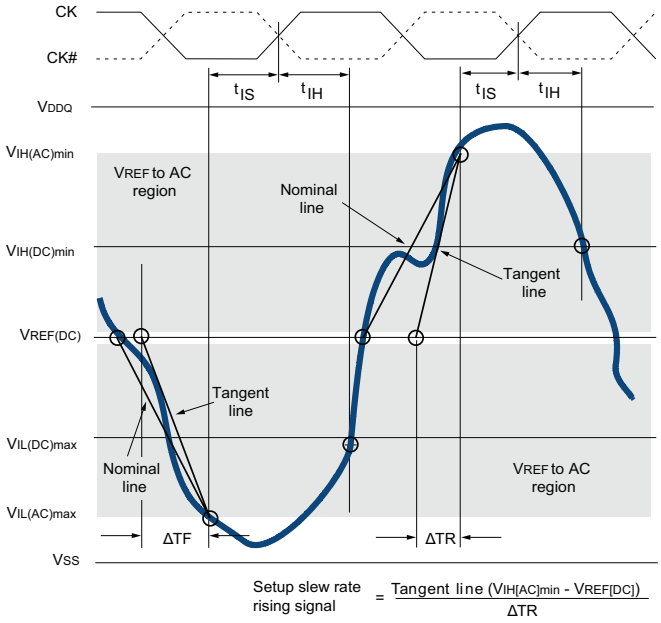


Figure 19 - Nominal Slew Rate for tIH

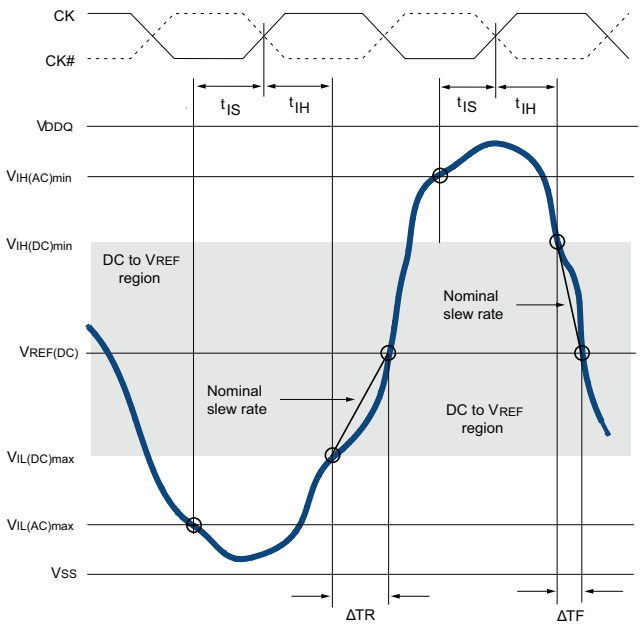
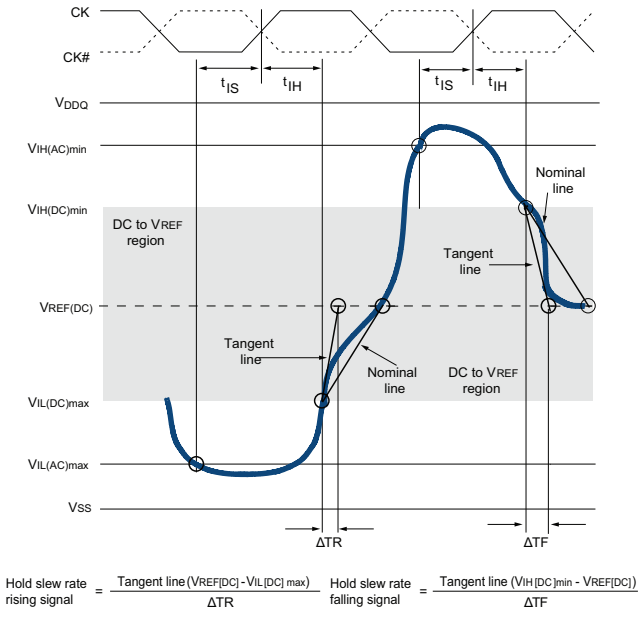


Figure 20 - Tangent Line for tIH



$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF[DC]} - V_{IL[DC]\,max})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH[DC]min} - V_{REF[DC]})}{\Delta TF}$$

Table 28 - DDR2-400/533 tDS, tDH Derating values with Differential Strobe

DQ Slew Rate V/ns	DQSx, DQSx\ Differential Slew Rate																	
	4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns			
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-	-	-
1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-	-	-
1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-	-	-
0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-	-	-
0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-	-	-
0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-	-	-
0.6					-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11		
0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53		
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116		

NOTES:

1. For all input signals, the total tDS and tDH required is calculated by adding the datasheet value to the derating value listed in the above table.

2. tDS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)MIN. tDS nominal slew rate for a first crossing of VIL(AC)MAX (Figure 32), if the actual signal is always earlier than the nominal slew rate line between the shaded "VREF(DC) to AC region", use the nominal slew rate for the derating value. If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC) to AC region", the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (Figure 33).

3. tDH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). tDH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC level to VREF(DC) region", use the nominal slew rate for derating value (Figure 34). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region", the rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value (see Figure 35).

4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached VIH[AC])/VIL[AC] at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC).

5. For slew rates between the values listed in this table, the derating values may be obtained via linear interpolation.

6. These values are typically not subject to production test. They are verified by design and characterization.

7. Single-ended DQSx requires special derating. The values in Table 26 are the DQS single-ended slew rate derating with DQS referenced at VREF and DQ referenced at the logic levels tDSb and tDHb. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to VREF is listed in Table 28 and 29. Table 28 provides the VREF-based fully derated values for the DQ (tDSa and tDHa) for DDR2-533. Table 29 provides the VREF-based fully derated values for the DQ (tDSa and tDHa) for DDR2-400.

Table 29 - DDR2 tDS, tDH Derating values with Differential Strobe

DQ Slew Rate V/ns	DQSx, DQSx\ Differential Slew Rate																	
	4.0V/ns		3.0V/ns		2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22	43	34	55	46	67	58
0.8	-13	-31	-13	-31	-13	-31	-1	-19	11	-7	23	5	35	17	47	29	59	41
0.7	-22	-54	-22	-54	-22	-54	-10	-42	2	-30	14	-18	26	-6	38	6	50	18
0.6	-34	-83	-34	-83	-34	-83	-22	-71	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-60	-125	-60	-125	-60	-125	-48	-113	-36	-101	-24	-89	-12	-77	0	-65	12	-53
0.4	-100	-188	-100	-188	-100	-188	-88	-176	-76	-164	-64	-152	-52	-140	-40	-128	-28	-116

NOTES:

1. For all input signals, the total tDS and tDH required is calculated by adding the datasheet value to the derating value listed in the above table

2. tDS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)MIN. tDS nominal slew rate for a first crossing of VIL(AC)MAX (Figure 32), if the actual signal is always earlier than the nominal slew rate line between the shaded "VREF(DC) to AC region", use the nominal slew rate for the derating value. If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC) to AC region", the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (Figure 33).

3. tDH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). tDH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC level to VREF(DC) region", use the nominal slew rate for derating value (Figure 34). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region", the rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value (see Figure 35).

4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached VIH[AC])/VIL[AC] at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC).

5. For slew rates between the values listed in this table, the derating values may be obtained via linear interpolation.

6. These values are typically not subject to production test. They are verified by design and characterization.

7. Single-ended DQS requires special derating. The values in Table 26 are the DQS single-ended slew rate derating with DQS referenced at VREF and DQ referenced at the logic levels tDSb and tDHb. Converting the derated base values from DQ referenced to the AC/DC trip points to DQ referenced to VREF is listed in Table 26. Table 26 provides the VREF-based fully derated values for the DQ (tDSa and tDHa) for DDR2-667. It is not advised to operate DDR2-800 devices with single-ended DQS; however, Table 26 would be used with the base values.

Table 30 - Single-Ended DQS Slew Rate Derating Values Using tDSb, tDHb

DQ Slew Rate V/ns	DQSx Single-Ended Slew Rate Derated (at VREF)																	
	2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns		0.6V/ns		0.4V/ns			
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	130	53	130	53	130	53	130	53	130	53	145	48	155	45	160	123	172	135
1.5	97	32	97	32	97	32	97	32	97	32	112	27	122	24	127	102	139	114
1.0	30	-10	30	-10	30	-10	30	-10	30	-10	45	-15	55	-18	60	60	72	72
0.9	25	-24	25	-24	25	-24	25	-24	25	-24	40	-29	50	-32	55	46	67	58
0.8	17	-41	17	-41	17	-41	17	-41	17	-41	32	-46	42	-49	47	29	59	41
0.7	5	-64	5	-64	5	-64	5	-64	5	-64	20	-69	30	-72	38	6	50	18
0.6	-7	-93	-7	-93	-7	-93	-7	-93	-7	-93	8	-98	18	-102	26	-23	38	-11
0.5	-28	-135	-28	-135	-28	-135	-28	-135	-28	-135	-13	-140	-3	-143	0	-65	12	-53
0.4	-78	-198	-78	-198	-78	-198	-78	-198	-78	-198	-63	-203	-53	-206	-40	-128	-28	-116

Table 31 - Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at DDR2-667

DQ Slew Rate V/ns	DQSx Single-Ended Slew Rate Derated (at VREF)																	
	2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns		0.6V/ns		0.4V/ns			
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	330	291	330	291	330	291	330	291	330	291	345	286	355	282	365	279	375	276
1.5	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	279	375	275
1.0	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	278	375	275
0.9	347	290	347	290	347	290	347	290	347	290	362	285	372	282	382	278	392	275
0.8	367	290	367	290	367	290	367	290	367	290	382	285	392	282	402	278	412	275
0.7	391	290	391	290	391	290	391	290	391	290	406	285	416	281	426	278	436	275
0.6	426	290	426	290	426	290	426	290	426	290	441	285	451	282	461	278	471	275
0.5	472	290	472	290	472	290	472	290	472	290	487	285	497	282	507	278	517	275
0.4	522	289	522	289	522	289	522	289	522	289	537	284	547	281	557	278	567	274

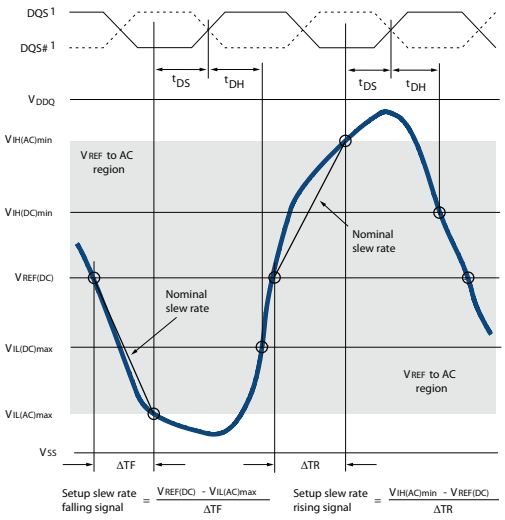
Table 32 - Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at VREF) at DDR2-533

DQ Slew Rate V/ns	DQSx Single-Ended Slew Rate Derated (at VREF)																	
	2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns		0.6V/ns		0.4V/ns			
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
2.0	355	341	355	341	355	341	355	341	355	341	370	336	380	332	390	329	400	326
1.5	364	340	364	340	364	340	364	340	364	340	379	335	389	332	399	329	409	325
1.0	380	340	380	340	380	340	380	340	380	340	395	335	405	332	415	328	425	325
0.9	402	340	402	340	402	340	402	340	402	340	417	335	427	332	437	328	447	325
0.8	429	340	429	340	429	340	429	340	429	340	444	335	454	332	464	328	474	325
0.7	463	340	463	340	463	340	463	340	463	340	478	335	488	331	498	328	508	325
0.6	510	340	510	340	510	340	510	340	510	340	525	335	535	332	545	328	555	325
0.5	572	340	572	340	572	340	572	340	572	340	587	335	597	332	607	328	617	325
0.4	647	339	647	339	647	339	647	339	647	339	662	334	672	331	682	328	692	324

Table 33 - Single-Ended DQS Slew Rate Fully Derated (DQS, DQ at Vref) at DDR2-400

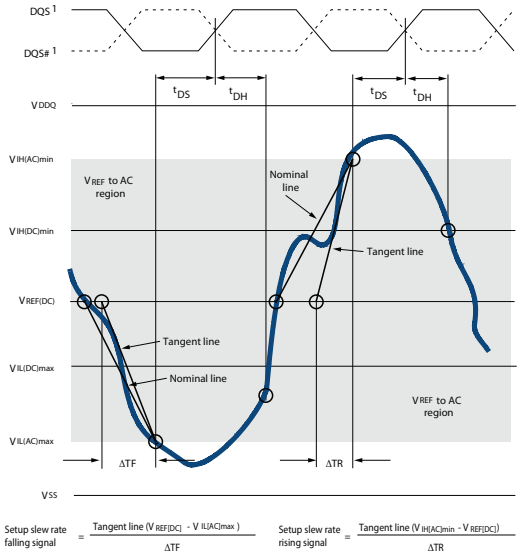
DQ Slew Rate V/ns	DQSx Single-Ended Slew Rate Derated (at VREF)																	
	2.0V/ns		1.8V/ns		1.6V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns		0.6V/ns		0.4V/ns	
	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH	Δ^tDS	Δ^tDH
2.0	405	391	405	391	405	391	405	391	405	391	420	386	430	382	440	379	450	376
1.5	414	390	414	390	414	390	414	390	414	390	429	385	439	382	449	379	459	375
1.0	430	390	430	390	430	390	430	390	430	390	445	385	455	382	465	378	475	375
0.9	452	390	452	390	452	390	452	390	452	390	467	385	477	382	487	378	497	375
0.8	479	390	479	390	479	390	479	390	479	390	494	385	504	382	514	378	524	375
0.7	513	390	513	390	513	390	513	390	513	390	528	385	538	381	548	378	558	375
0.6	560	390	560	390	560	390	560	390	560	390	575	385	585	382	595	378	605	375
0.5	622	390	622	390	622	390	622	390	622	390	637	385	647	382	657	378	667	375
0.4	697	389	697	389	697	389	697	389	697	389	712	384	722	381	732	378	742	374

Figure 21 - Nominal Slew Rate for tDS



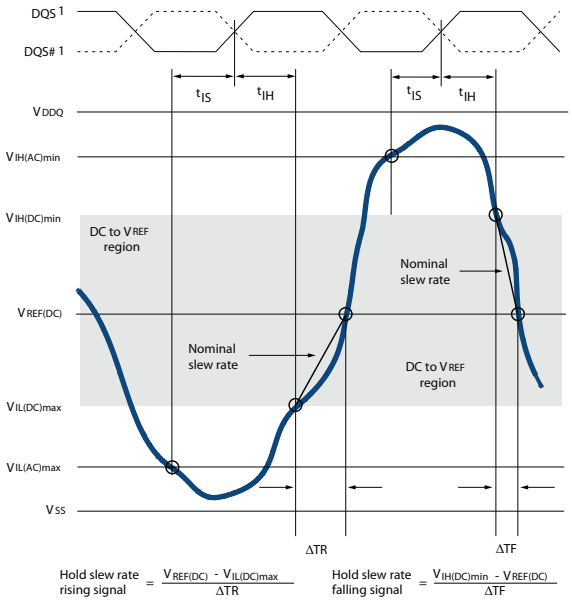
Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$

Figure 22 - Tangent Line for tDS



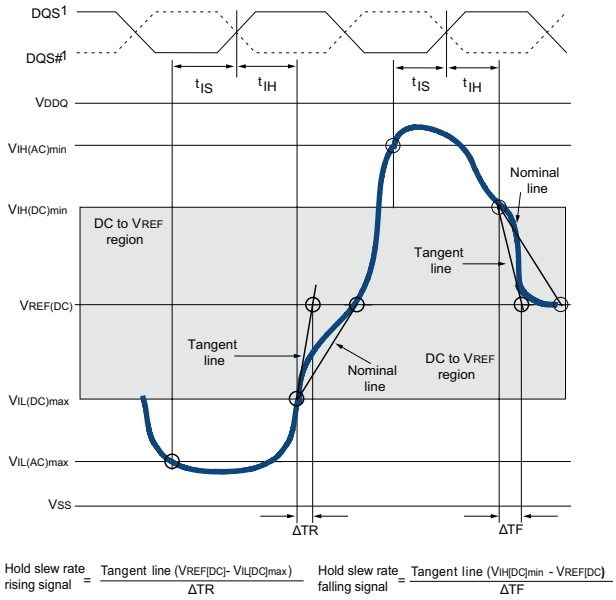
Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 23 - Nominal Slew Rate for tDH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 24 - Tangent Line for tDH



Note: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)max}$ and $V_{IH(DC)min}$.

Figure 25 - AC Input Test Signal Waveform Command/Address Balls

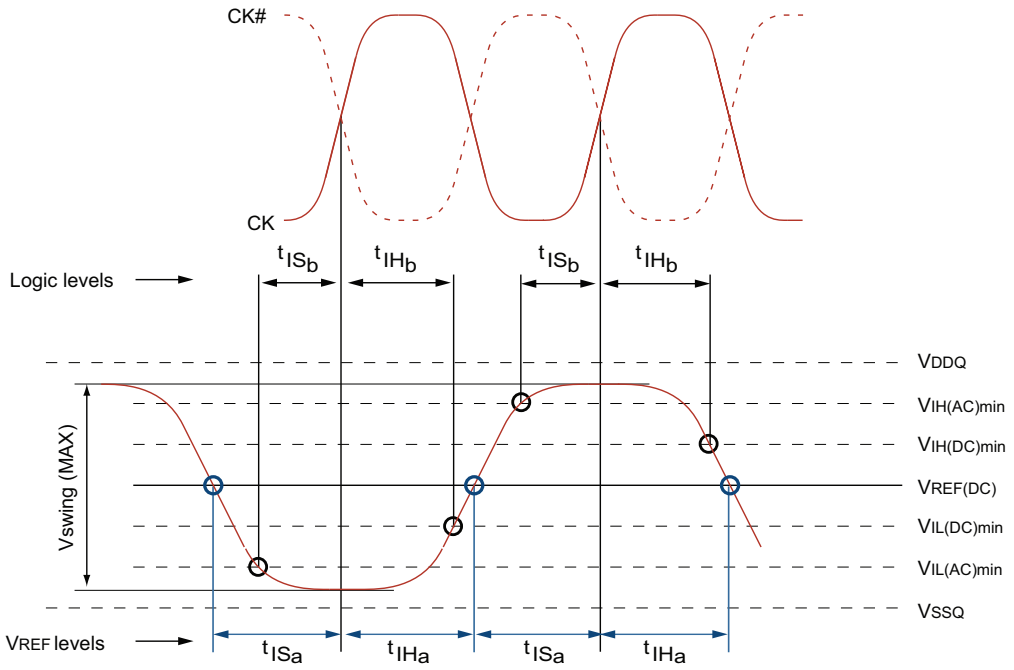


Figure 26 - AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)

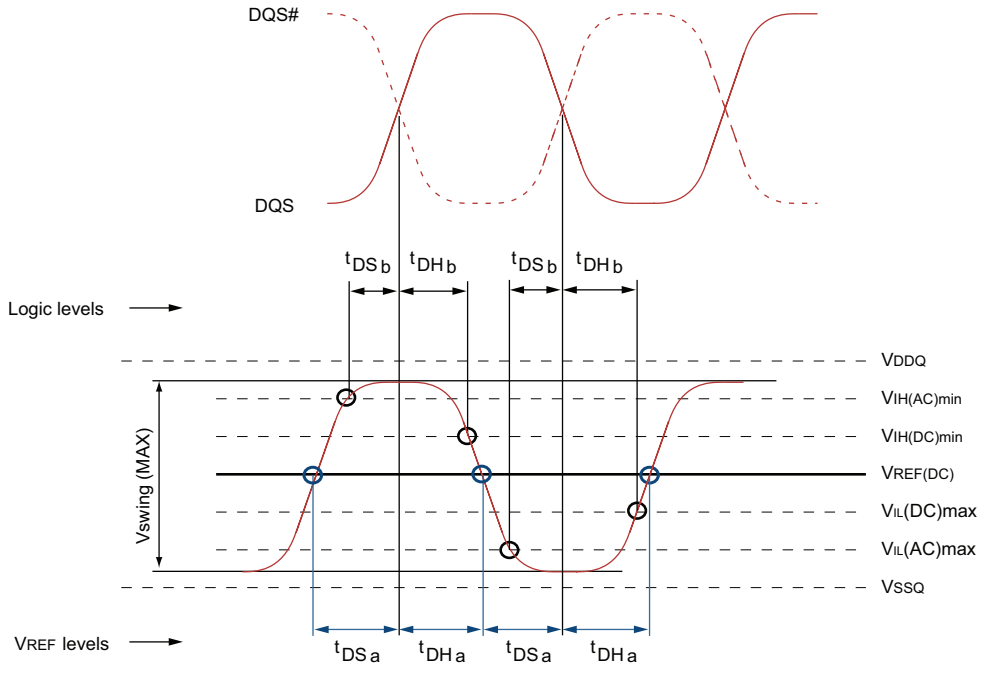


Figure 27 - AC Input Test Signal Waveform for Data with DQS (Single-Ended)

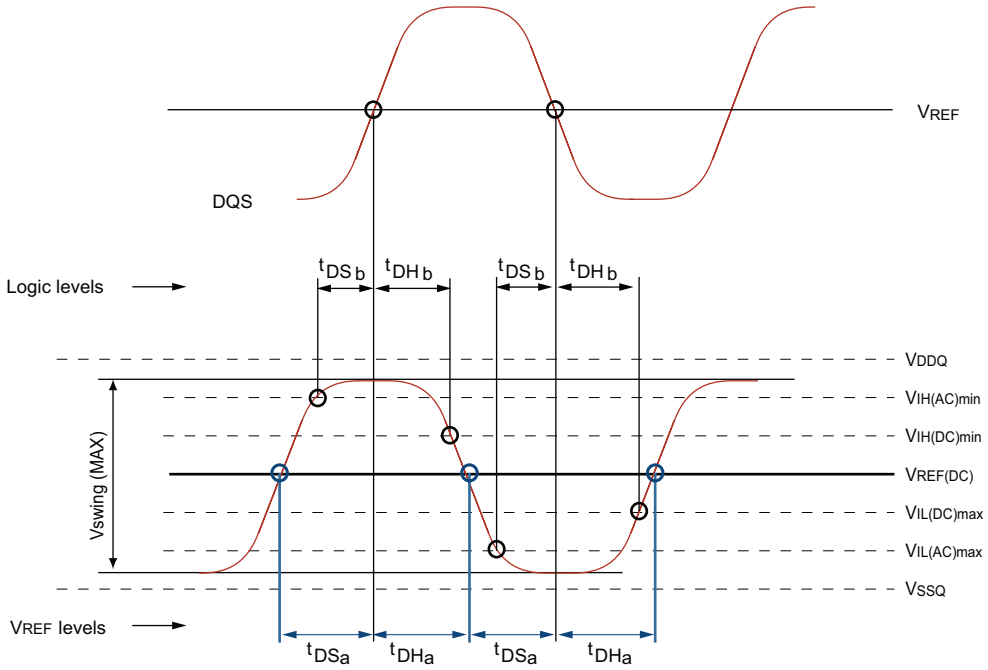
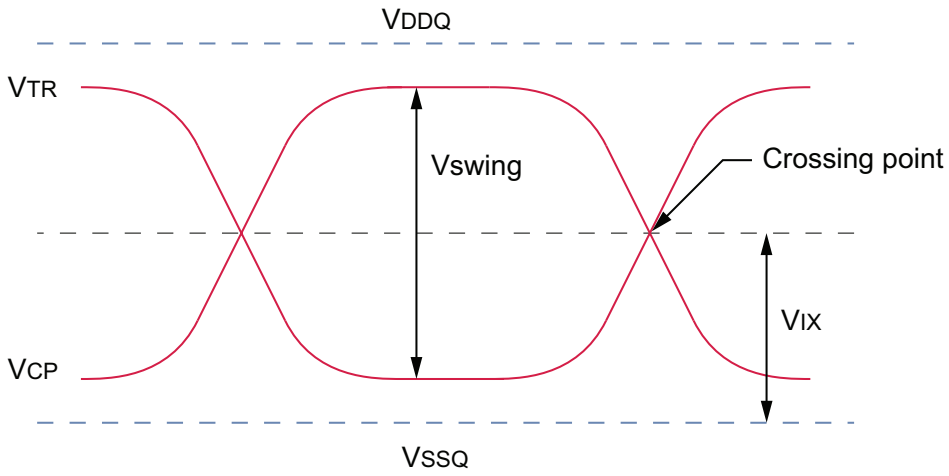


Figure 28 - AC Input Test Signal Waveform (Differential)



COMMANDS TRUTH TABLE

Table 34: Truth Table - DDR2 Commands

Function	Cycle	CKE Prev Cycle	CKE Current CS\	RAS\	CAS\	WE\	BA1-BA0	AN -A11	A10	A9-A10	Notes		
LOAD MODE		H	H	L	L	L	L	BA	OP Code				1-3,4,6
REFRESH		H	H	L	L	L	H	X	X	X		X	1-3
SELF REFRESH ENTRY		H	L	L	L	L	H	X	X	X		X	1-3,4,7
SELF REFRESH EXIT		L	H	H	X	X	X	X	X	X		X	1-3
				L	H	H	H						
PRECHARGE SINGLE BANK		H	H	L	L	H	L	BA	X	L		X	1-3,6
PRECHARGE ALL BANKS		H	H	L	L	H	L	X	X	H		X	1-3
BANK ACTIVATE		H	H	L	L	H	H	BA	ROW Address				1-4
WRITE		H	H	L	H	L	L	BA	Column Address	L		Column Address	1-6,8
WRITE with AUTO PRECHARGE		H	H	L	H	L	L	BA	Column Address	H		Column Address	1-6,8
READ		H	H	L	H	L	H	BA	Column Address	L		Column Address	1-6,8
READ with AUTO PRECHARGE		H	H	L	H	L	H	BA	Column Address	H		Column Address	1-6,8
NO OPERATION		H	X	L	H	H	H	X	X	X		X	1-3
DEVICE DESELECT		H	X	H	X	X	X	X	X	X		X	1-3
POWER-DOWN ENTRY		H	L	H	X	X	X	X	X	X		X	1-3,9
				L	H	H	H						
POWER-DOWN EXIT		L	H	H	X	X	X	X	X	X		X	1-3,9
				L	H	H	H						

NOTES:

1. All commands are defined by states of CS\, RAS\, CAS\, WE\ and CKE at the rising edge of the clock.
2. The state of ODT does not affect the states described in this table. The ODT function is not available during SELF REFRESH. See ODT timing for details.
3. "X" denotes either a "H" or 'L" (but a defined LOGIC Level) for valid IDD measurements.
4. BA0-BA1 for densities up to 2.5Gb modules, BA2 included for bank address on ≥ 4Gb modules
5. An n is the most significant address bit for a given density and configuration. Some larger address bits may be "DON'T CARE" during column addressing, depending on density and configuration.
6. Bank Addresses (BA) determines which bank is to be operated upon. BA during a LOAD MODE command selects which mode register is programmed.
7. SELF REFRESH exit is asynchronous
8. Burst READS or WRITES at BL = 4 cannot be terminated or interrupted.
9. The POWER-DOWN mode does not perform any REFRESH operations. The duration of POWER-DOWN is limited by the REFRESH requirements outlined in the AC parametric section.

Table 35: Truth Table - Current State Bank n - Command to Bank n

Current State	CS\	RAS\	CAS\	WE\	Command/Action	Notes
ANY	H	X	X	X	DESELECT (NOP/continue previous operation)	1-6
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	1-6
IDLE	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
	L	L	L	H	REFRESH	1-6,7
	L	L	L	L	LOAD MODE	1-6,7
ROW Active	L	H	L	H	READ (select COLUMN and start READ burst)	1-6,8
	L	H	L	L	WRITE (select COLUMN and start WRITE burst)	1-6,8
	L	L	H	L	PRECHARGE (deactivate ROW in bank or banks)	1-6,9
READ (Auto Precharge Disabled)	L	H	L	H	READ (select COLUMN and start READ burst)	1-6,8
	L	H	L	H	WRITE (select COLUMN and start WRITE burst)	1-6,8,10
	L	L	H	L	PRECHARGE (start PRECHARGE)	1-6,9
WRITE (Auto Precharge Disabled)	L	H	L	H	READ (select COLUMN and start READ burst)	1-6,8
	L	H	L	L	WRITE (select COLUMN and start WRITE burst)	1-6,8
	L	L	H	L	PRECHARGE (start PRECHARGE)	1-6,9

NOTES:

1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH and after ^{t}XSNR has been met (if the previous state was SELF REFRESH)

2. This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the below.

3. Current state definitions:

IDLE:	The bank has been precharged, ^{t}RP has been met and any READ burst is complete.
ROW Active	A ROW in a bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
READ	A READ burst has been initiated with auto precharge disabled and has not yet terminated.
WRITE	A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.

4. The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table and according to Table 36.

PRECHARGE	Starts with registration of a PRECHARGE command and ends when ^{t}RP is met, the bank will be in the idle state.
READ W/ AUTO PRECHARGE ENABLED	Starts with registration of a READ command with Auto Precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.
ROW Activate	Starts with registration of a WRITE command with Auto Precharge enabled and ends when ^{t}RCD is met, the bank will be in the ROW active state.
WRITE W/ AUTO Precharge enabled	Starts with registration of a WRITE command with Auto Precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following state must not be interrupted by any executable command (DESELECT or NOP commands must be applied on each positive clock edge during these states):

Notes Continued

REFRESH	Starts with registration of a REFRESH command and ends when ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.
ACCESSING MODE REGISTER	Starts with registration of a the LOAD MODE command and ends when ^{t}MRD has been met. After^{t} MRD is met, the DDR2 SDRAM will be in the all banks idle state.
PRECHARGE ALL	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and bursts are not in progress.
8. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
10. A WRITE command may be applied after the completion of the READ burst.

Table 36: Truth Table - Current State Bank n - Command to Bank m

Current State	CS\	RAS\	CAS\	WE\	Command/Action	Notes
ANY	H	X	X	X	DESELECT (NOP/continue previous operation)	1-6
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	1-6
IDLE	X	X	X	X	Any command otherwise allowed to bank m	1-6
ROW Active,	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
ACTIVE,	L	H	L	H	READ (select COLUMN and start READ burst)	1-6,7
or PRECHARGE	L	H	L	L	WRITE (select COLUMN and start WRITE burst)	1-6,7
	L	L	H	L	PRECHARGE	1-6
READ	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
(Auto Precharge	L	H	L	H	READ (select COLUMN and start new READ burst)	1-7
Disabled)	L	H	L	L	WRITE (select COLUMN and start WRITE burst)	1-8
	L	L	H	L	PRECHARGE	1-6
WRITE	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
(Auto Precharge	L	H	L	H	READ (select COLUMN and start READ burst)	1-7,9,10
Disabled)	L	H	L	L	WRITE (select COLUMN and start new WRITE burst)	1-7
	L	L	H	L	PRECHARGE	1-6
READ	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
(Auto Precharge)	L	H	L	H	READ (select COLUMN and start new READ burst)	1-7
	L	H	L	L	WRITE (select COLUMN and start WRITE burst)	1-8
	L	L	H	L	PRECHARGE	1-6
WRITE	L	L	H	H	ACTIVATE (select and activate ROW)	1-6
(Auto Precharge)	L	H	L	H	READ (select COLUMN and start READ burst)	1-7,10
	L	H	L	L	WRITE (select COLUMN and start new WRITE burst)	1-7
	L	L	H	L	PRECHARGE	1-6

Notes

1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH and after ^{t}XSNR has been met (if the previous state was SELF REFRESH)
2. This table is bank-specific, except where noted (the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the below.
3. Current state definitions:

IDLE:	The bank has been precharged, ^{t}RP has been met and any READ burst is complete.
ROW Active	A ROW in a bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
READ	A READ burst has been initiated with auto precharge disabled and has not yet terminated.
WRITE	A WRITE burst has been initiated with auto precharge disabled and has not yet terminated.
READ with AUTO PRECHARGE enabled/WRITE with AUTO PRECHARGE enabled	The READ with Auto Precharge enabled or WRITE with Auto Precharge enabled states can be broken into two parts; the access period and the Precharge period. For READ with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For WRITE with Auto Precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. This device supports concurrent Auto Precharge such that when a READ with Auto Precharge is enabled or a WRITE with Auto Precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the READ or WRITE data transfer already in process. In either case, all other related limitations apply (contention between READ data and WRITE data must be avoided).

The minimum delay from a READ or WRITE command with AUTO PRECHARGE enabled to a command to a different bank is summarized in Table 37.

4. REFRESH and LOAD MODE commands may only be issued when all banks are idle
5. Not Used
6. All states and sequences not shown are illegal or reserved
7. READs and WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled
8. A WRITE command may be applied after the completion of the READ burst.
9. Requires appropriate DM
10. The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/^{t}CK, whichever is greater.

Table 37: Minimum Delay with Auto Precharge Enabled

From Command (Bank n)	To Command (Bank m)	Minimum Delay (with Concurrent AUTO PRECHARGE)	UNITS
WRITE with AUTO PRECHARGE	READ or READ with Auto Precharge	(CL - 1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE with Auto Precharge	(BL/2)	
	PRECHARGE or ACTIVATE	1	
READ with AUTO PRECHARGE	READ OR READ WITH Auto Precharge	(BL/2)	^{t}CK
	WRITE or WRITE with Auto Precharge	(BL/2) + 2	
	PRECHARGE or ACTIVATE	1	

DESELECT

The DESELECT function (CS\ HIGH) prevents new commands from being executed. The module is effectively deselected. Operations already in progress are not affected. DESELECT is also referred to as COMMAND INHIBIT.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 device to perform a NOP (CS\ is LOW; RAS\, CAS\ and WE\ are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for subsequent row activation at a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent AUTO PRECHARGE, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. After a bank has been precharged, it is in the idle state and must be activated prior to any READ and or WRITE commands being issued to a bank (idle state) or if the previously open row is already in the process of precharging. However, the PRECHARGE period will be determined by the last PRECHARGE command issued to the bank.

ACTIVATE

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the bank address inputs determines the bank, and the address inputs select the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

LOAD MODE (LM)

The mode registers are loaded via bank address and address inputs. The bank address balls determine which mode register will be programmed. The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

READ

The READ command is used to initiate a burst READ access to an active row. The value on the bank address inputs determine the bank, and the address provided on the address inputs A_0-A_i (where A_i is the most significant column address bit for a given configuration) selects the starting column location. The value on input A10 determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. The module also support the AL feature, which allows a READ or WRITE command to be issued prior to ^{t}RCD(MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

WRITE

The WRITE command is used to initiate a burst WRITE access to an active row. The value on the bank select inputs selects the bank, and the address on the address inputs A_0-A_i(where A_i is the most significant column address bit for a given configuration) select the starting column location. The value on input A_{10} determines whether or not AUTO PRECHARGE is used. If AUTO PRECHARGE is selected, the row being accessed will be precharged at the end of WRITE burst; if AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

The module also support the AL feature, which allows WRITE or READ commands to be issued prior to ^{t}RCD(MIN) by delaying the actual registration of the READ/WRITE command to the internal device by AL clock cycles.

Input data appearing on the DQ's is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

SELF REFRESH

The SELF REFRESH command can be used to retain data even if the rest of the system is powered down. When in the SELF REFRESH mode, the DDR2 device retains data without external clocking. All power supply inputs (including V_{REF}) must be maintained at valid levels upon entry/exit and during SELF REFRESH operation.

REFRESH

REFRESH is issued during normal operation and is analogous t CAS\ before RAS\ (CBR) REFRESH. All banks must be in the idle mode prior to issuing a REFRESH command. This command is non-persistent, so it must be issued each time a REFRESH command is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during a REFRESH command.

MODE REGISTER (MR)

The MODE REGISTER is used to define the specific mode of operation. This definition includes the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, WRITE recovery, and POWER-DOWN mode, as shown in Figure 29. Contents of the MODE REGISTER can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables must be programmed when the command is issued.

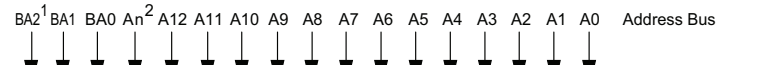
The MR is programmed via the LM command and will retain the stored information until it is programmed again or until the device loses power (except for bit M_8, which is SELF-CLEARING). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly. The LM command can only be issued (or reissued) when all banks are in the PRECHARGED state (idle state) and no bursts are in progress. The Memory controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVATE command. Violating either of these requirements will result in an unspecified operation.

BURST LENGTH

Burst length is defined by bits M_0-M_2, as shown in Figure 29. READ and WRITE accesses to the DDR2 device are burst-oriented, with BURST LENGTH being programmable to either four or eight. The BURST LENGTH determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the BURST LENGTH is effectively selected. All accesses for that BURST take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A_0-Ai when BL=4 and by A_3-Ai when BL=8 (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

FIGURE 29 - MR DEFINITIONS



M12	PD Mode
0	Fast exit (normal)
1	Slow exit (low power)

M7	Mode
0	Normal
1	Test

M8	DLL Reset
0	No
1	Yes

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	Reserved
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M11	M10	M9	Write Recovery
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

M3	Burst Type
0	Sequential
1	Interleaved

M15	M14	Mode Register Definition
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

M6	M5	M4	CAS Latency (CL)
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Notes:
1. M16 (BA2) is only applicable for densities ≥ 1Gb, reserved for future use, and must be programmed to "0."
2. Mode bits (Mn) with corresponding address balls (An) greater than M12 (A12) are reserved for future use and must be programmed to "0".
3. Not all listed WR and CL options are supported in any individual speed grade.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved. The BURST TYPE is selected via bit M3, as shown in Figure 29. The ordering of accesses within a burst is determined by the BURST LENGTH, BURST TYPE, and the starting column address, as shown in Table 38.

Table 38: Burst Definition

Burst Length	Starting Column Address (A[2,1,0])	Order of Accesses within a Burst: Type = Sequential	Order of Accesses within a Burst: Type = Interleaved
4	0 0	0,1,2,3	0,1,2,3
	0 1	1,2,3,0	1,0,3,2
	1 0	2,3,0,1	2,3,0,1
	1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2.3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	101	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	110	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	111	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

OPERATING MODE

The normal operating mode is selected by issuing a command with bit M7 set to "0" and all other bits set to the desired values, as shown in Figure 29. When bit M7 is "1", no other bits of the MODE REGISTER are programmed. Programming bit M7 to "1" places the DDR2 iMOD into a test mode that is only used by the manufacturer and should not be used. No operation or functionality is guaranteed if M7 bit is "1".

DLL RESET

DLL RESET is defined by bit M8 as shown in Figure 29. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is SELF-CLEARING, meaning it returns back to a value of "0" after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for the required clock cycles which synchronizes the DLL, may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

WRITE RECOVERY

WRITE RECOVERY (WR) time is defined by bits M9-M11, as shown in Figure 29. The WR register is used by the module during WRITE with AUTO PRECHARGE operation. During WRITE with AUTO PRECHARGE operation, the module delays the internal AUTO PRECHARGE operation by WR clocks (programmed in bits M9-M11) from the last data burst.

WR values of 2, 3, 4, 5, 6, 7 or 8 clocks may be used for programming bits M9-M11. The user is required to program the value of WR which is calculated by dividing ^{t}WR (in nanoseconds) by ^{t}CK (in nanoseconds) and rounding up a non-integer value to the next integer; WR(cycles) = ^{t}WR(ns)/^{t}CL(ns). Reserved states should not be used as an unknown operation or incompatibility with future versions may result.

POWER-DOWN MODE

Active POWER-DOWN (PD) mode is defined by bit M12, as shown in Figure 29. PD mode enables the user to determine the active power-down mode which determines performance versus power savings. PD mode bit M12 does not apply to PRECHARGE PD mode.

When bit M12=0, standard active PD mode, or "fast exit" active PD mode, is enabled. The tXARD parameter is used for fast-exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12=1, a lower-power active PD mode, or "slow-exit" active PD mode is enabled. The tXARDS parameter is used for the slow-exit active PD exit timing. The DLL can be enabled but "frozen" during ACTIVE PD mode because the exit-to-READ command timing is relaxed. The power difference expected between IDD3P normal and IDD3P low-power mode is defined in the DDR2 IDD Specifications and Conditions table.

CAS LATENCY (CL)

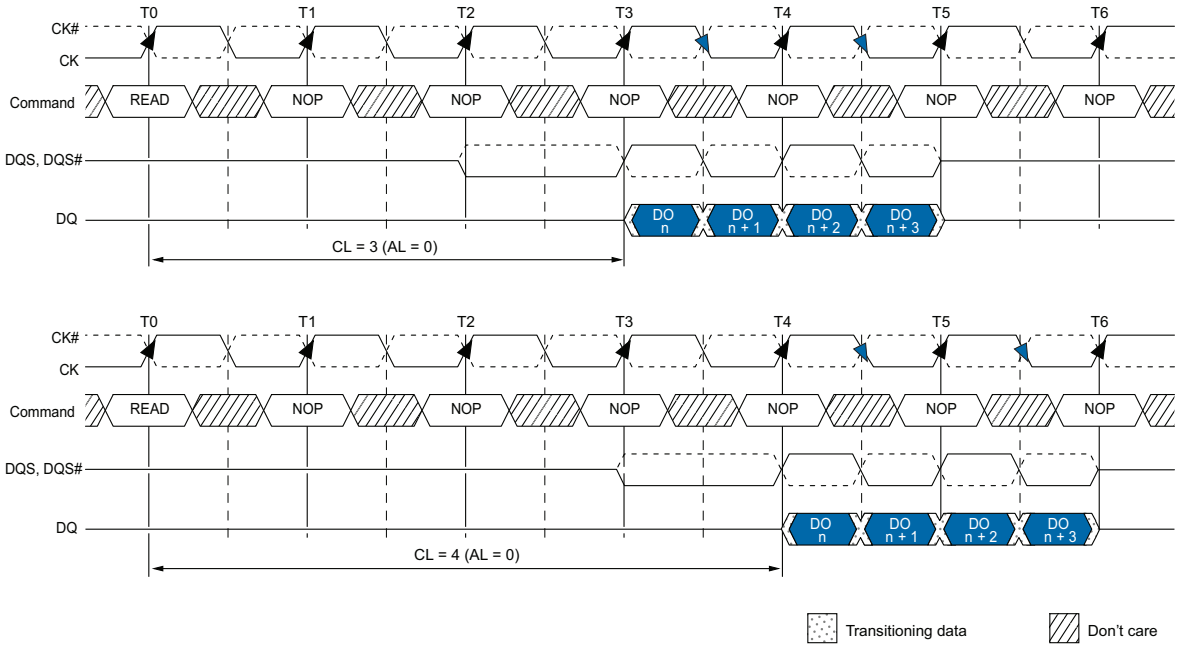
The CAS LATENCY (CL) is defined by bits M4-M6 as shown in Figure 29. CL is the delay in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, 5, 6 or 7 clocks, depending on the speed grade option of the iMOD being used.

The module does not support any half-clock latencies. Reserved states should not be used as an unknown state or operation or incompatibility with future revisions may result.

The module also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to tRCD(MIN) by delaying the internal command to the DDR2 iMOD by AL clocks. The AL feature is described in further detail in the Posted CAS Additive Latency description.

Examples of CL=3 and CL=4 are shown in Figure 30; both assume AL=0. If a READ command is registered at clock edge n, and the CL is m clocks, the data will be available nominally coincident with clock edge n + m (this assumes AL = 0).

FIGURE 30 - CL



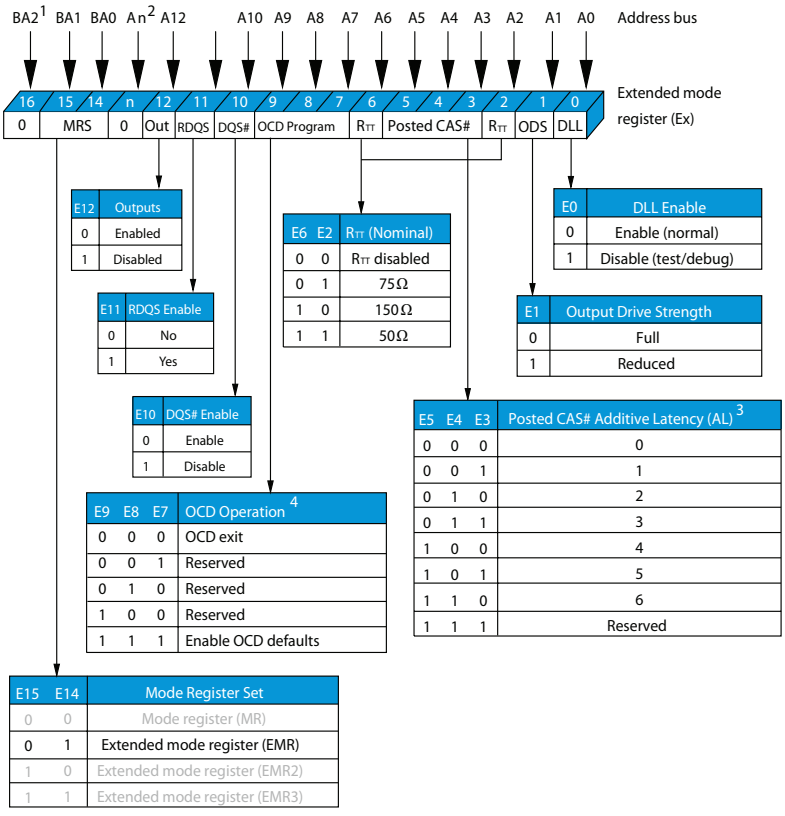
Notes:
1. BL = 4.
2. Posted CAS# additive latency (AL) = 0.
3. Shown with nominal tAC, tDQSCK, and tDQSQ.

EXTENDED MODE REGISTER (EMR)

The EXTENDED MODE REGISTER controls functions beyond those available and controlled via the MODE REGISTER (MR); these additional functions are DLL enable/disable, OUTPUT DRIVE strength, On-Die-Termination (ODT), Posted AL, Off-Chip Driver Impedance calibration (OCD), DQS\ enable/disable and Output disable/enable. These function are controlled via the bits shown in Figure 31. The EMR is programmed via the LM command and will retain the stored information until it is programmed again or the module loses power. Re-programming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress and the controller must wait the specified time (^{t}MRD) before initiating any subsequent operations. Violating either of these requirements could result in an unspecified operation.

FIGURE 31 - EMR DEFINITIONS



Notes:
1. E16 (BA2) is only applicable for densities ≥ 1Gb, reserved for future use, and must be programmed to "0".
2. Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to "0".
3. Not all listed AL options are supported in any individual speed grade.
4. As detailed in the Initialization (page 82) section notes, during initialization of the OCD operation, all three bits must be set to "1" for the OCD default state, then set to "0" before initialization is finished.

DLL ENABLED/DISABLED

The DLL may be ENABLED or DISABLED by programming bit E0 during the LM command, as shown in Figure 31. These specifications are applicable when the DLL is enabled for normal operation. DLL ENABLE is required during POWER-UP initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by re-setting the DLL using the LM command.

The DLL is automatically DISABLED when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operations.

Anytime the DLL is ENABLED (and subsequently reset), 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Anytime the DLL is DISABLED and the iMOD is operated below 25MHz, any AUTO REFRESH command should be followed by a PRECHARGE ALL command.

ON-DIE-TERMINATION (ODT)

ODT effective resistance, RTT(EFF), is defined by bits E2 and E6 of the EMR, as shown in Figure 31. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 memory controller to independently turn on or off ODT for any or all devices. RTT effective resistance values of 50Ω, 75Ω and 150Ω are selectable and apply to each DQ, DQS/DQS\, and DM signals. Bits (E6,E2) determine what ODT resistance is enabled by turning on/off "sw1, sw2 or sw3".

The ODT effective resistance value is selected by enabling switch "sw1", which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω (RTT2 [EFF]=R2/2). Similarly, if "sw2" is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω each, enabling an effective resistance of 75Ω (RTT2 [EFF] = R2/2). Similarly, if "sw3" is enabled, all R2 values that are 100Ω each, enable and effective ODT resistance of 50Ω. Reserved states should not be used, as an unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during ACTIVE, ACTIVE POWER-DOWN (both fast-exit and slow-exit modes), and PRECHARGE POWER-DOWN modes of operation.

ODT must be turned off prior to entering SELF REFRESH mode. During POWER-UP and INITIALIZATION of the DDR2 iMOD, ODT should be disabled until the EMR command is issued. This will enable the ODT feature, at which point the ODT ball will determine the RTT(EFF) value. Anytime the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled.

DQS\ ENABLE/DISABLE

The DQS\ ball is ENABLED by bit E10=0, DQS\ is the complement of the differential data strobe pair. When DISABLED, DQS\ should be left floating; however, it may be tied to ground via a 20Ω to 10KΩ resistor.

OUTPUT DRIVE STRENGTH

The OUTPUT DRIVE STRENGTH is defined by bit E1 as shown in Figure 32. The NORMAL DRIVE STRENGTH for all outputs is specified to be SSTL_18. Programming bit E1=0 selects normal (full strength) DRIVE STRENGTH for all outputs. Selecting a REDUCED DRIVE STRENGTH option (E1=1) will reduce all outputs to approximately 45 to 60 percent of the SSTL-18 DRIVE STRENGTH. This option is intended for the support of lighter load and/or point-to-point environments.

OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE/DISABLE function is defined by bit E12 as shown in Figure 31. When ENABLED (E12=0), all outputs (DQ, DQS, DQS\) function normally. When DISABLED (E12=1), all outputs are DISABLED, thus removing output buffer current. The output DISABLE feature is intended to be used during IDD characterization of READ current.

OFF-CHIP DRIVER (OCD) IMPEDANCE CALIBRATION

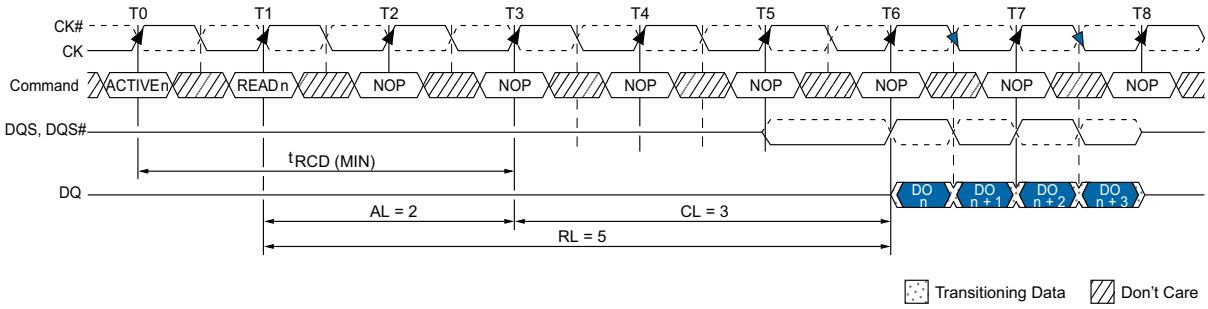
The OFF-CHIP DRIVER (OCD) function is an optional DDR2 JEDEC feature which is not supported by LOGIC Devices iMOD device, therefore this function must be set and maintained in the default state. Enabling this function outside of the default settings will alter the I/O drive characteristics and the timing and output I/O specifications will no-longer be valid.

POSTED CAS ADDITIVE LATENCY (AL)

POSTED CAS ADDITIVE (AL) is supported to make the command and data bus efficient for sustainable bandwidths in the DDR2 iMOD. Bits E3-E5 define the value of AL. Bits E3-E5 allow the user to program the DDR2 iMOD with an AL of 0, 1, 2, 3, 4, 5, or 6 clocks. Reserved states should not be used as an unknown operation or incompatibility with future revisions may result.

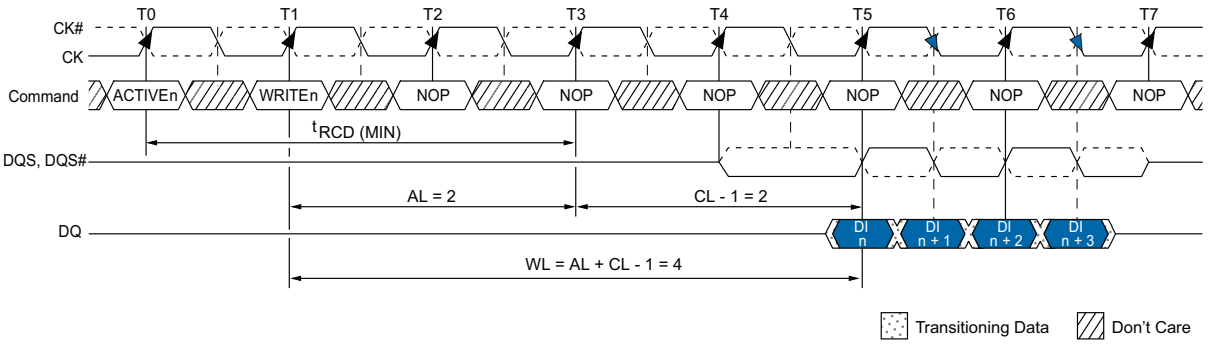
In this operation, the DDR2 iMOD allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) – 1 x ^{t}CK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 iMOD device. RL is controlled by the sum of AL and CL; RL = AL + CL. WRITE latency (WL) is equal to RL minus on clock; WL = AL + CL – 1 x ^{t}CK.

Figure 32 - READ Latency



Notes:
1. BL = 4
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
3. RL = AL + CL = 5.

Figure 33 - WRITE Latency



Notes:
1. BL = 4
2. CL = 3.
3. WL = AL + CL - 1 = 4.

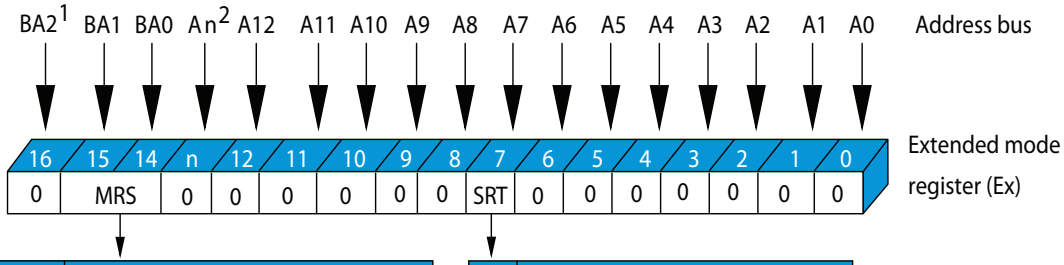
EXTENDED MODE REGISTER 2 (EMR2)

The EXTENDED MODE REGISTER 2 (EMR2) controls functions beyond those controlled by the MODE REGISTER. Currently all bits in the EMR2 are reserved, except for E7, which is used in commercial or high-temperature operations, as shown in Figure 34. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or until the iMOD is subjected to a loss of power condition. Reprogramming the EMR2 will not alter the contents of the array, provided it has been performed correctly.

Bit E7 (A7) must be programmed as "1" to provide a faster REFRESH RATE on IT, ET or M devices if TC is or does exceed 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in an unspecified operation.

FIGURE 34 - EMR2 DEFINITIONS



E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

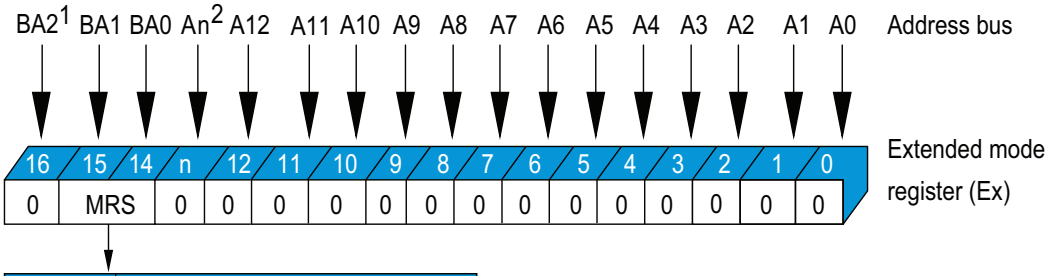
E7	SRT Enable
0	1X refresh rate (0°C to 85°C)
1	2X refresh rate (>85°C)

Notes:
1. E16 (BA2) is only applicable for densities ≥ 1Gb, reserved for future use, and must be programmed to "0".
2. Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to "0".

EXTENDED MODE REGISTER 3 (EMR3)

The EXTENDED MODE REGISTER 3 (EMR3) controls functions beyond those controlled by the MODE REGISTER. Currently all bits of the EMR3 are reserved, as shown in Figure 35. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or until the iMOD is subjected to a loss of power condition. Reprogramming the EMR3 will not alter the contents of the memory array, provided it is performed correctly.

FIGURE 35 - EMR3 DEFINITIONS



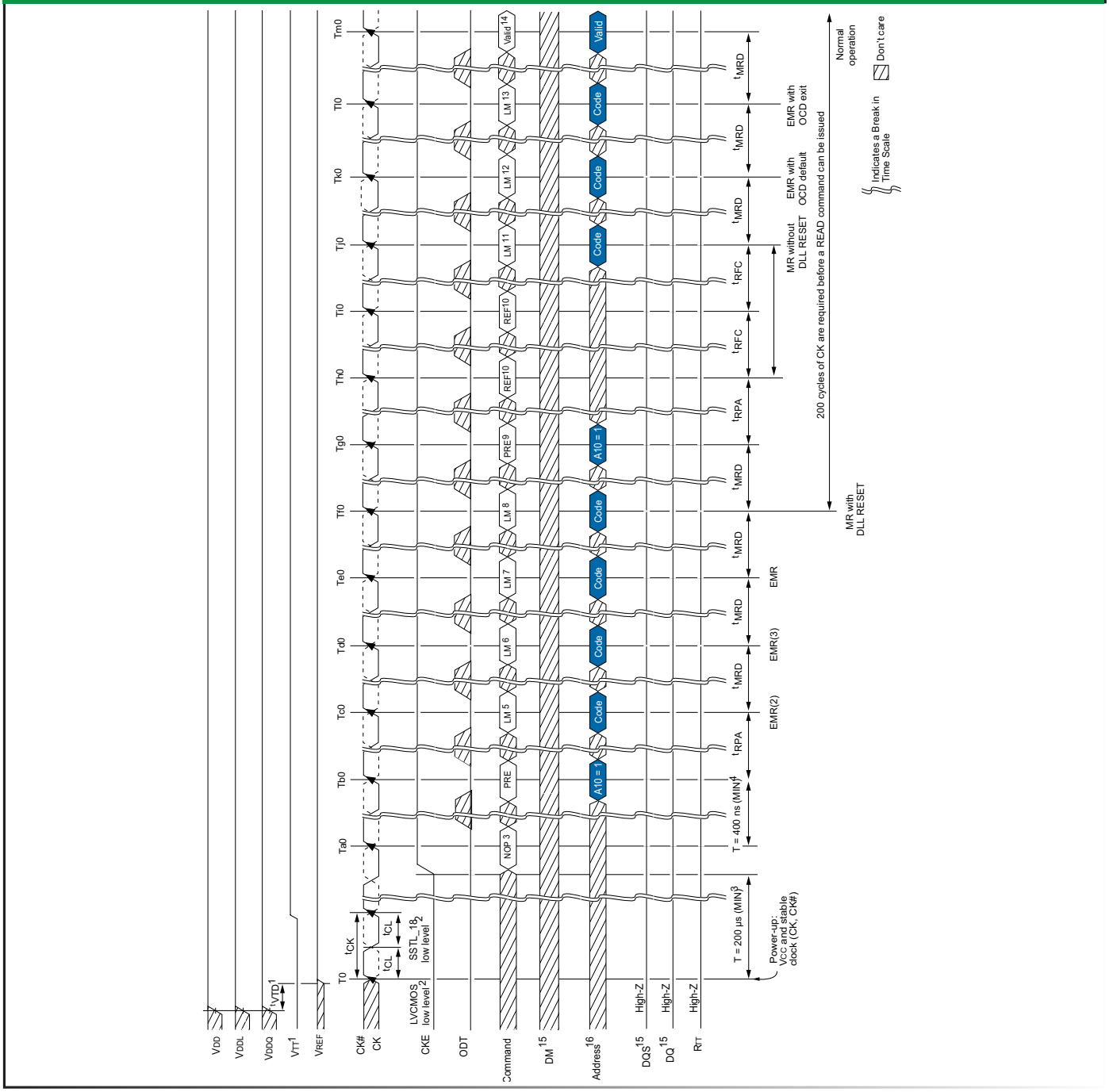
E15	E14	Mode Register Set
0	0	Mode register (MR)
0	1	Extended mode register (EMR)
1	0	Extended mode register (EMR2)
1	1	Extended mode register (EMR3)

Notes:
1. E16 (BA2) is only applicable for densities ≥ 1Gb, reserved for future use, and must be programmed to “0”.
2. Mode bits (En) with corresponding address balls (An) greater than E12 (A12) are reserved for future use and must be programmed to “0”.

INITIALIZATION

The module must be POWERED-UP and INITIALIZED in a predefined manner. Operational procedures other than those specified may result in undefined operation. Figure 36 illustrates, and the notes outline the sequence required for POWER-UP and INITIALIZATION.

Figure 36 - DDR2 Power-Up and Initialization

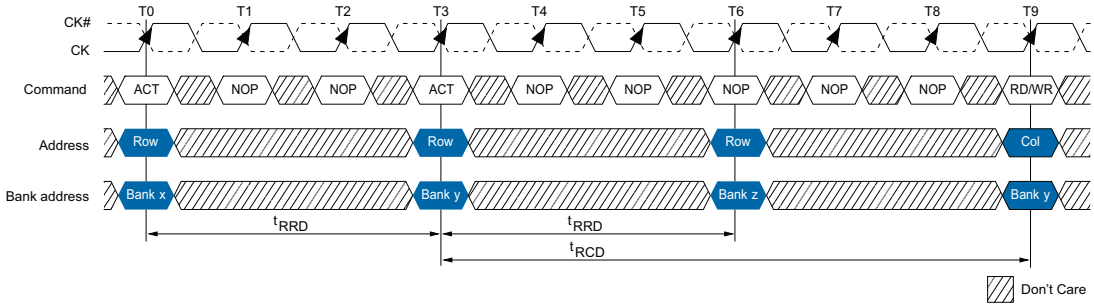


ACTIVATE

Before an READ or WRITE commands can be issued to a bank within the DDR2 iMOD, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated.

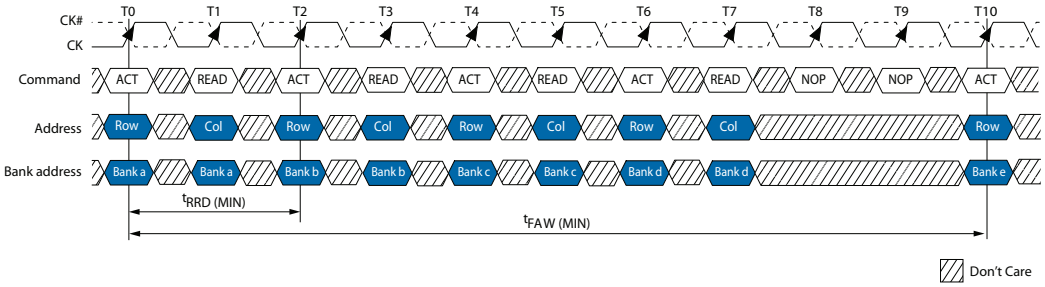
After a row is opened with an ACTIVATE command, a READ or WRITE command may be issued to that row subject to the ^{t}RCD specification. ^{t}RCD(MIN) should be defined by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD(MIN) specification of 20ns with a 266MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks, rounded up to 6. This is shown in Figure 37.

Figure 37 - Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)



A subsequent ACTIVATE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by ^{t}RC. A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in reduction of total row access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by ^{t}RRD. DDR2 with 8-bank architectures have an additional requirement: ^{t}FAW. This requires no more than four ACTIVATE commands may be issued in any given ^{t}FAW(MIN) period, as shown in Figure 38.

Figure 38 - Multibank Activate Restriction



Note: 1. DDR2-533 (-37E, x4 or x8), ^{t}CK = 3.75ns, BL = 4, AL = 3, CL = 4, ^{t}RRD (MIN) = 7.5ns, ^{t}FAW (MIN) = 37.5ns.

READ

READ bursts are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and the AUTO PRECHARGE is either enabled or disabled for that BURST sequence or access. If AUTO PRECHARGE is enabled, the row being accessed is automatically PRECHARGED at the completion of the burst. If AUTO PRECHARGE is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL; RL = AL + CL. The value of AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (at the next crossing of CKx and CKx\). Figure 39 shows examples of RL based on different AL and CL settings.

DQSx/DQSx\ is driven by the DDR2 iMOD along with output data. The initial LOW state on DQSx and the HIGH state on DQSx\ coincident with the last data-out element are known as the READ preamble (^{t}PRE). The low state on DQSx and the HIGH state coincident with the last data-out element are know as the READ postamble (^{t}PRST).

Upon completion of a BURST, assuming no other commands have been initiated, the DQ buss will go HIGH-Z. A detailed explanation of ^{t}DQSCK (DQSx transition skew to CL) and ^{t}AC (data-out transition skew to CKx) is shown in Figure 48.

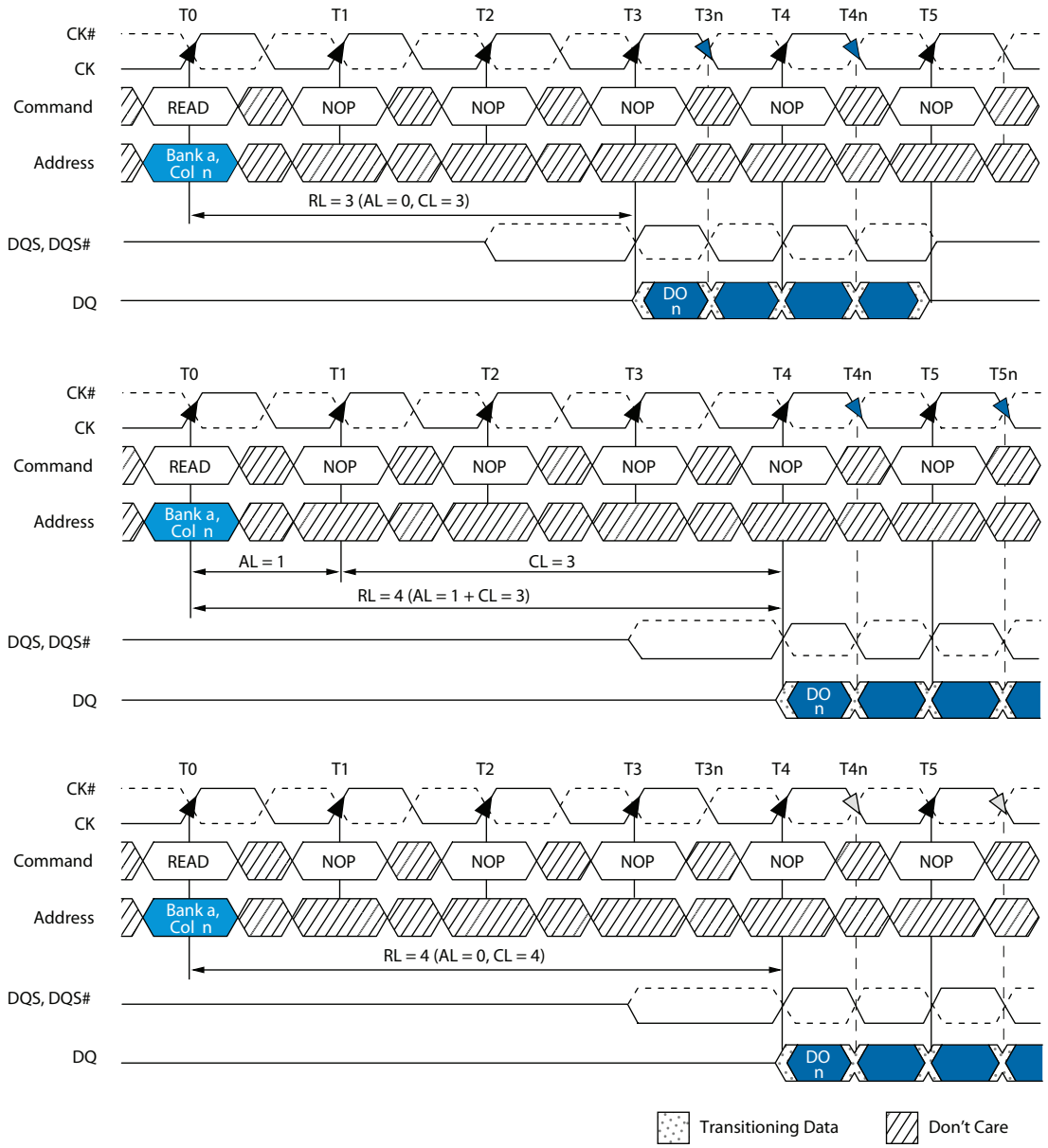
Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals BL/2 cycles (see Figure 40).

Nonconsecutive READ data is illustrated in Figure 41. Full-speed random READ accesses within a page (or pages) can be performed. DDR2 iMOD devices support the use of concurrent AUTO PRECHARGE timing.

DDR2 iMOD devices do not allow interrupting or truncating of an READ burst using BL = 4 operations. Once the BL=4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with AUTO PRECHARGE disabled) using VL=8 operation, the READ may be interrupted and truncated only by another READ burst as long as the interruption occurs on a 4-bit boundary, and this allowed due to the 4n prefetch architecture of the DDR2 iMOD. AS shown in Figure 43, READ burst BL=8 operations may not be interrupted or truncated with any other command except for another READ.

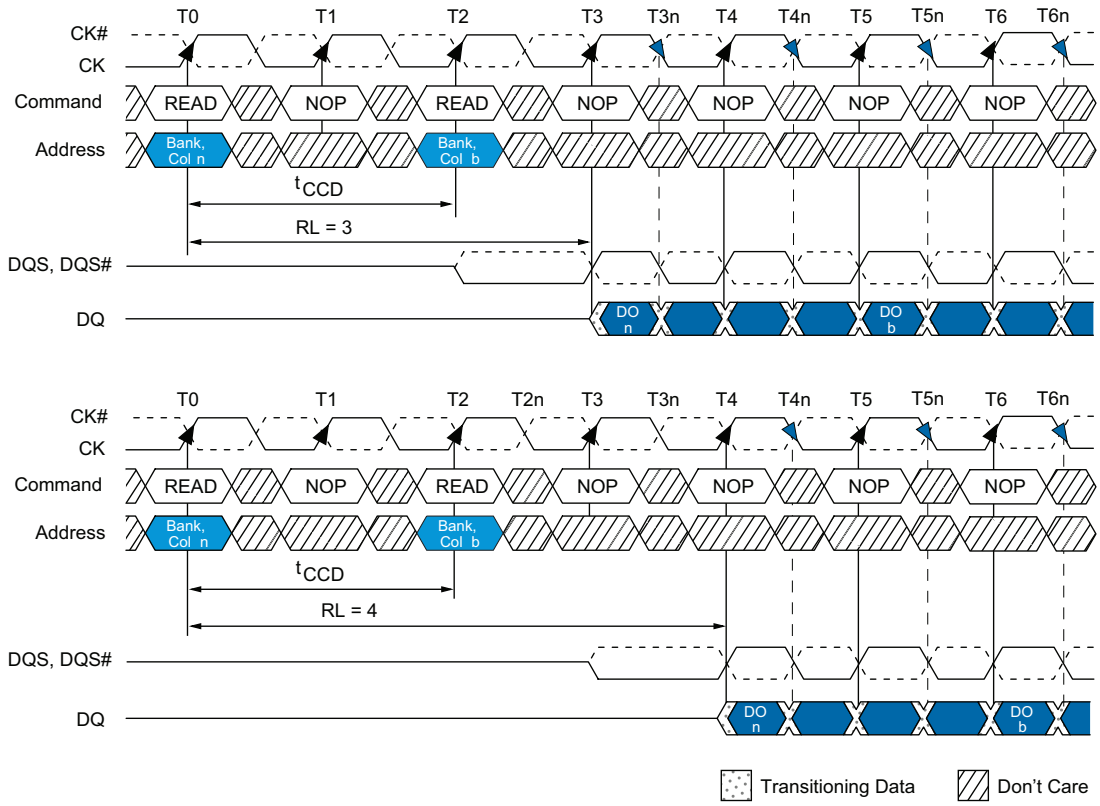
Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst is shown in Figure 43.

Figure 39 - READ Latency



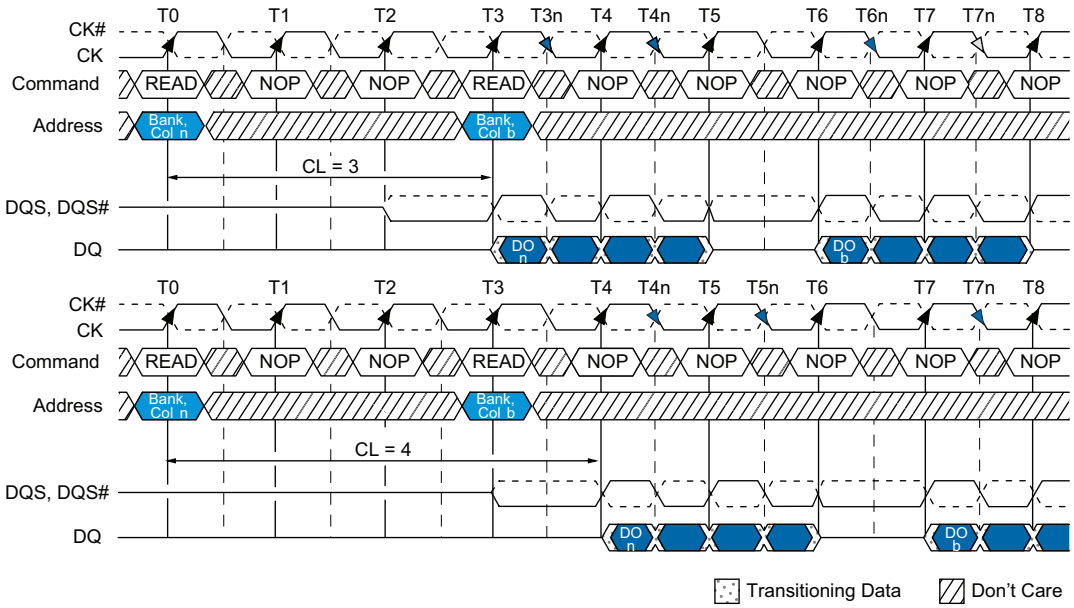
Notes:
1. DO n = data-out from column n.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 40 - Consecutive READ Bursts



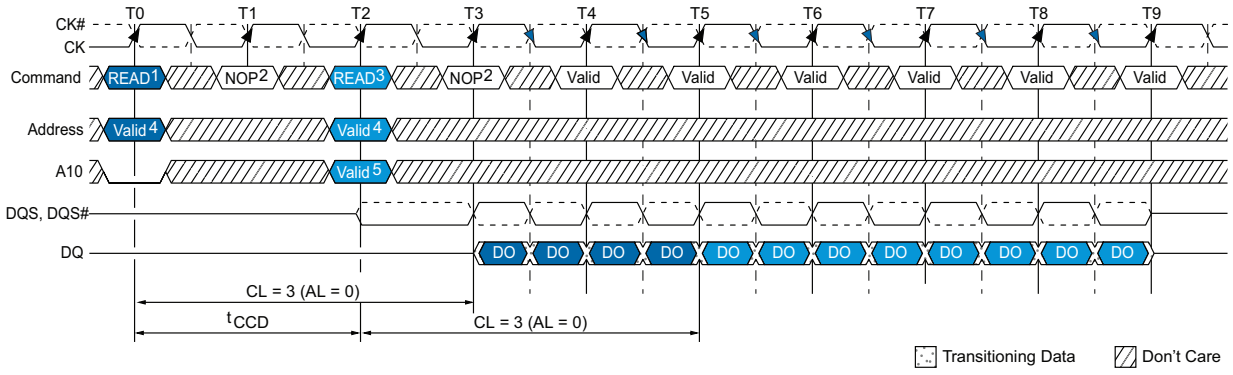
Notes:
1. DOn (or b) = data-out from column (or column b).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DOn.
4. Three subsequent elements of data-out appear in the programmed order following DOb.
5. Shown with nominal tAC, tDQSCK, and tDQSQ.
6. Example applies only when READ commands are issued to same device.

Figure 41 - Nonconsecutive READ Bursts



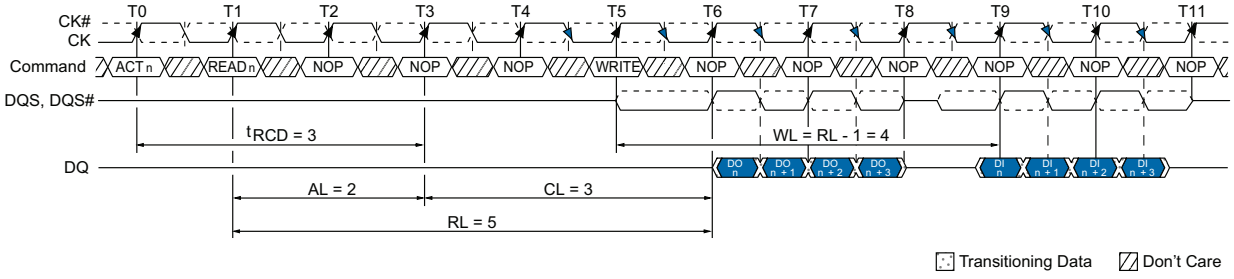
Notes:
1. DOn (or b) = data-out from column n (or column b).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DOn.
4. Three subsequent elements of data-out appear in the programmed order following DOb.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

Figure 42 - READ Interrupted by READ



Notes:
1. BL = 8 required; auto precharge must be disabled (A10 = LOW).
2. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
3. Interrupting READ command must be issued exactly 2 × ^{t}CK from previous READ.
4. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
5. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting READ command.
6. Example shown uses AL = 0; CL = 3, BL = 8, shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 43 - READ-to-WRITE



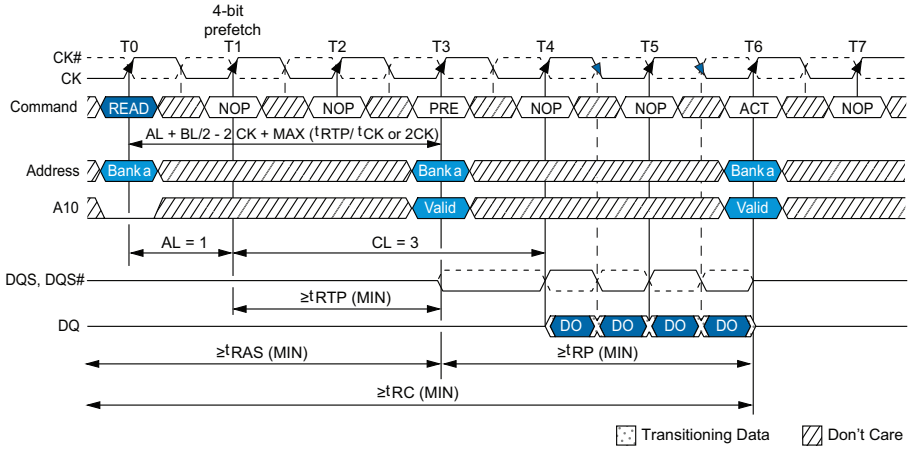
Notes:
1. BL = 4; CL = 3; AL = 2.
2. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ WITH PRECHARGE

A READ burst may be followed by a PRECHARGE command to the same bank, provided AUTO PRECHARGE is not activated. The minimum READ to PRECHARGE command spacing to the same bank has two requirements that must be satisfied: AL + BL/2 clocks and ^{t}RTP. ^{t}RTP is the minimum time from the rising clock edge that initiates the last 4-bit PREFETCH of a READ command to the PRECHARGE command. For BL=4, this is the time from the actual READ (AL after the READ command) to PRECHARGE command. For BL=8, this is the time from AL + 2 x CL after the READ-to-PRECHARGE command. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. However, part of the row PRECHARGE time is hidden during the access of the last data elements.

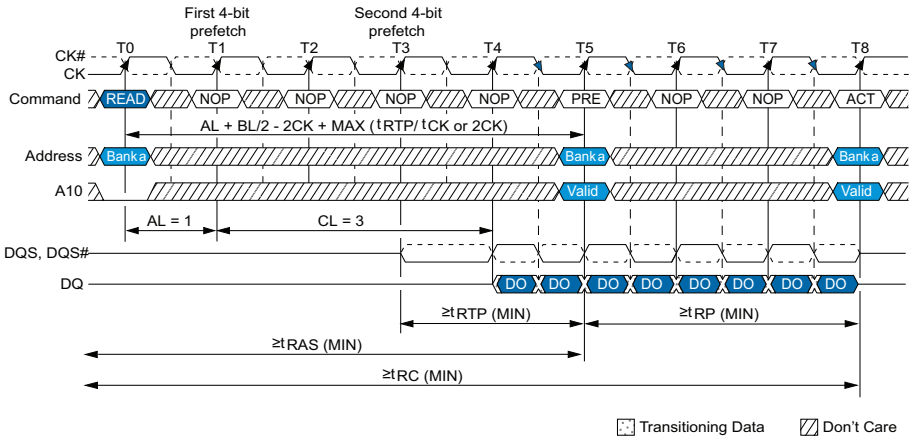
Examples of READ-to-PRECHARGE for BL=4 are shown in Figure 44 and in Figure 45 for BL=8. The delay from READ-to-PRECHARGE to the same is AL + BL/2 – 2CK + MAX (^{t}RP/^{t}CK or 2 x CK) where MAX means the larger of the two.

Figure 44 - READ-to-PRECHARGE – BL = 4



Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 4.
2. ^{t}RTP≥ 2 clocks.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 45 - READ-to-PRECHARGE – BL = 8



Notes:
1. RL = 4 (AL = 1, CL = 3); BL = 8.
2. ^{t}RTP≥ 2 clocks.
3. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

READ WITH AUTO PRECHARGE

If A10 is high when a READ command is issued, the READ with AUTO PRECHARGE function is engaged. The module starts an AUTO PRECHARGE operation on the rising edge of clock that is AL + (BL/2) cycles later than the READ with AUTO PRECHARGE command provided ^{t}RAS(MIN) and ^{t}RTP are satisfied. If ^{t}RAS(MIN) is not satisfied at this rising clock edge, the start point of the AUTO PRECHARGE operation will be delayed until ^{t}RAS(MIN) is satisfied. When the internal PRECHARGE is pushed out by ^{t}RTP, ^{t}RP starts at the point where the internal PRECHARGE happens.

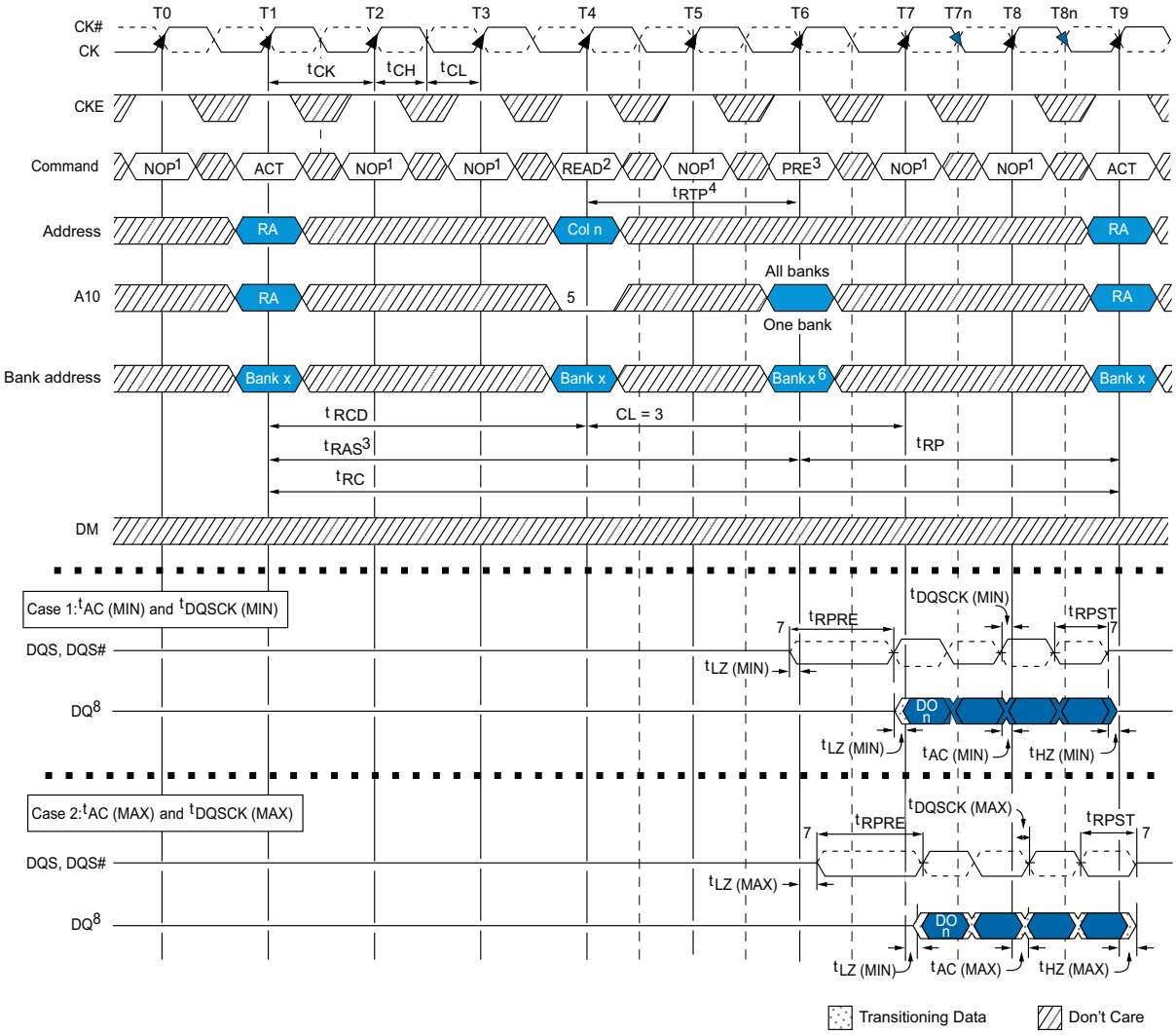
When BL=4, the minimum time from READ with AUTO PRECHARGE to the next ACTIVATE command is AL + (^{t}RTP + ^{t}RP)/^{t}CK. When BL=8, the minimum time from READ with AUTO PRECHARGE to the next ACTIVATE command is AL + 2 clocks + (^{t}RTP + ^{t}RP)/^{t}CK. The term (^{t}RTP + ^{t}RP)/^{t}CK is always rounded up to the next integer. A general purpose equation can also be used: AL + B>/2 – 2CK + (^{t}RTP + ^{t}RP)/^{t}CK. In any event, the internal PRECHARGE does not start earlier than two clocks after the last 4-bit prefetch.

READ with AUTO PRECHARGE command may be applied to one bank while another bank is operational. This is referred to as CONCURRENT AUTO PRECHARGE operation. Examples of READ with PRECHARGE and READ with AUTO PRECHARGE with applicable timing requirements are shown in Figure 46.

Table 39: READ Using CONCURRENT AUTO PRECHARGE

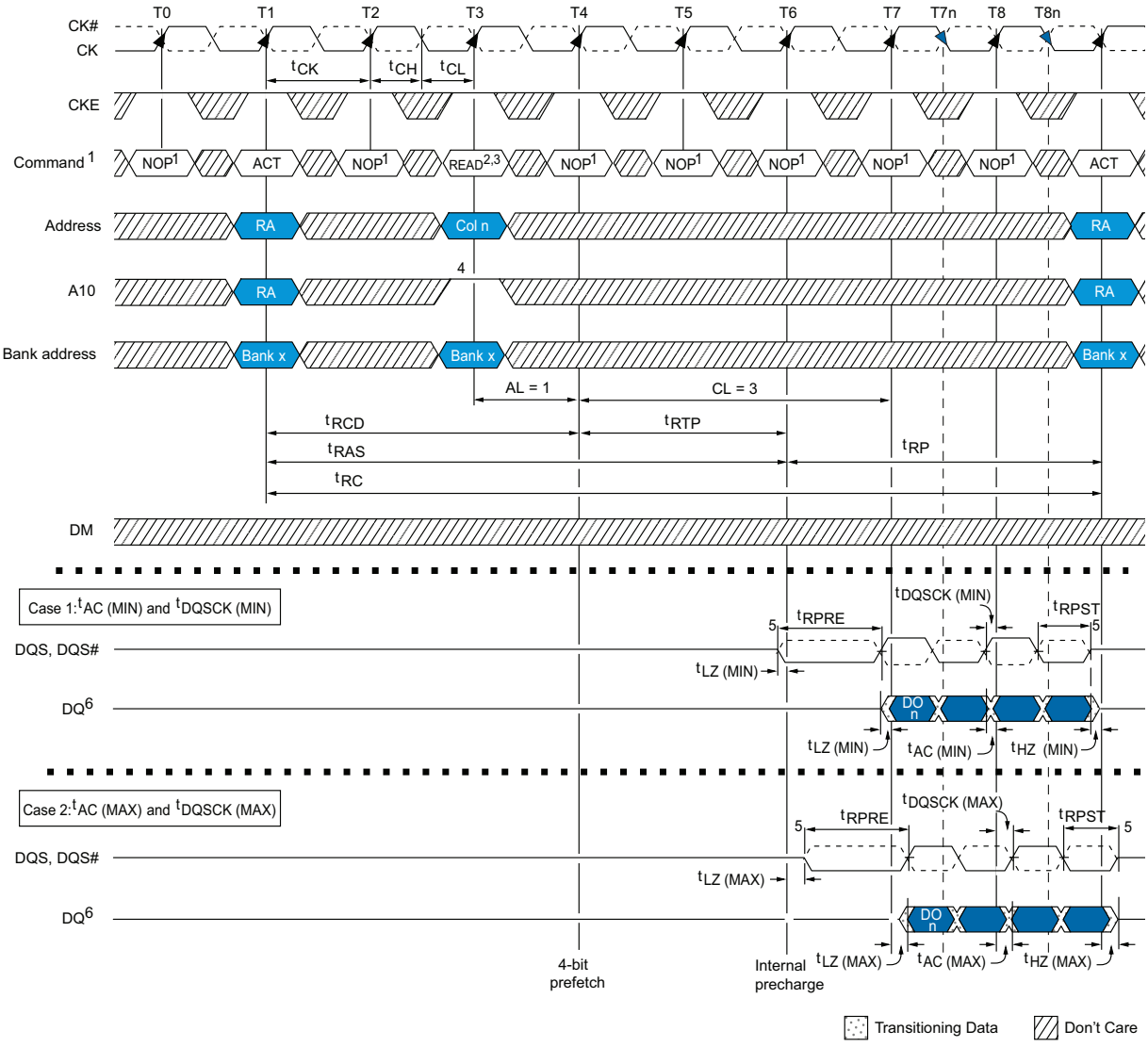
From Command (Bank n)	To Command (Bank m)	Minimum Delay (with Concurrent AUTO PRECHARGE)	UNITS
READ with AUTO PRECHARGE	READ or READ with Auto Precharge	(BL/2)	^{t}CK
	WRITE or WRITE with Auto Precharge	(BL/2) + 2	
	PRECHARGE or ACTIVATE	1	

Figure 46 - Bank Read – Without Auto Precharge



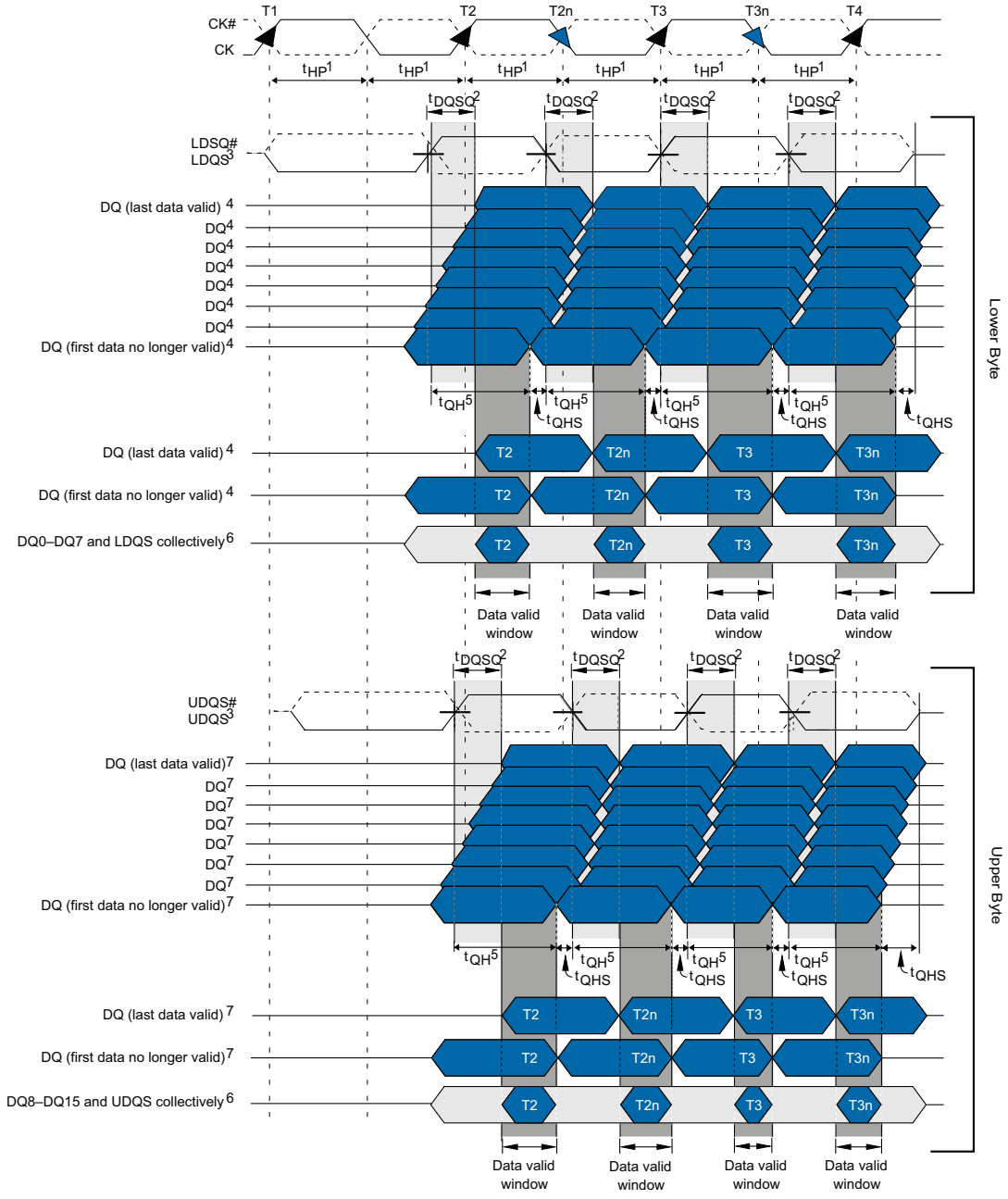
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. The PRECHARGE command can only be applied at T6 if ^{t}RAS (MIN) is met.
4. READ-to-PRECHARGE = AL + BL/2 - 2CK + MAX (^{t}RTP/ ^{t}CK or 2CK).
5. Disable auto precharge.
6. "Don't Care" if A10 is HIGH at T5.
7. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
8. DO n = data-out from column n; subsequent elements are applied in the programmed order.

Figure 47 - Bank Read – with Auto Precharge



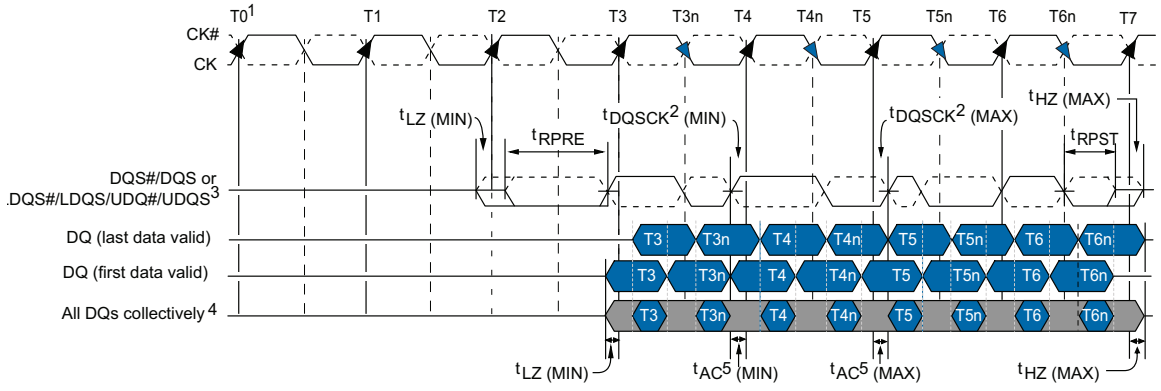
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
3. The DDR2 SDRAM internally delays auto precharge until both tRAS (MIN) and tRTP (MIN) have been satisfied.
4. Enable auto precharge.
5. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.
6. DO n = data-out from column n; subsequent elements are applied in the programmed order.

Figure 48 - Data Output Timing – tDQSQ, tQH, and Data Valid Window



Notes:
1. tHP is the lesser of tCL or tCH clock transitions collectively when a bank is active.
2. tDQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
3. DQ transitioning after the DQS transitions define the tDQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.

Figure 49 - Data Output Timing – tAC and tDQSCK



Notes:

1. READ command with CL = 3, AL = 0 issued at T0.
2. tDQSCK is the DQS output window relative to CK and is the long-term component of DQS skew.
3. DQ transitioning after DQS transitions define tDQSQ window.
4. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
5. tAC is the DQ output window relative to CK and is the "long term" component of DQ skew.
6. tLZ (MIN) and tAC (MIN) are the first valid signal transitions.
7. tHZ(MAX) and tAC(MAX) are the latest valid signal transitions.
8. I/O balls, when entering or exiting High-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

WRITE

WRITE bursts are initiated with a WRITE command. The device uses WL equal to RL minus one clock cycle (WL = RL - 1CK. The starting column and bank addresses are provided with the WRITE command, and AUTO PRECHARGE is either enabled or disabled for that access. If AUTO PRECHARGE is enabled, the row being accessed is PRECHARGED at the completion of the burst.

During WRITE bursts, the first valid data in element will be registered on the first rising edge of DQSx following the WRITE command, and subsequent data elements will be registered on successive edges of DQSx. The low state on DQSx between the WRITE command and the first rising edge is known as the WRITE preamble; the low state on DQSx following the last data-in element is known as the postamble.

The time between the WRITE command and the first rising DQSx edge is WL ± tDQSS. Subsequent DQSx positive rising edges are timed, relative to the associated clock edge, as ± tDQSS. tDQSS is specified with a relatively wide range (25 percent of on clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (tDQSS [MIN] and tDQSS[MAX]) might not be intuitive, they have also been included. Figure 50 shows the nominal case and the extremes of tDQSS for BL=4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous data flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued x cycles after the first WRITE command, where x equals BL/2.

Figure 51 shows concatenated bursts of BL = 4 and how full-speed random WRITE accesses within a page or pages can be performed. An example of non consecutive WRITE accesses is shown in Figure 52. DDR2 iMOD devices support concurrent AUTO PRECHARGE options as shown in Table 40.

The module does not allow interrupting or truncating any WRITE burst using BL=4 operation. Once the BL=4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE BL=8 operation (with AUTO PRECHARGE disabled) might be interrupted and truncated only by another WRITE command, as shown in Figure 53.

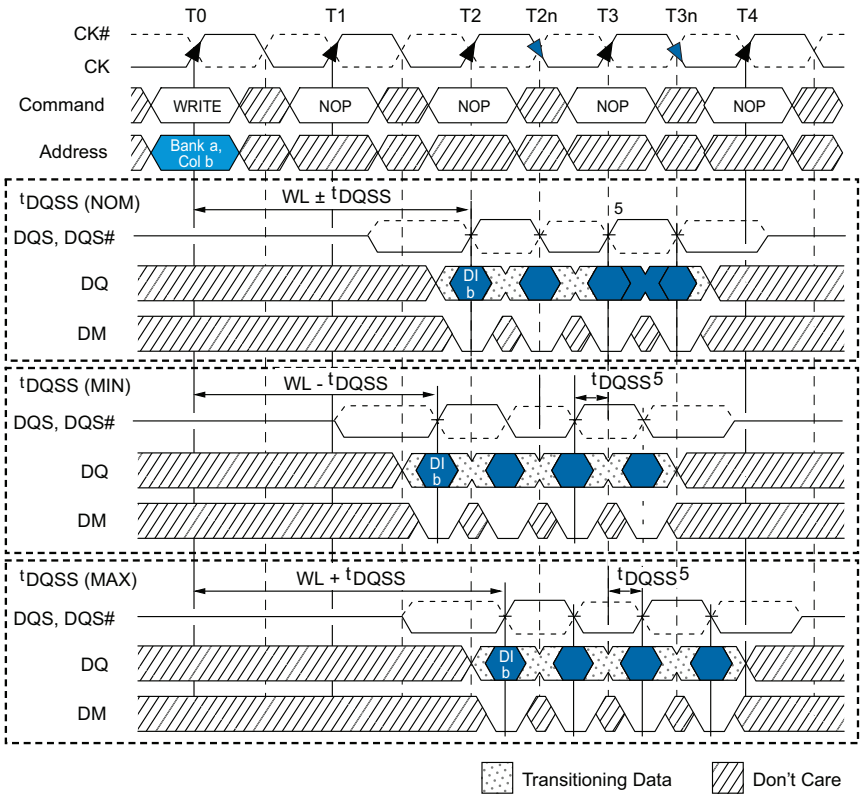
Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE, tWTR should be met, as shown in Figure 54. The number of clock cycles required to meet tWTR is either 2 or tWTR/tCK, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. tWR must be met, as shown in Figure 55. tWR starts at the end of the data burst, regardless of the data mask condition.

WRITE Continued

Table 40: WRITE Using Concurrent Auto Precharge

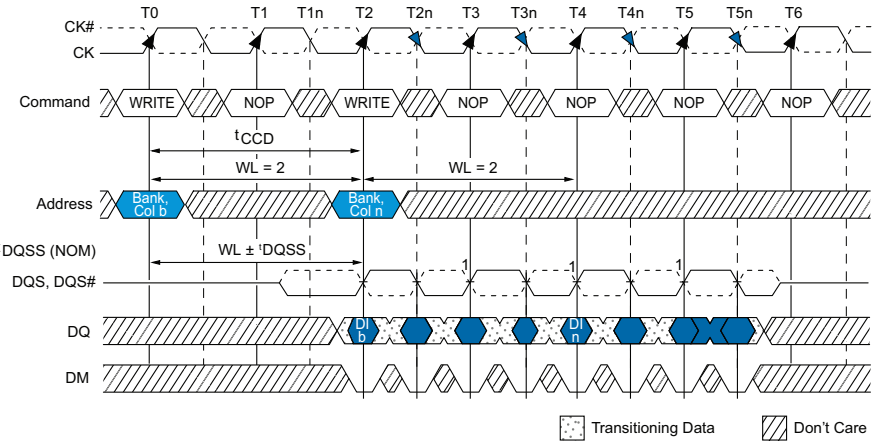
From Command (Bank n)	To Command (Bank m)	Minimum Delay (with Concurrent AUTO PRECHARGE)	UNITS
WRITE with AUTO PRECHARGE	READ or READ with Auto Precharge	(CL-1) + (BL/2) + tWTR	tCK
	WRITE or WRITE with Auto Precharge	(BL/e)	
	PRECHARGE or ACTIVATE	1	

Figure 50 - Write Burst



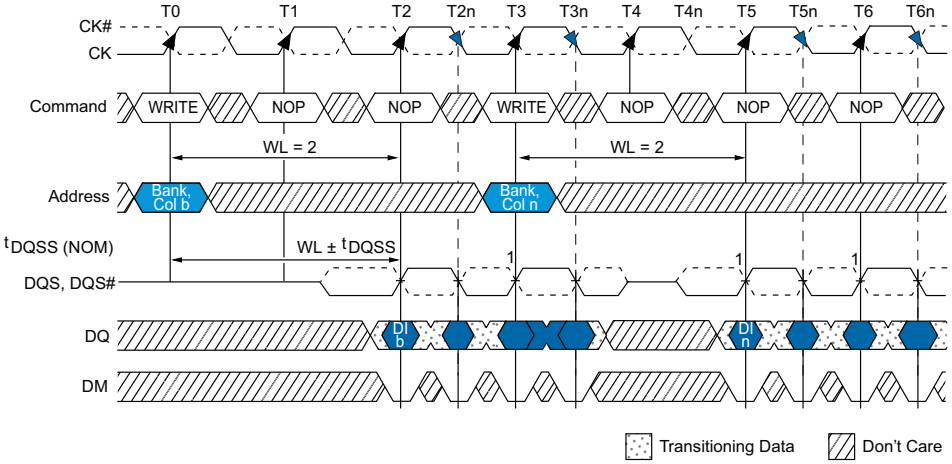
Notes:
1. Subsequent rising DQS signals must align to the clock within tDQSS.
2. DI b = data-in for column b.
3. Three subsequent elements of data-in are applied in the programmed order following DI b.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 51 - Consecutive WRITE-to-WRITE



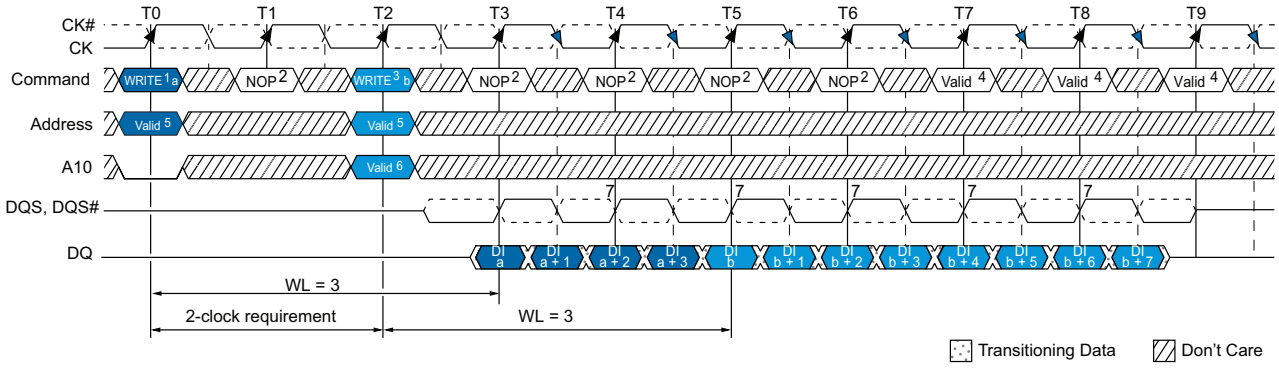
Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI b, etc. = data-in for column b, etc.
3. Three subsequent elements of data-in are applied in the programmed order following DI b.
4. Three subsequent elements of data-in are applied in the programmed order following DI n.
5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

Figure 52 - Nonconsecutive WRITE-to-WRITE



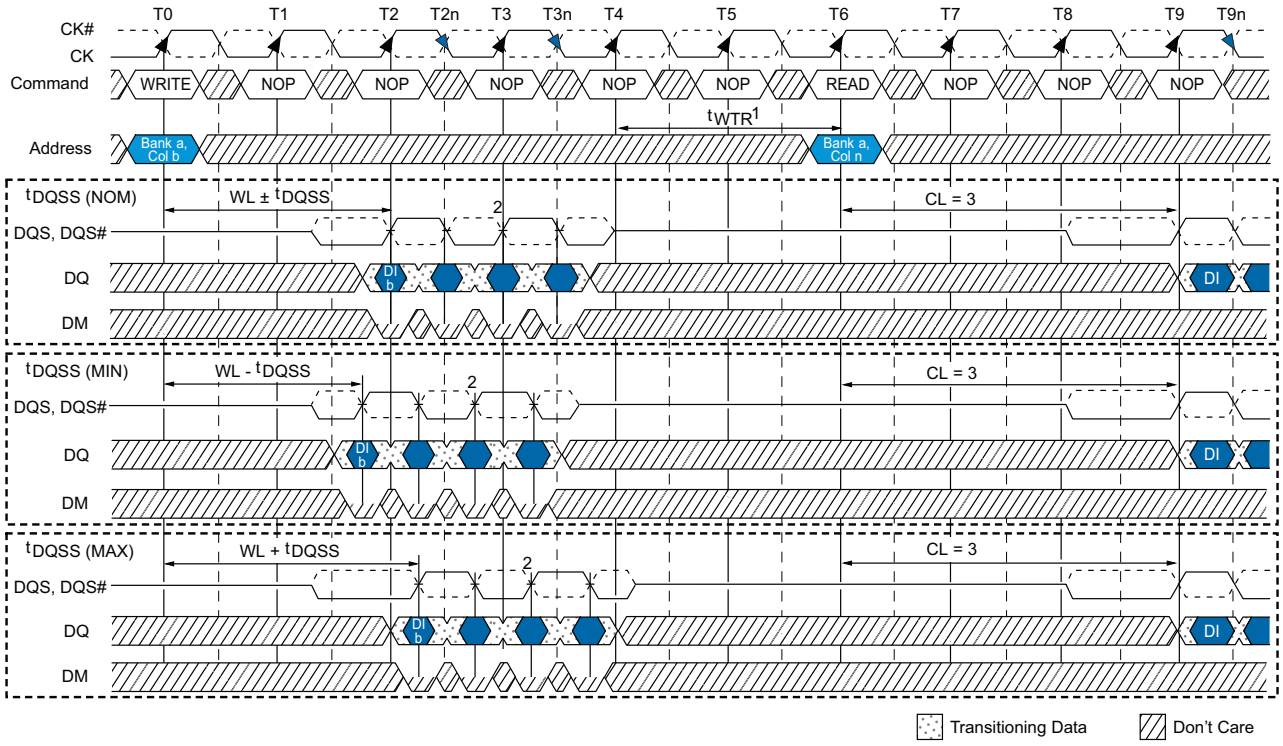
Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DIb (or n), etc. = data-in for column b (or columnn).
3. Three subsequent elements of data-in are applied in the programmed order following DI b.
4. Three subsequent elements of data-in are applied in the programmed order following DI n.
5. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
6. Each WRITE command may be to any bank.

FIGURE 53 - WRITE INTERRUPTED BY WRITE



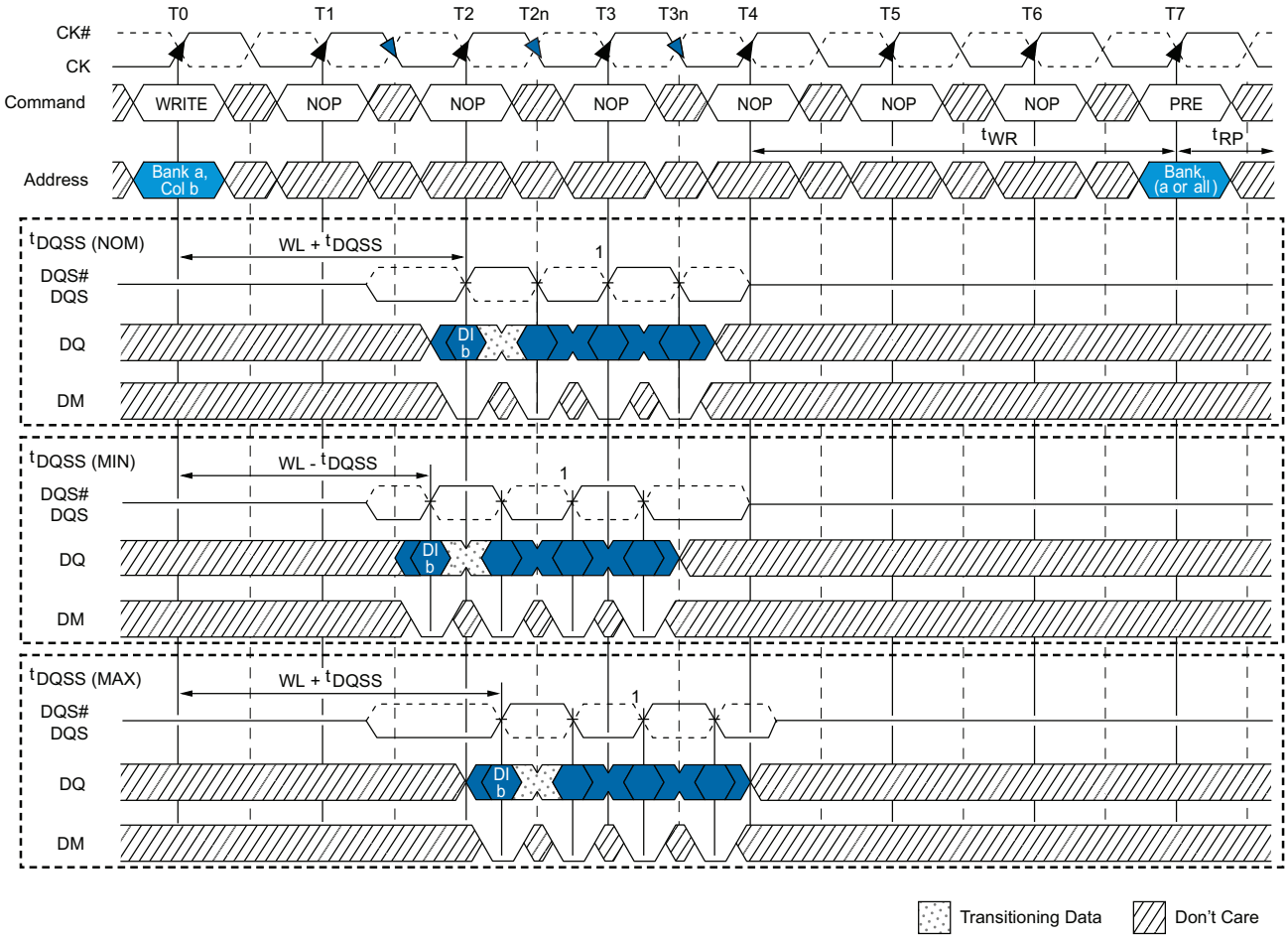
Notes:
1. BL = 8 required and auto precharge must be disabled (A10 = LOW).
2. The NOP or COMMAND INHIBIT commands are valid. The PRECHARGE command cannot be issued to banks used for WRITEs at T0 and T2.
3. The interrupting WRITE command must be issued exactly 2 × ^{t}CK from previous WRITE.
4. The earliest WRITE-to-PRECHARGE timing for WRITE at T0 is WL + BL/2 +^{t}WR where ^{t}WR starts with T7 and not T5 (because BL = 8 from MR and not the truncated length).
5. The WRITE command can be issued to any valid bank and row address (WRITE command at T0 and T2 can be either same bank or different bank).
6. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting WRITE command.
7. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
8. Example shown uses AL = 0; CL = 4, BL = 8.

Figure 54 - WRITE-to-READ



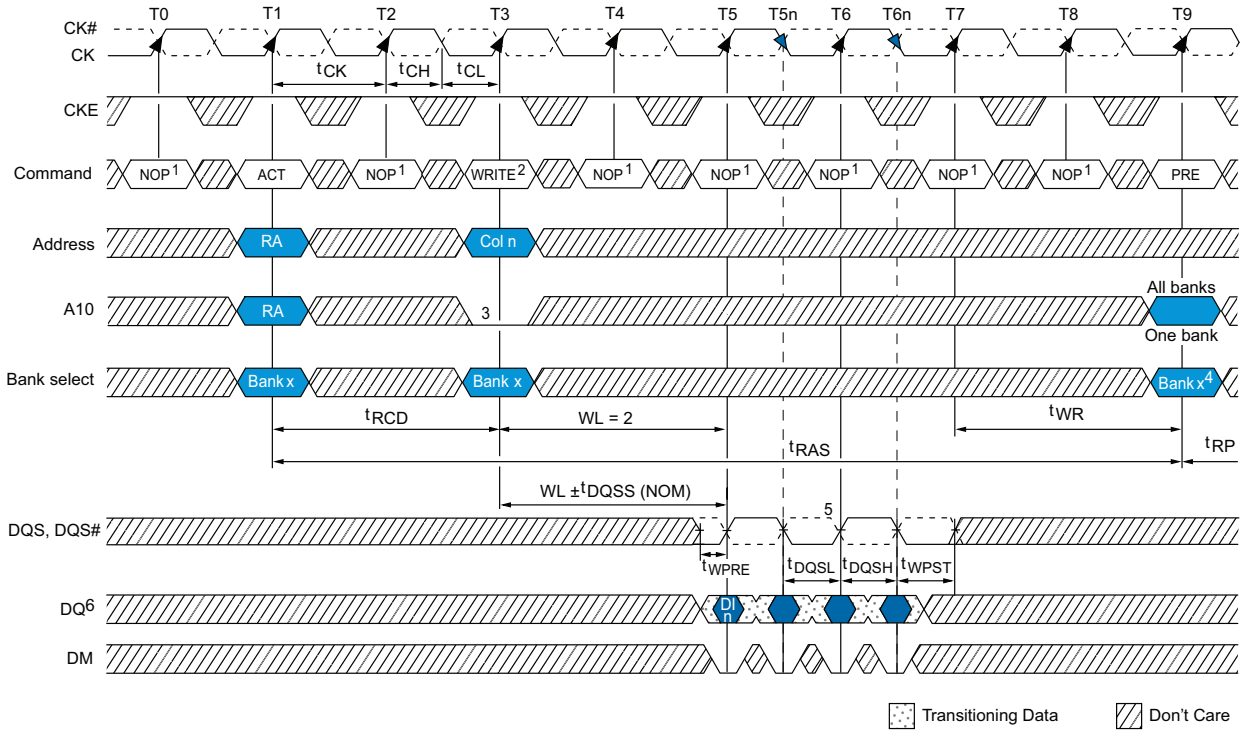
Notes:
1. tWTR is required for any READ following a WRITE to the same device, but it is not required between module ranks.
2. Subsequent rising DQS signals must align to the clock within tDQSS.
3. DI b = data-in for column b; DO n = data-out from column n.
4. BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. One subsequent element of data-in is applied in the programmed order following DI b.
6. tWTR is referenced from the first positive CK edge after the last data-in pair.
7. A10 is LOW with the WRITE command (auto precharge is disabled).
8. The number of clock cycles required to meet tWTR is either 2 or tWTR/tCK, whichever is greater.

Figure 55 - WRITE-to-PRECHARGE



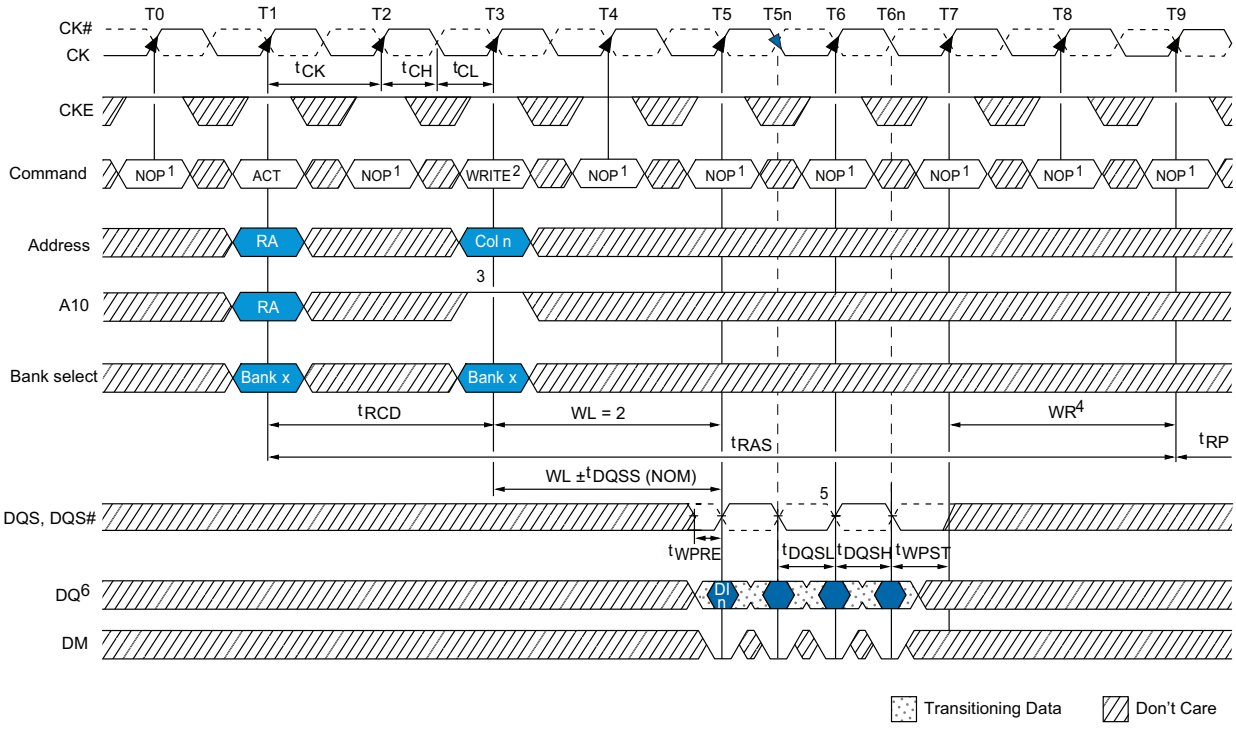
Notes:
1. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
2. DI b = data-in for column b.
3. Three subsequent elements of data-in are applied in the programmed order following DI b.
4. BL = 4, CL = 3, AL = 0; thus, WL = 2.
5. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
6. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
7. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 56 - Bank Write – Without Auto Precharge



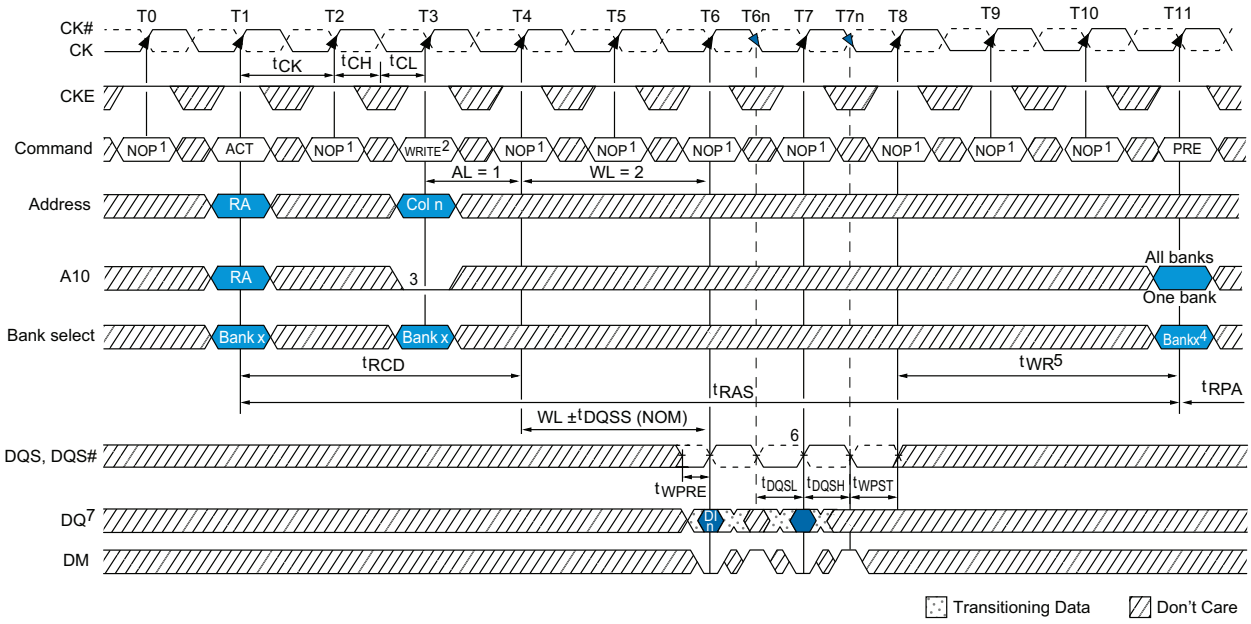
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T9.
5. Subsequent rising DQS signals must align to the clock within tDQSS.
6. DI n = data-in for column n; subsequent elements are applied in the programmed order.
7. tDSH is applicable during tDQSS (MIN) and is referenced from CK T5 or T6.
8. tDSS is applicable during tDQSS (MAX) and is referenced from CK T6 or T7.

Figure 57 - Bank Write – with Auto Precharge



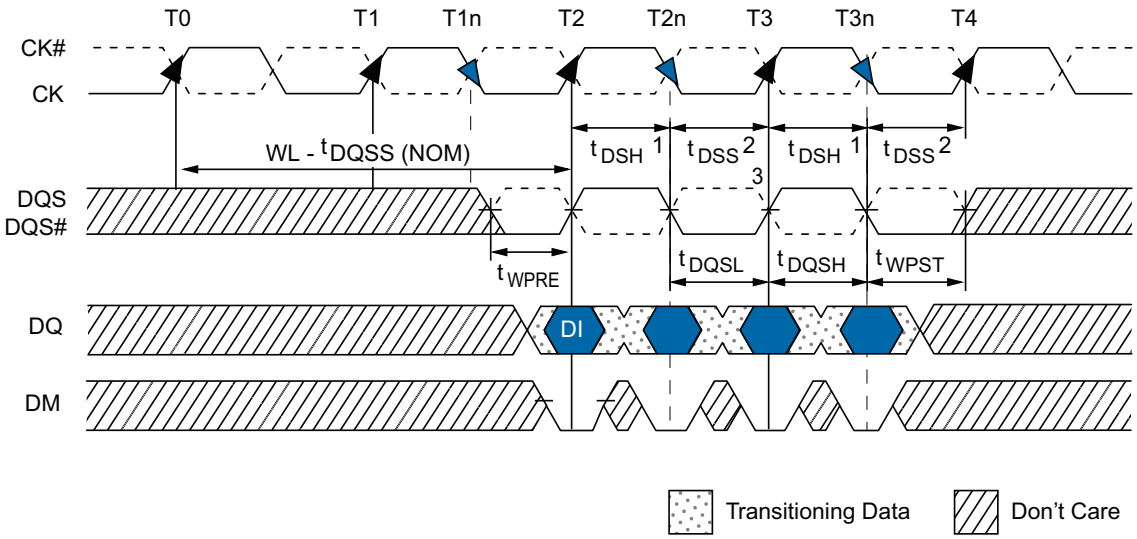
Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4 and AL = 0 in the case shown.
3. Enable auto precharge.
4. WR is programmed via MR9–MR11 and is calculated by dividing ^{t}WR (in ns) by ^{t}CK and rounding up to the next integer value.
5. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
6. DI n = data-in from column n; subsequent elements are applied in the programmed order.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.

Figure 58 - WRITE – DM Operation



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4, AL = 1, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T11.
5. ^{t}WR starts at the end of the data burst regardless of the data mask condition.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.
7. DI n = data-in for column n; subsequent elements are applied in the programmed order.
8. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T6 or T7.
9. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T7 or T8.

Figure 59 - Data Input Timing



Notes:
1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).
3. Subsequent rising DQS signals must align to the clock within tDQSS.
4. WRITE command issued at T0.
5. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
6. WRITE command with WL = 2 (CL = 3, AL = 0) issued at T0.

PRECHARGE

PRECHARGE can be initiated by either a manual PRECHARGE command or by an AUTO PRECHARGE in conjunction with either a READ or WRITE command. PRECHARGE will deactivate the open row in a particular bank or the open row in all banks. The PRECHARGE operation is shown in the previous READ and WRITE operation sections.

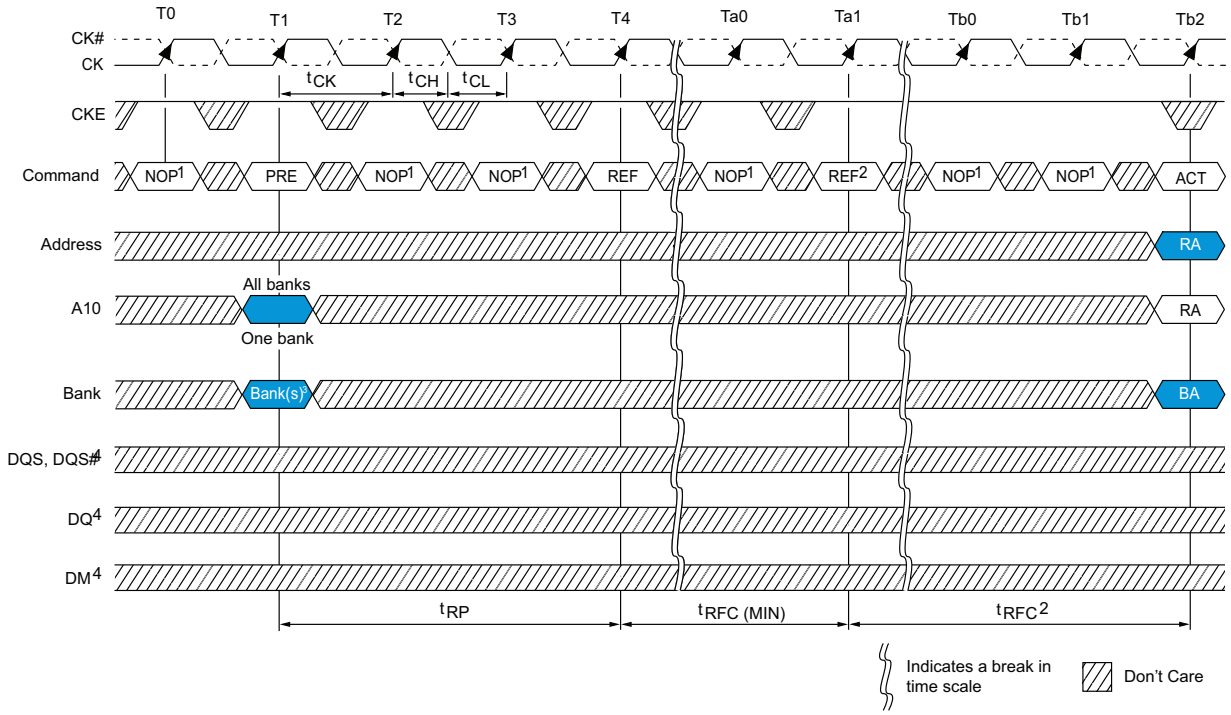
During a manual PRECHARGE command, the A_{10} input determines whether one or all banks are to be PRECHARGED. In the case where only one bank is to be precharged, bank address inputs determine the bank to be precharged. When all banks are to be precharged, the bank address inputs are treated as "Don't Care".

Once a bank has been PRECHARGED, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. When a single-bank PRECHARGE command is issued, tRP timing applies. When the PRECHARGE ALL command is issued, tRPA timing applies, regardless of the number of banks opened.

REFRESH

For Industrial temperature devices when TC is ≤ 85°C requires a REFRESH cycle at an average interval of 7.8125µS (MAX) and all rows in all banks must be refreshed at least once every 64ms. The REFRESH begins when the REFRESH command is registered and ends tRFC(MIN) later. The average interval must be reduced to 3.9µS(MAX) when TC is > 85°C.

Figure 60 - Refresh Mode

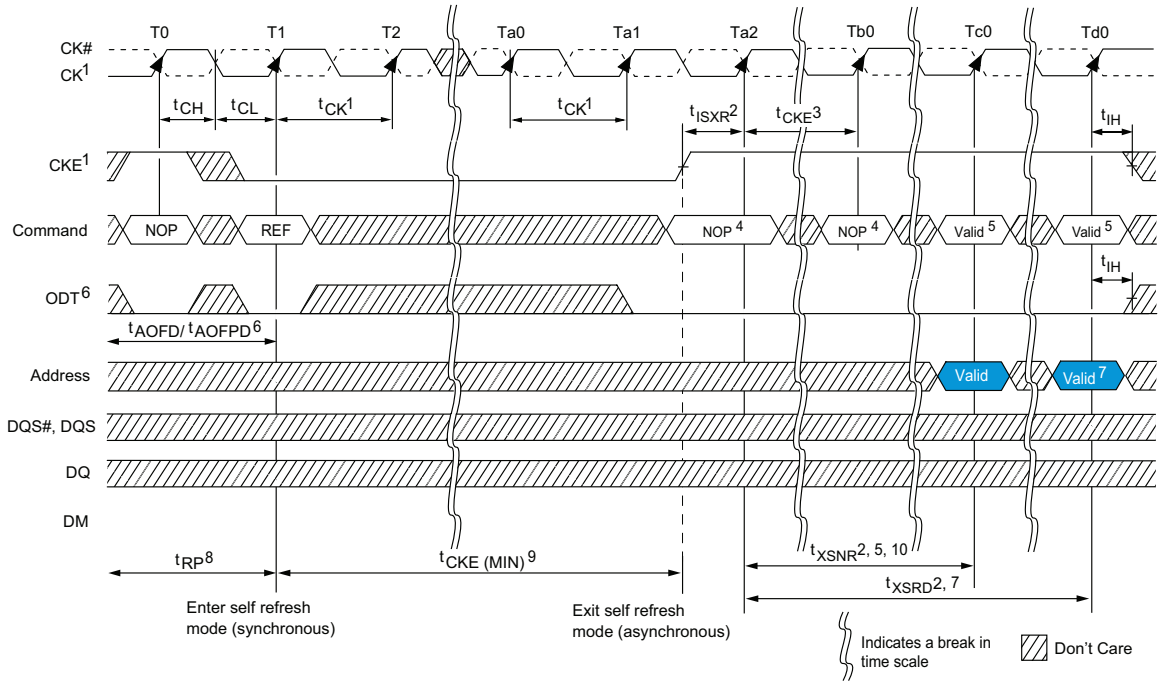


Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
2. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.
3. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.

SELF REFRESH

The SELF REFRESH command is initiated when CKE is low. The differential clock should remain stable and meet ^{t}CKE specifications at least 1 x ^{t}CK after entering SELF REFRESH mode. The procedure for exiting SELF REFRESH requires a sequence of commands. First, the differential clock must be stable and meet ^{t}CK specifications at least 1 x ^{t}CK prior to CKE going back to HIGH. Once CKE is HIGH (^{t}CKE[MIN] has been satisfied with three clock registrations), the module must have NOP or DESELECT commands issued for ^{t}XSNR. A simple algorithm for meeting both REFRESH and DLL requirements is used to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Figure 61 - Self Refresh



Notes:
1. Clock must be stable and meeting ^{t}CK specifications at least 1 × ^{t}CK after entering self refresh mode and at least 1 × ^{t}CK prior to exiting self refresh mode.
2. Self refresh exit is asynchronous; however, ^{t}XSNR and ^{t}XSRD timing starts at the first rising clock edge where CKE HIGH satisfies ^{t}ISXR.
3. CKE must stay HIGH until ^{t}XSRD is met; however, if self refresh is being re-entered, CKE may go back LOW after ^{t}XSNR is satisfied.
4. NOP or DESELECT commands are required prior to exiting self refresh until state Tc0, which allows any nonREAD command.
5. ^{t}XSNR is required before any nonREAD command can be applied.
6. ODT must be disabled and R_{TT} off (^{t}AOFD and ^{t}AOFPD have been satisfied) prior to entering self refresh at state T1.
7. ^{t}XSRD (200 cycles of CK) is required before a READ command can be applied at state Td0.
8. Device must be in the all banks idle state prior to entering self refresh mode.
9. After self refresh has been entered, ^{t}CKE (MIN) must be satisfied prior to exiting self refresh.
10. Upon exiting SELF REFRESH, ODT must remain LOW until ^{t}XSRD is satisfied.

POWER DOWN MODE

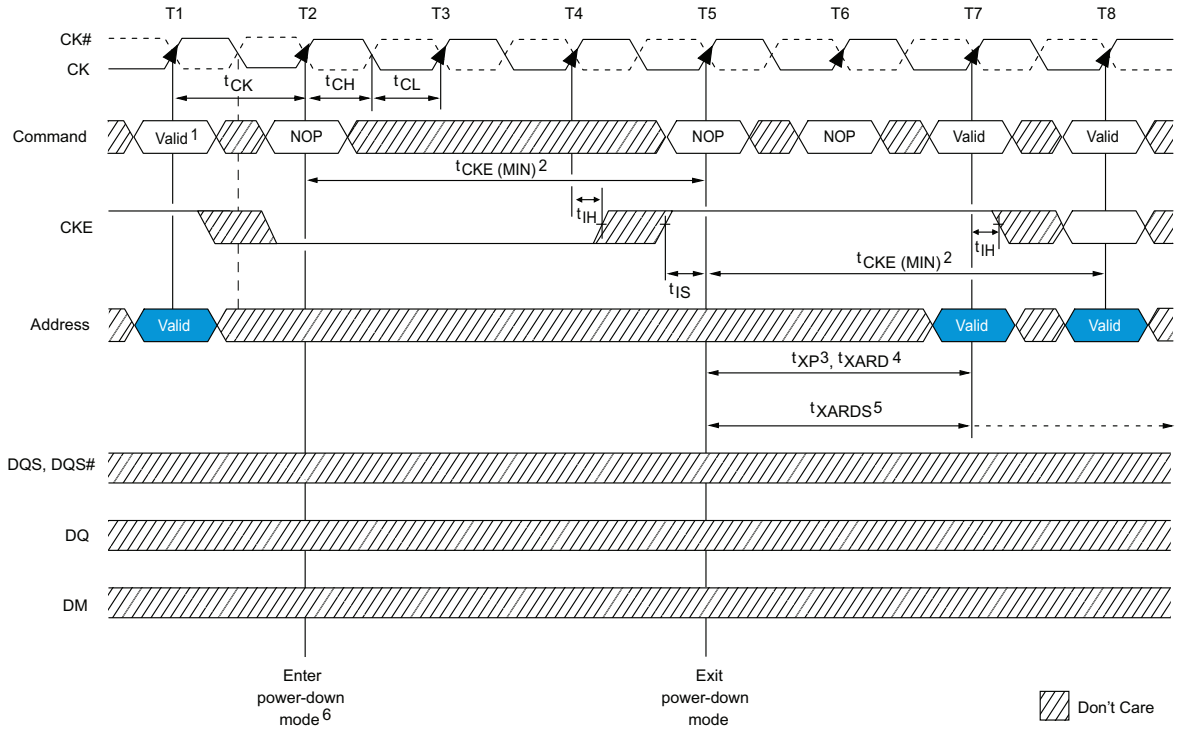
The module supports multiple POWER DOWN modes that allow significant power savings over normal operating modes. CKE is used to enter and exit different POWER DOWN modes. POWER DOWN entry and exit timings are shown in Figure 62. Detailed POWER DOWN entry conditions are shown in Figure 63. Table 41 is the CKE Truth Table. DDR2 iMOD device require CLE to be registered HIGH (active) at all times that an access is in progress from the issuing of a READ or WRITE command until completion of the burst. Thus, a clock suspend is not supported. For READs, a burst completion is defined when the READ postamble and ^{t}WR (WRITE-to- PRECHARGE command) or ^{t}WTR (WRITE-to-READ command) are satisfied, as shown in Figure 64, and Figure 65 or Figure 66. The number of clock cycles required to meet ^{t}WTR is either two or ^{t}WTR/tCK, whichever is greater.

POWER DOWN mode is entered when CKE is registered low coincident with an NOP or DESELECT command. CKE is not allowed to go LOW during a MODE REGISTER or EXTENDED MODE REGISTER command time, or while a READ or WRITE operation is in progress. If POWER DOWN occurs when all banks are idle, this mode is referred to as PRECHARGE POWER DOWN. If POWER DOWN occurs when there is a row active in any bank, this mode is referred to as ACTIVE POWER DOWN. Entering POWER DOWN deactivates the input and output buffers, excluding CK, CK\, ODT and CKE. For maximum power savings, the DLL is frozen during PRECHARGE POWER DOWN. Exiting ACTIVE POWER DOWN requires the device to be at same voltage and frequency as when it entered POWER DOWN, Exiting PRECHARGE POWER DOWN requires the device to be at the same voltage as when it entered POWER DOWN; however, the clock frequency is allowed to change.

The maximum duration for either ACTIVE or PRECHARGE POWER DOWN is limited by the REFRESH requirements of the devices ^{t}RFC(MAX). The minimum duration for POWER DOWN entry and exit is limited by the ^{t}CKE (MIN) parameter. The following must be maintained while in POWER DOWN mode; CKE LOW, a stable clock signal, a stable power supply signal at the inputs. All other input signals are “Don’t Care” except ODT.

The POWER DOWN state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command).

Figure 62 - Power-Down



Notes:

1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVATE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. tCKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 × tCK + tIH. CKE must not transition during its tIS and tIH window.
3. tXP timing is used for exit precharge power-down and active power-down to any non-READ command.
4. tXARD timing is used for exit active power-down to READ command if fast exit is selected via MR (bit 12 = 0).
5. tXARDS timing is used for exit active power-down to READ command if slow exit is selected via MR (bit 12 = 1).
6. No column accesses are allowed to be in progress at the time power-down is entered. If the DLL was not in a locked state when CKE went LOW, the DLL must be reset after exiting power-down mode for proper READ operation.

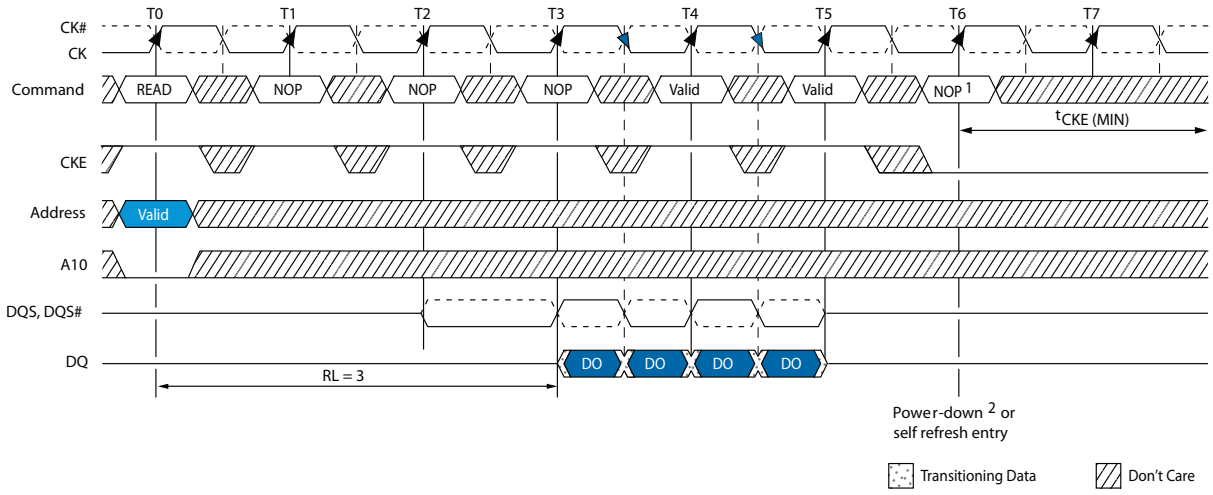
Table 41: Truth Table - CKE

Current State	CKE Prev. Cycle (n-1)	CKE Curr. Cycle (n)	COMMAND (n) CS\, RAS\, CAS\, WE\	Action (n)	Notes
POWER-DOWN	L	L	X	Maintain POWER-DOWN	1-6
	L	H	DESELECT OR NOP	POWER-DOWN exit	1-4,7,8
SELF REFRESH	L	L	X	Maintain SELF REFRESH	1-4,6
	L	H	DESELECT OR NOP	SELF-REFRESH exit	1-4,7,8,11,12
BANK(S) ACTIVE	H	L	DESELECT OR NOP	Active POWER-DOWN entry	1-4,7,8,11,12
ALL BANKS ACTIVE	H	L	DESELECT OR NOP	PRECHARGE POWER-DOWN entry	1-4,7,8,11
	H	L	REFRESH	SELF REFRESH entry	1-4,10,12,13
	H	H	Shown in Table 34		1-4,14

NOTES:

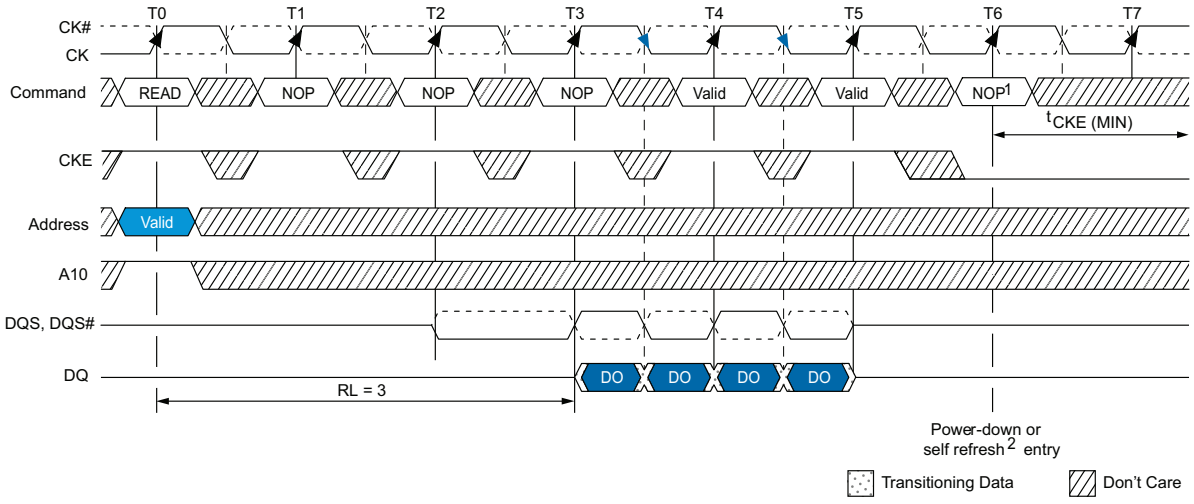
1. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge n.
3. Command (n) is the command registered at clock edge n, and action (n) is a result of command (n)
4. The state of ODT does not affect the states described in this table. The ODT function is not available during SELF REFRESH.
5. POWER-DOWN modes do not perform any REFRESH operations. The duration of POWER-DOWN mode is therefore limited by the REFRESH requirements
6. "X" means "DON'T CARE" (including floating around VREF) in SELF REFRESH and POWER-DOWN. However, ODT must be driven HIGH or LOW in POWER-DOWN if the ODT function is enabled via the EMR (extended mode register)
7. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
8. Valid commands for POWER-DOWN Entry and Exit are NOP and DESELECT Only.
9. On SELF REFRESH Exit, DESELECT or NOP commands must be issued on every clock edge occurring during the ^{t}XSNR period. READ commands may be issued only after ^{t}XSRD (200) clocks) is satisfied.
10. Valid commands for SELF REFRESH Exit are NOP and DESELECT only.
11. POWER-DOWN and SELF REFRESH can not be entered while READ or WRITE operations, LOAD MODE, or PRECHARGE operations are in progress. See SELF REFRESH for a list of restrictions.
12. Minimum CKE HIGH time is ^{t}CKE=3 x ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 x ^{t}CK. This requires a minimum of 3 clock cycles of registration.
13. SELF REFRESH mode can only be entered from the ALL BANKS idle state.
14. Must be a legal command, as defined in Table 34.

Figure 63 - READ-to-Power-Down or Self Refresh Entry



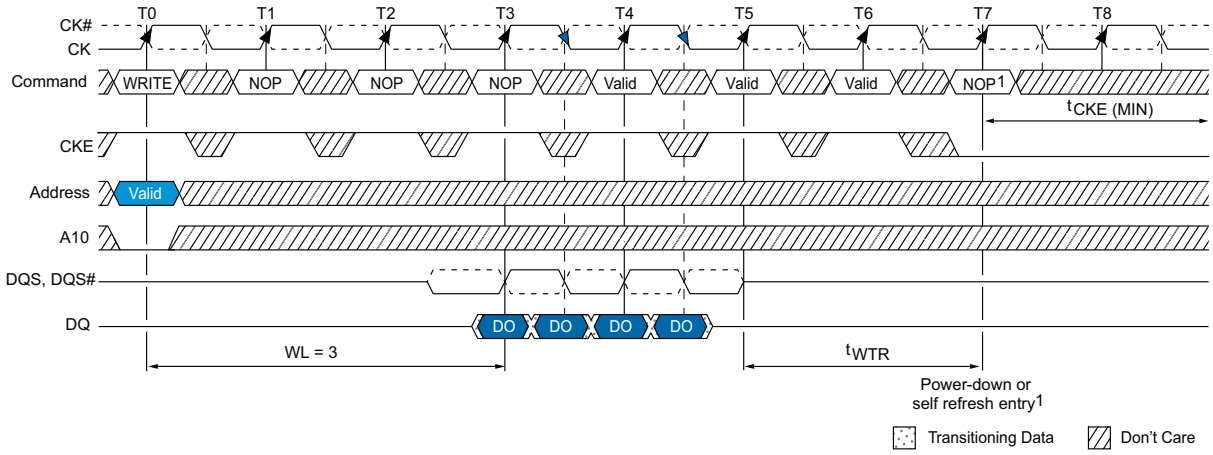
Notes:
1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

Figure 64 - READ with Auto Precharge-to-Power-Down or Self Refresh Entry



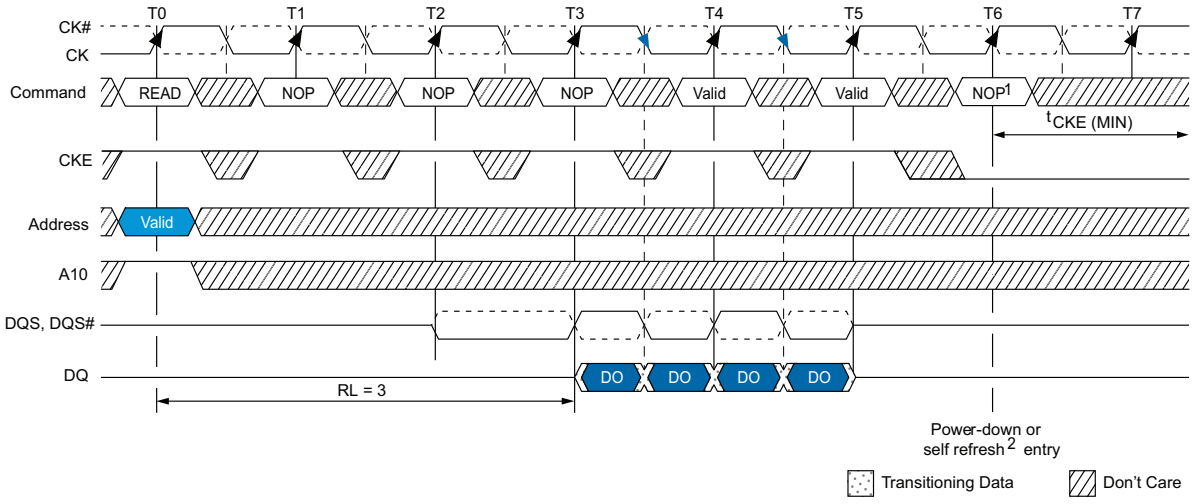
Notes:
1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

Figure 65 - WRITE-to-Power-Down or Self Refresh Entry



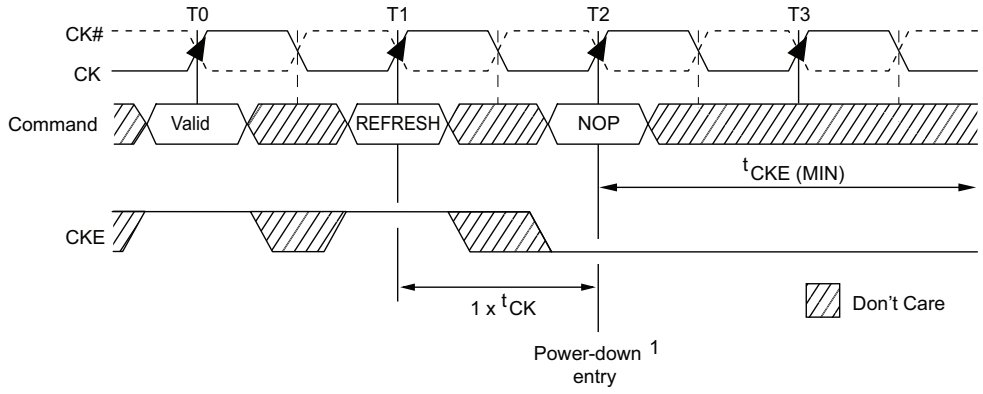
Note: 1. Power-down or self refresh entry may occur after the WRITE burst completes.

Figure 66 - WRITE with Auto Precharge-to-Power-Down or Self Refresh Entry



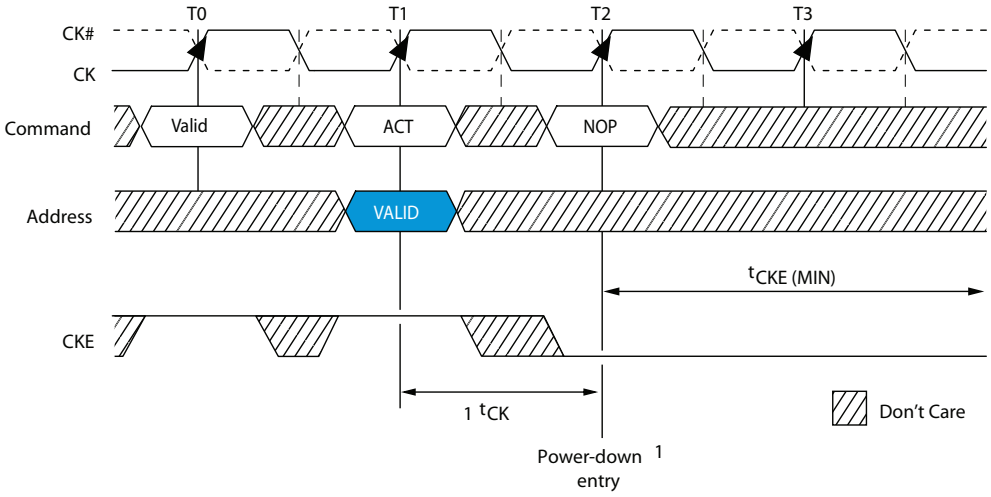
Notes:
1. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.
2. Power-down or self refresh entry may occur after the READ burst completes.

Figure 67 - REFRESH Command-to-Power-Down Entry



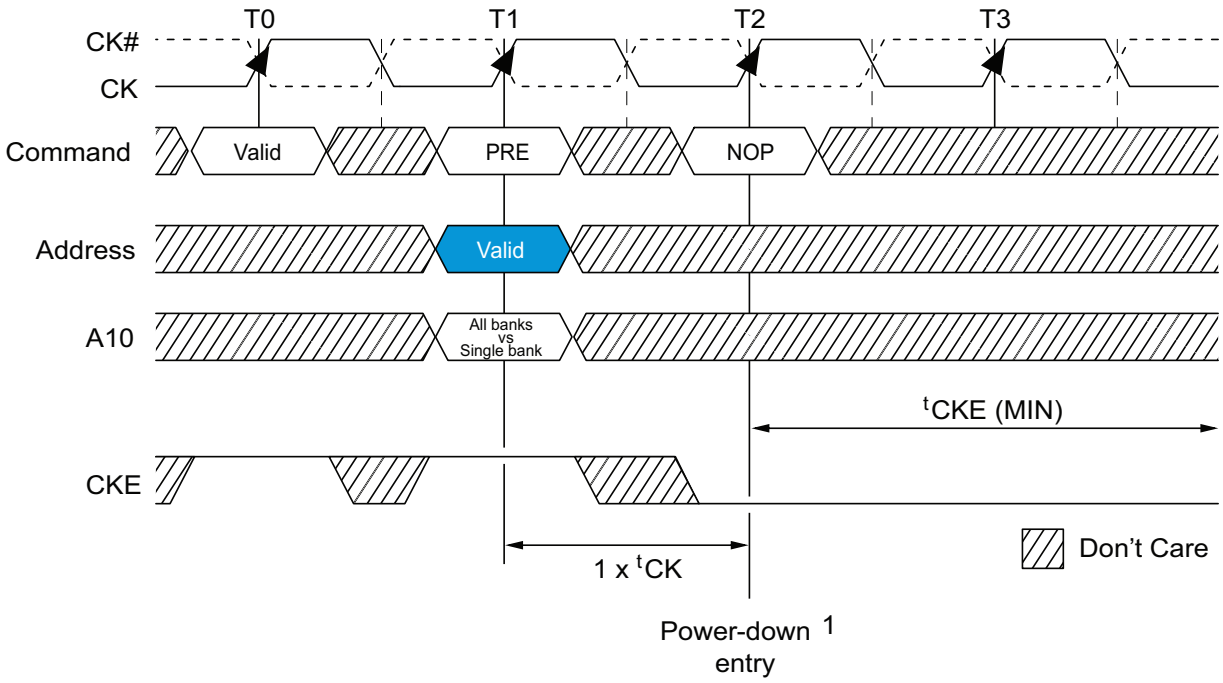
Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the REFRESH command. Precharge power-down entry occurs prior to ^{t}RFC (MIN) being satisfied.

Figure 68 - ACTIVATE Command-to-Power-Down Entry



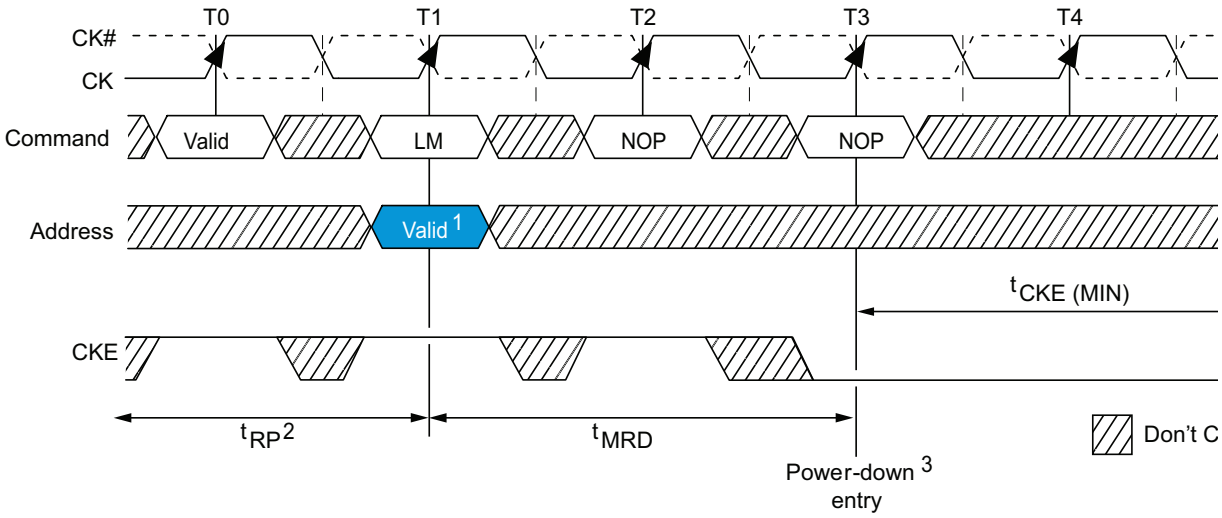
Note: 1. The earliest active power-down entry may occur is at T2, which is 1 × ^{t}CK after the ACTIVATE command. Active power-down entry occurs prior to ^{t}RCD (MIN) being satisfied.

Figure 69 - PRECHARGE Command-to-Power-Down Entry



Note: 1. The earliest precharge power-down entry may occur is at T2, which is 1 × ^{t}CK after the PRECHARGE command. Precharge power-down entry occurs prior to ^{t}RP (MIN) being satisfied.

Figure 70 - LOAD MODE Command-to-Power-Down Entry



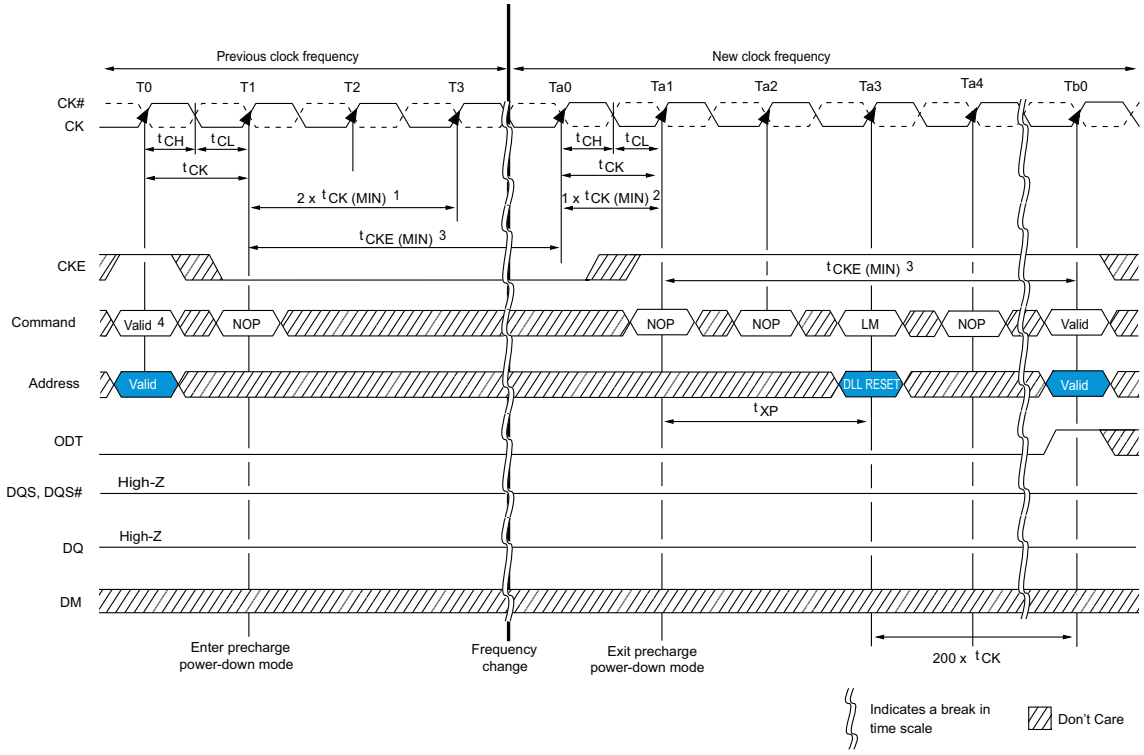
Notes:
1. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.
2. All banks must be in the precharged state and ^{t}RP met prior to issuing LM command.
3. The earliest precharge power-down entry is at T3, which is after ^{t}MRD is satisfied.

PRECHARGE POWER DOWN CLOCK FREQUENCY CHANGE

When the module is in PRECHARGE POWER DOWN mode, ODT must be turned off and CKE must be at a logic LOW level. A minimum of two differential clock cycles must pass after CKE goes LOW before clock frequency may change. The device input clock frequency is allowed to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input lock frequency change, ODT and CKE must be held stable LOW levels. When the input clock frequency is changed, new stable clocks must be provided to the device before PRECHARGE POWER DOWN may be exited and DLL must be reset via MR after PRECHARGE POWER DOWN exit. Depending on the new clock frequency, additional LM commands might be required to adjust the CL, WR, AL and so forth.

Depending on the new clock frequency, and additional LM command might be required to appropriately set the WR-MR9, MR10 and MR11. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL Lock time, the DDR2 is ready to operate with a new clock frequency.

FIGURE 71 - INPUT CLOCK FREQUENCY CHANGE DURING PRECHARGE POWER-DOWN MODE



Notes:
1. A minimum of 2 × ^{t}CK is required after entering precharge power-down prior to changing clock frequencies.
2. When the new clock frequency has changed and is stable, a minimum of 1 × ^{t}CK is required prior to exiting precharge power-down.

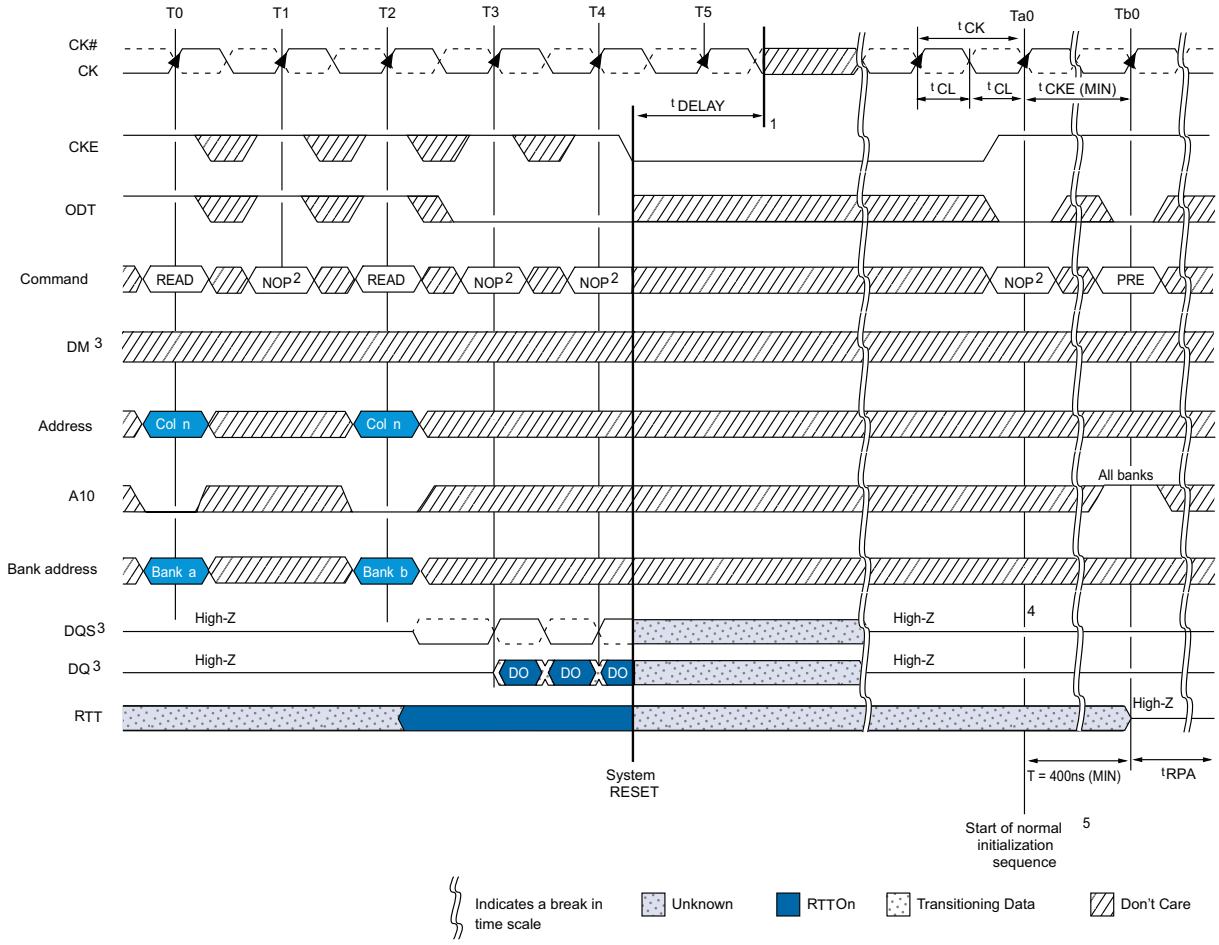
RESET

DDR2 applications may force a RESET state to the device anytime during normal operation. If an application or control block directs the device or array to enter RESET condition, CKE is used to ensure the device resumes normal operation after re-initialization. All data will be lost during a RESET condition; however, the DDR2 iMOD will continue to operate properly if the following conditions outlined in this section are satisfied.

The RESET condition defined here assumes all supply voltages (all supply voltages and VREF) are stable and meet all DC specification guidelines, prior to, during and after the RESET operation. All other inputs of the device are a "Don't Care" during RESET with the exception of CKE.

If CKE drops LOW asynchronously during any valid operation, (including a READ or WRITE burst) the memory controller must satisfy the timing parameter ^{t}DELAY, before turning off the clocks. Stable clocks must exist at the CK, CK\ inputs before CKE is driven HIGH, at which time the normal initialization sequence must occur. The device is now ready for normal operation after the initialization sequence. Figure 72 shows the proper sequence for a RESET operation.

Figure 72 - RESET Function



Notes:

1. VDD, VDDL, VDDQ, VTT, and VREF must be valid at all times.
2. Either NOP or DESELECT command may be applied.
3. DM represents DM for x4/x8 configuration and UDM, LDM for x16 configuration. DQS represents DQS, DQS#, UDQS, UDQS#, LDQS, LDQS#, RDQS, and RDQS# for the appropriate configuration (x4, x8, x16).
4. In certain cases where a READ cycle is interrupted, CKE going HIGH may result in the completion of the burst.
5. Initialization timing is shown in Figure 35.

ODT TIMING

Once a 12ns delay (^{t}MOD) has been satisfied, and after the ODT function has been enabled via the EMR LOAD MODE command, ODT can be accessed under two timing categories. ODT will operate either in synchronous mode or asynchronous mode, depending on the state of CKE. ODT can switch anytime except during self REFRESH mode and a few clocks after being enabled via the EMR, as shown in Figure 73.

There are two timing categories for ODT, TURN ON and TURN OFF. During active mode (CKE HIGH) and fast exit POWER DOWN mode (any row of any bank open, CKE LOW, MR[12=0]), ^{t}AOND, ^{t}AON, ^{t}AOFD and ^{t}AOF timing parameters are applied, as shown in Figure 74.

During slow exit POWER DOWN mode and PRECHARGE POWER DOWN mode, tAONPD and tAOFPD timing parameters are applied, as shown in Figure 75.

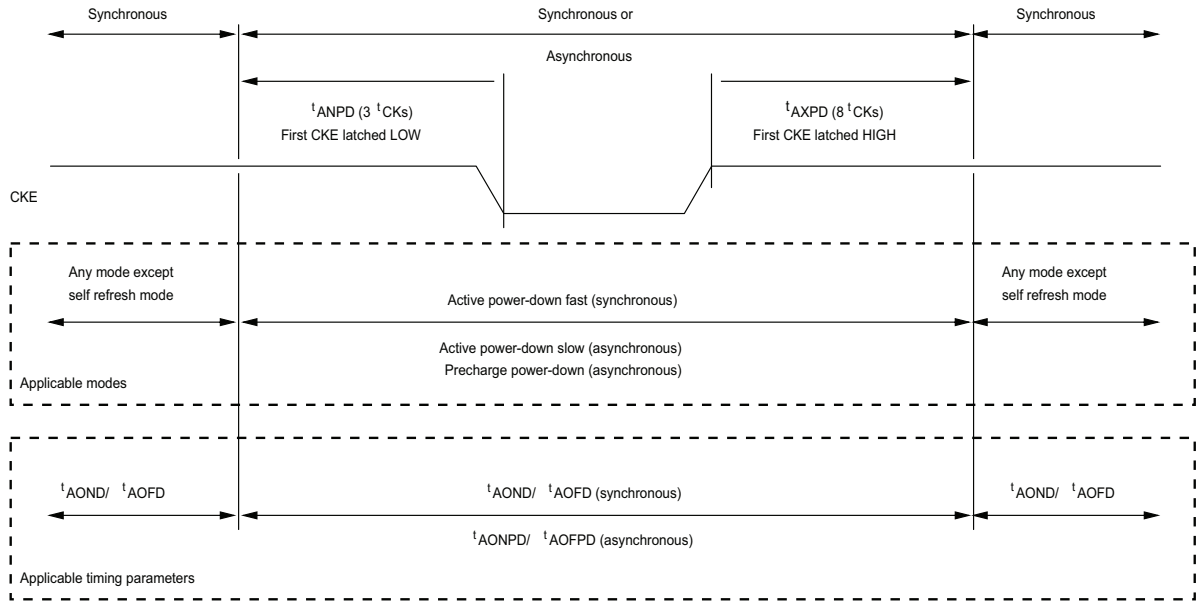
ODT turn-off timing, prior to entering any POWER DOWN mode, is determined by the parameter ^{t}ANPD(MIN), as shown in Figure 76. At state T_2, the ODT HIGH signal satisfies tANPD(MIN) prior to entering POWER DOWN mode at T_5. When ^{t}ANPD(MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 76 also shows the example where ^{t}ANPD(MIN) is NOT satisfied, because ODT HIGH does not occur until state T_3. When ^{t}ANPD(MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

ODT turn-on timing, prior to entering any POWER DOWN mode, is determined by the parameter ^{t}ANPD(MIN), as shown in Figure 77. At state T_2, the ODT HIGH signal satisfies ^{t}ANPD(MIN) prior to entering POWER DOWN mode at T_5. When ^{t}ANPD(MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 77 also shows the example where ^{t}ANPD(MIN) is NOT satisfied because ODT HIGH does not occur until state T_3. When ^{t}ANPD(MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

ODT turn-off timing after exiting any POWER DOWN mode is determined by the parameter ^{t}AXPD(MIN), as shown in Figure 78. At state Ta_1, the ODT LOW signal satisfies ^{t}AXPD(MIN) after exiting POWER DOWN mode at stat T_1. When ^{t}AXPD(MIN) is satisfied, ^{t}AOPD and ^{t}AOF timing parameters apply. Figure 78 also shows the example where ^{t}AXPD(MIN) is NOT satisfied because ODT LOW occurs at state Ta_0. When ^{t}AXPD(MIN) is NOT satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing after exiting either slow-exit POWER DOWN mode or PRECHARGE POWER DOWN mode is determined by the parameter ^{t}AXPD(MIN), as shown in Figure 79. At state Ta_1, the ODT HIGH signal satisfies ^{t}AXPD(MIN) after exiting POWER DOWN mode at state T_1. When ^{t}AXPD(MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 79 also shows the example where ^{t}AXPD(MIN) is NOT satisfied because ODT HIGH occurs at Ta_0. When ^{t}AXPD(MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

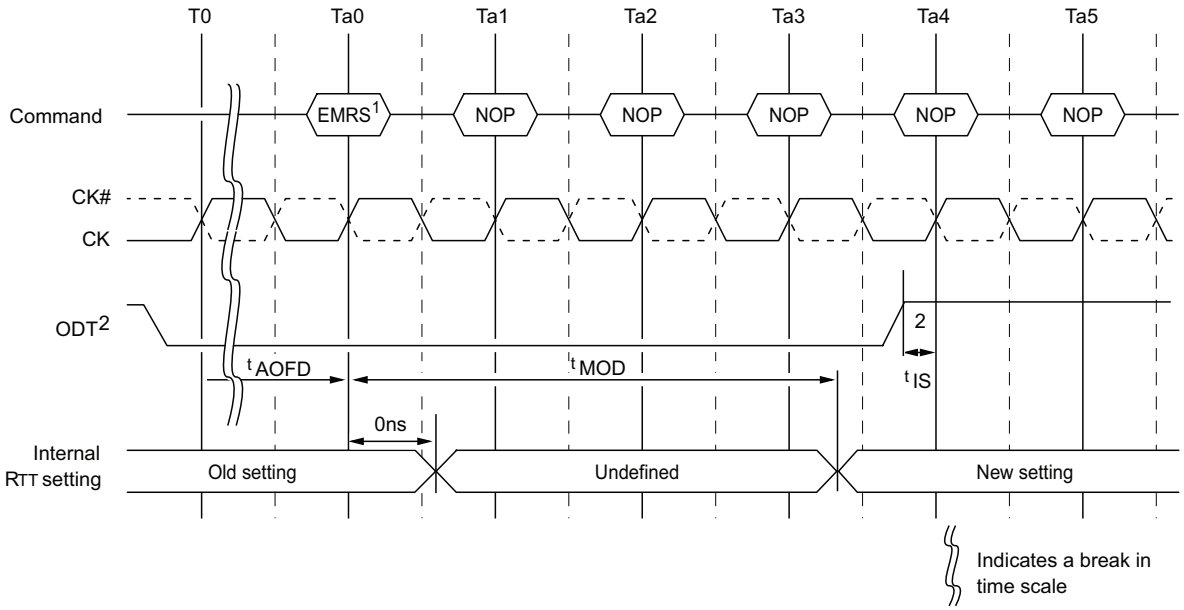
FIGURE 73 - ODT TIMING FOR ENTERING AND EXITING POWER-DOWN MODE



MRS COMMAND TO ODT UPDATE DELAY

During normal operation, the value of the effective termination resistance can be changed with an EMRS set command. ^{t}MOD(MAX) updates the RTT setting.

Figure 74 - Timing for MRS Command to ODT Update Delay



Notes:

1. The LM command is directed to the mode register, which updates the information in EMR (A6, A2), that is, R_{TT} (nominal).
2. To prevent any impedance glitch on the channel, the following conditions must be met: ^{t}AOFD must be met before issuing the LM command; ODT must remain LOW for the entire duration of the ^{t}MOD window until ^{t}MOD is met.

Figure 75 - ODT Timing for Active or Fast-Exit Power-Down Mode

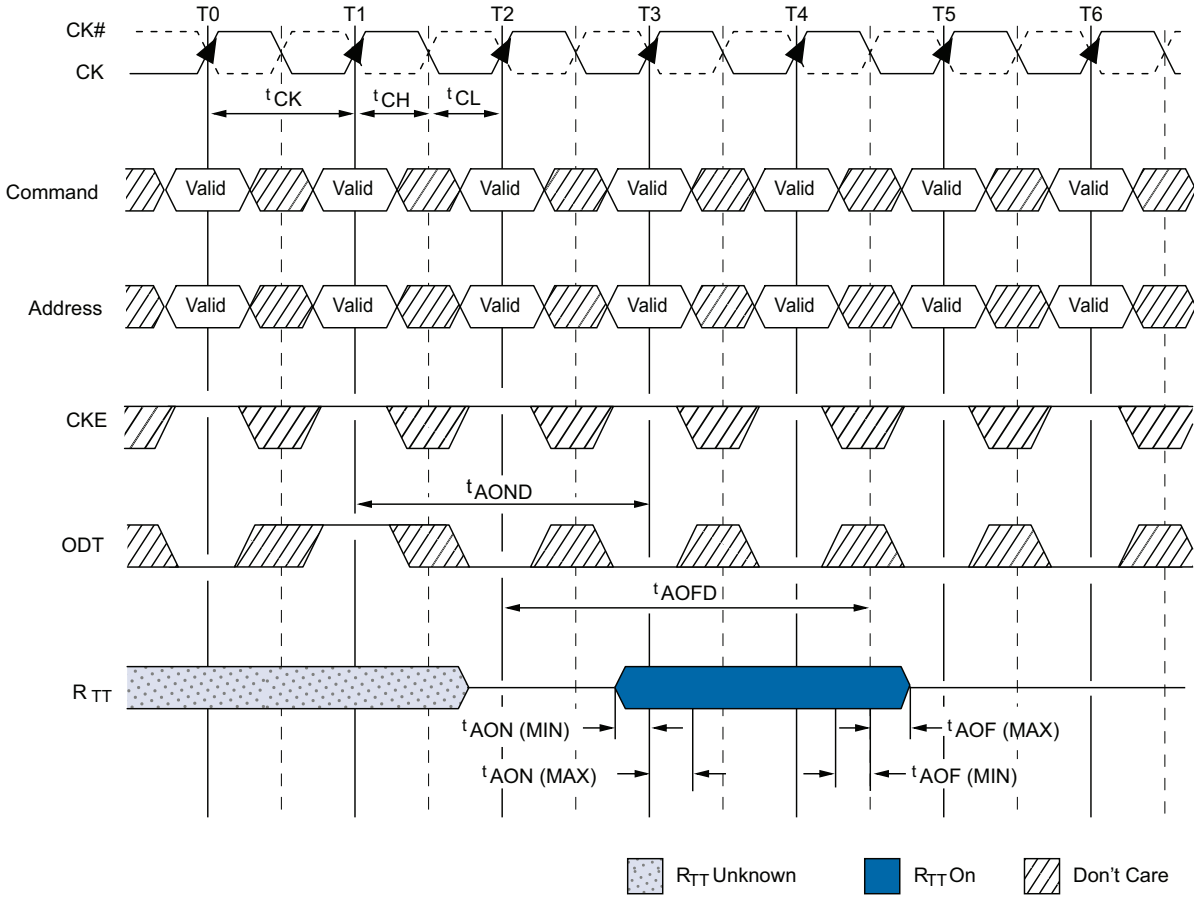


Figure 76 - ODT Timing for Slow-Exit or Precharge Power-Down Modes

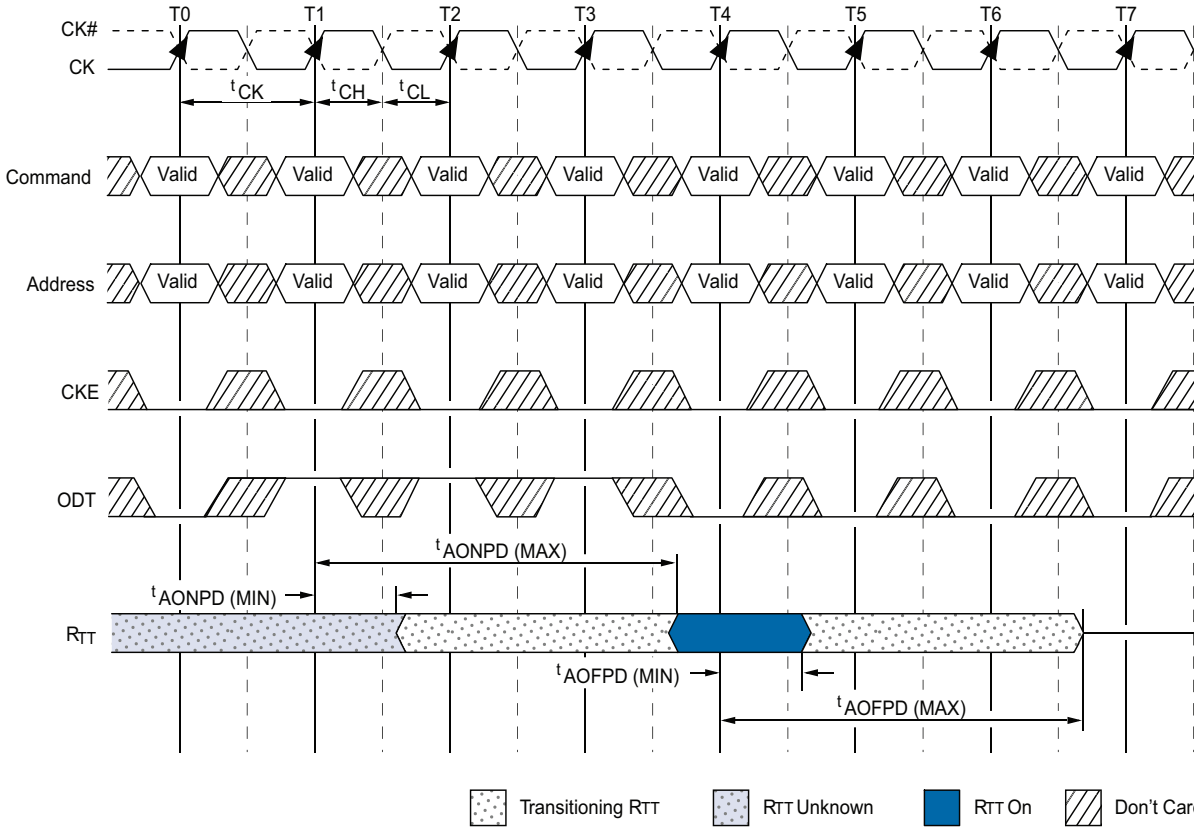


Figure 77 - ODT Turn-Off Timings When Entering Power-Down Mode

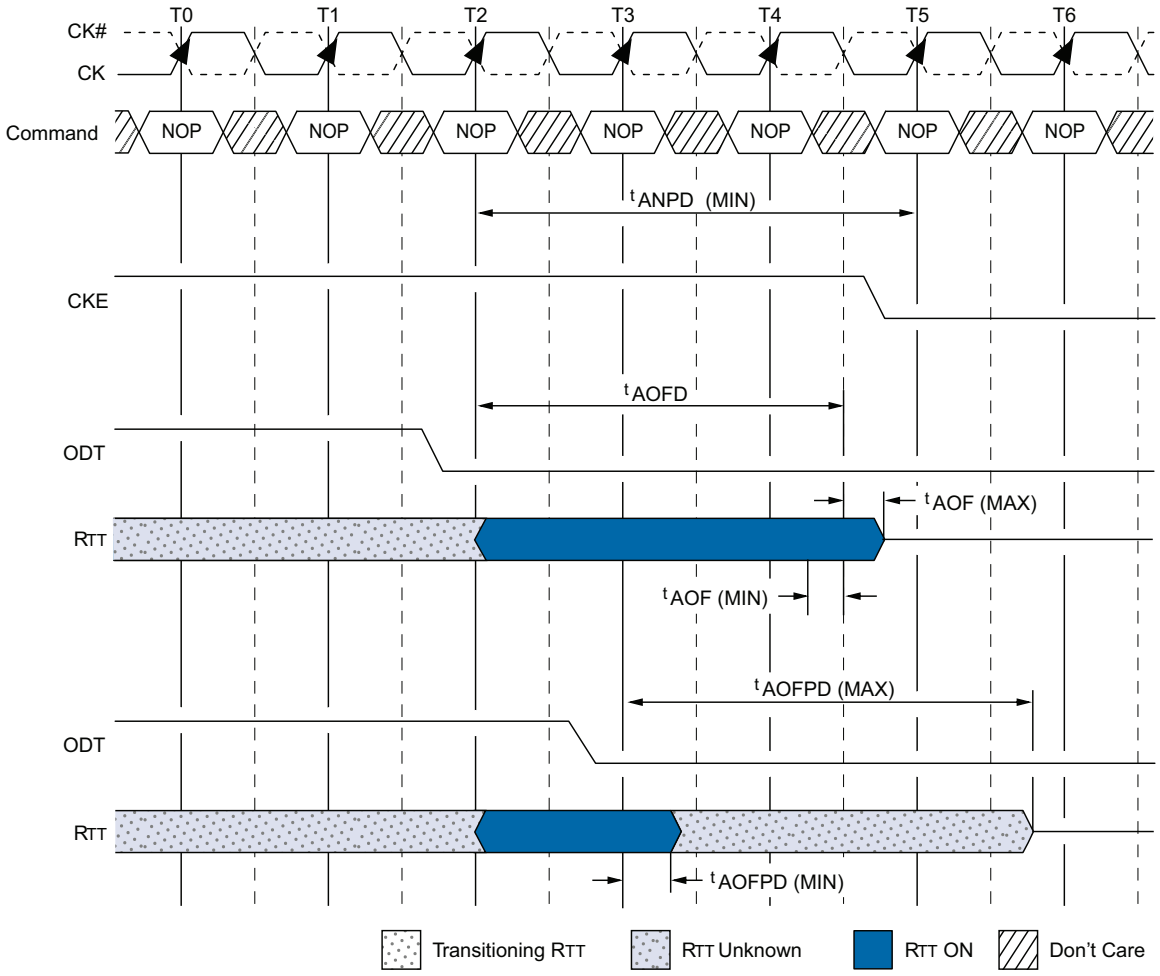


Figure 78 - ODT Turn-On Timing When Entering Power-Down Mode

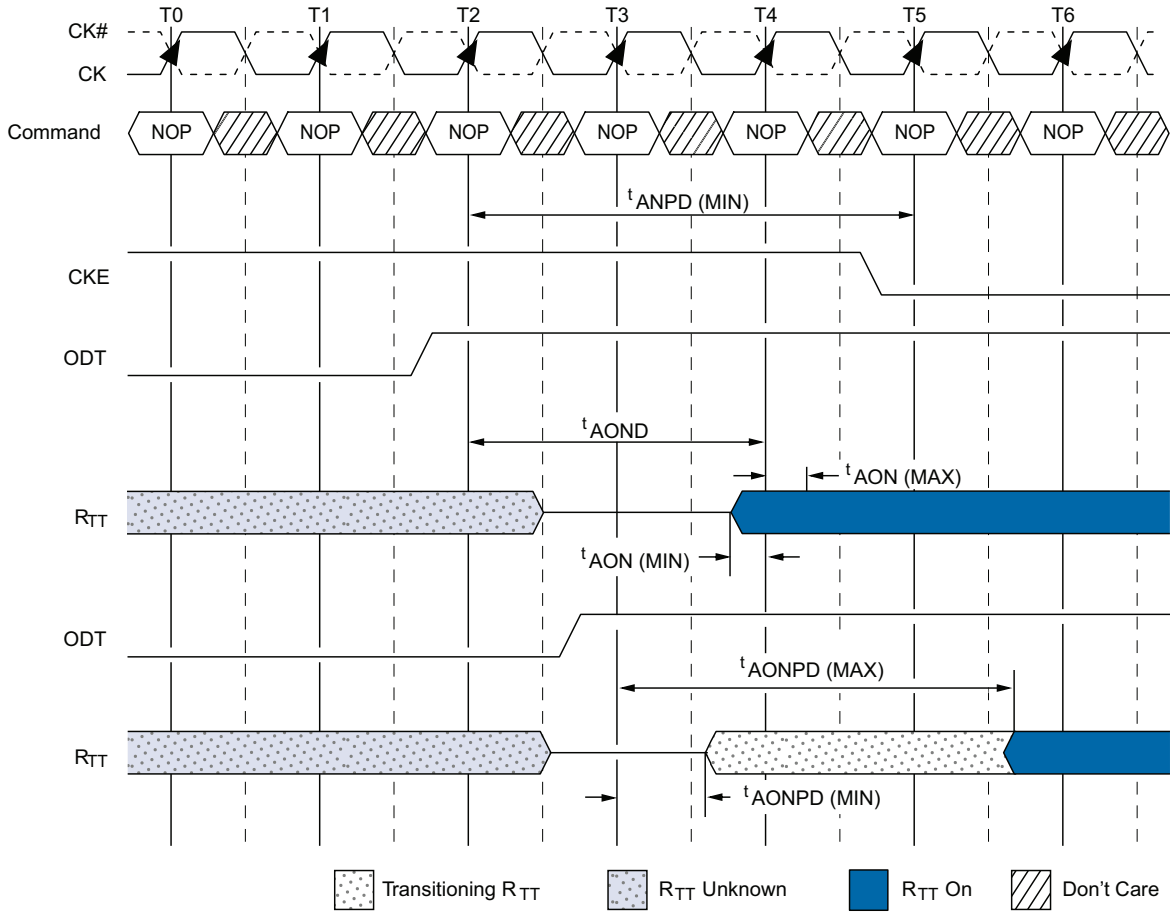
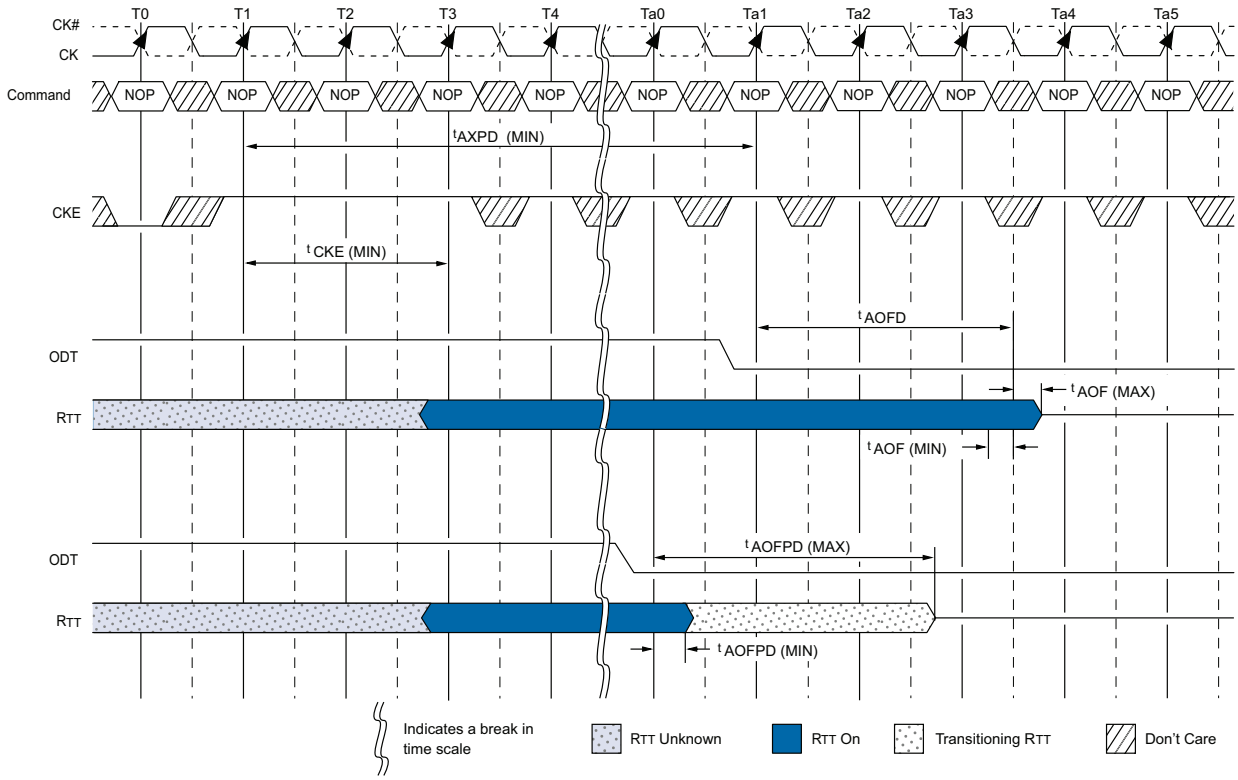


Figure 79 - ODT Turn-Off Timing When Exiting Power-Down Mode



Revision History

Revision	By	Issue Date	Description Of Change
A	BV	6/24//2015	INITIATE