High Speed Highly Integrated 4GB DDR4 Memory Module

FEATURES

- Wide Word DD4 SDRAM Module
- Configurations:
- – 64Meg x 32 x 8 banks x 2 Channels
- – 64Meg x 72 x 8 banks x 1 Channels
- – 64Meg x 40 x 8 banks x 2 Channels
- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV/+250mV
- On-chip, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C of 0°C to 95°C; Extended Temps Available
  – 64ms, 8192-cycle refresh at 0°C to 85°C
  – 32ms between 85°C to 95°C
  – 16ms between 95°C to 105°C
  – 8ms between 105°C to 125°C
- 8 internal banks: 2 groups of 4 banks each
- 8n-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination
- (ODT)
- Data bus inversion (DBI) for databus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79 compliant

SPEED GRADES[1] — Marking

- FBGA package (Pb-free)
  – 321-ball 15mm x 20mm
  - 0.8mm pitch
- Timing – cycle time[1]
  – 0.625ns @ CL = 22 (DDR4-3200) -062
  – 0.682ns @ CL = 20 (DDR4-2933) -068
  – 0.750ns @ CL = 19 (DDR4-2666) -75
  – 0.833ns @ CL = 17 (DDR4-2400) -083
  – 0.937ns @ CL = 16 (DDR4-2133) -093
  – 1.071ns @ CL = 13 (DDR4-1866) -107
- Operating temperature
  – Commercial (0° ≤ T_C ≤ 95°C) None

Note 1. Limited availability on some options. Consult factory before ordering.

High Performance Highly Integrated Module

Features

Table 1: Key Timing Parameters

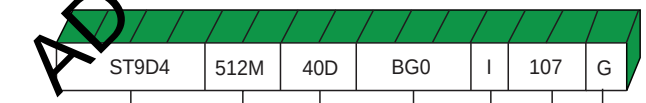
Speed Grade	Data Rate (MT/s)	Target ^{t}RCD- ^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-062 [6]	3200	22-22-22	13.75	13.75	13.75
-068 [5]	2933	21-21-21	14.32	14.32	14.32
-075 [4]	2666	19-19-19	14.25	14.25	14.25
-083 [3]	2400	17-17-17	14.16	14.16	14.16
-093 [2]	2133	16-16-16	15	15	15
-107 [1]	1866	13-13-13	13.92	13.92	13.92

Notes:
1. Backward compatible to 1600, CL = 11.
2. Backward compatible to 1600, CL = 11 and 1866, CL = 13.
3. Backward compatible to 1600, CL = 11; 1866, CL = 13; and 2133, CL = 15.
4. Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; and 2400, CL = 17. Limited availability.
   Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; and 2666, CL = 19.
5. Limited availability.
   Backward compatible to 1600, CL = 11; 1866, CL = 13; 2133, CL = 15; 2400, CL = 17; 2666, CL = 19; and 2933,
6. CL = 20 and CL = 21. Limited availability.

Table 2: Addressing

Parameter	512 Meg x 32(40)
Number of bank groups	2
Bank group address	BG0
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	64K (A[15:0])
Column addressing	1K (A[9:0])
Page size	2KB

Figure 1 - Part Numbers



DDR4 HiMOD

Word = 512MB

PBGA
15 X 20 mm

Wordwidth
x40
S = Single Channel
D = Dual Channel

Code	Solder Finish
	Leaded
G	Green

Code	Speed Grade
107	1.07ns / 1866 Mbps
093	0.93ns / 2133 Mbps
083	0.83ns / 2400 Mbps
075	0.75ns / 2666 Mbs
068	0.68ns / 2933 Mbs
062	0.62ns / 3200 Mbs

Example: ST9D4512M40DBG0I125

Note: Not all options can be combined.
Contact Sales for available offerings.

Temperature	Code
Commercial (0°C to 70°C)	C
Industrial (-40°C to 85°C)	I
Extended (-40°C to 105°C)	E
Military (-55°C to 125°C)	M

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Description

This DDR4 SDRAM Module is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The module uses an 8*n*-prefetch architecture to achieve high-speed operation. The 8*n*-prefetch architecture is combined with an interface to transfer two data words per clock cycle at the I/O pins.

A single READ or WRITE operation for the DDR4 SDRAM consists of a single 8*n*-bit wide, four-clock data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins. on page

Extended Temperatures

Industrial temperature (IT) device operation requires that the case temperature not exceed below –40°C or above 95°C. JEDEC specifications require the refresh rate to double when TC exceeds 85°C; this also requires use of the high-temperature self refresh option. Above 95°C the required refresh rate requirement again doubles. Additionally, ODT resistance and the input/output impedance must be derated when operating outside of the commercial temperature range, when T$_J$ is between -40°C and 70°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL enabled mode of operation (normal operation), unless stated otherwise.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ
- term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
- The terms “_t” and “_c” are used to represent the true and complement of a differential signal pair.
- The term “_n” is used to represent a signal that is active LOW.
- The terms “DQS” and “CK” found throughout the data sheet are to be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise.
- Any specific requirement takes precedence over a general statement.
  Any functionality not specifically stated is considered undefined, and not supported, and may result in unknown operation.
- Addressing is denoted as BG[*n*] for bank group, BA[*n*] for bank address, and A[*n*] for row/col address.
- The NOP command is only allowed when exiting maximum power savings mode or when entering gear-down mode, and only a DES command should be used.
- Not all specifications listed are finalized industry standards; best estimates are provided when an industry standard has not been finalized.
- The Module must reach a stable V_{DD} level and CKE must be toggled at least once every 8192 × ^{t}REFI for proper operation. In the event CKE is tied HIGH, toggling CS_n at least once every 8192 × ^{t}REFI is an acceptable alternative. Placing the DRAM into self refresh alleviates the need to toggle CKE.

Figure 2: ST9D4512M32DBG0 Equivalent Functional Diagram

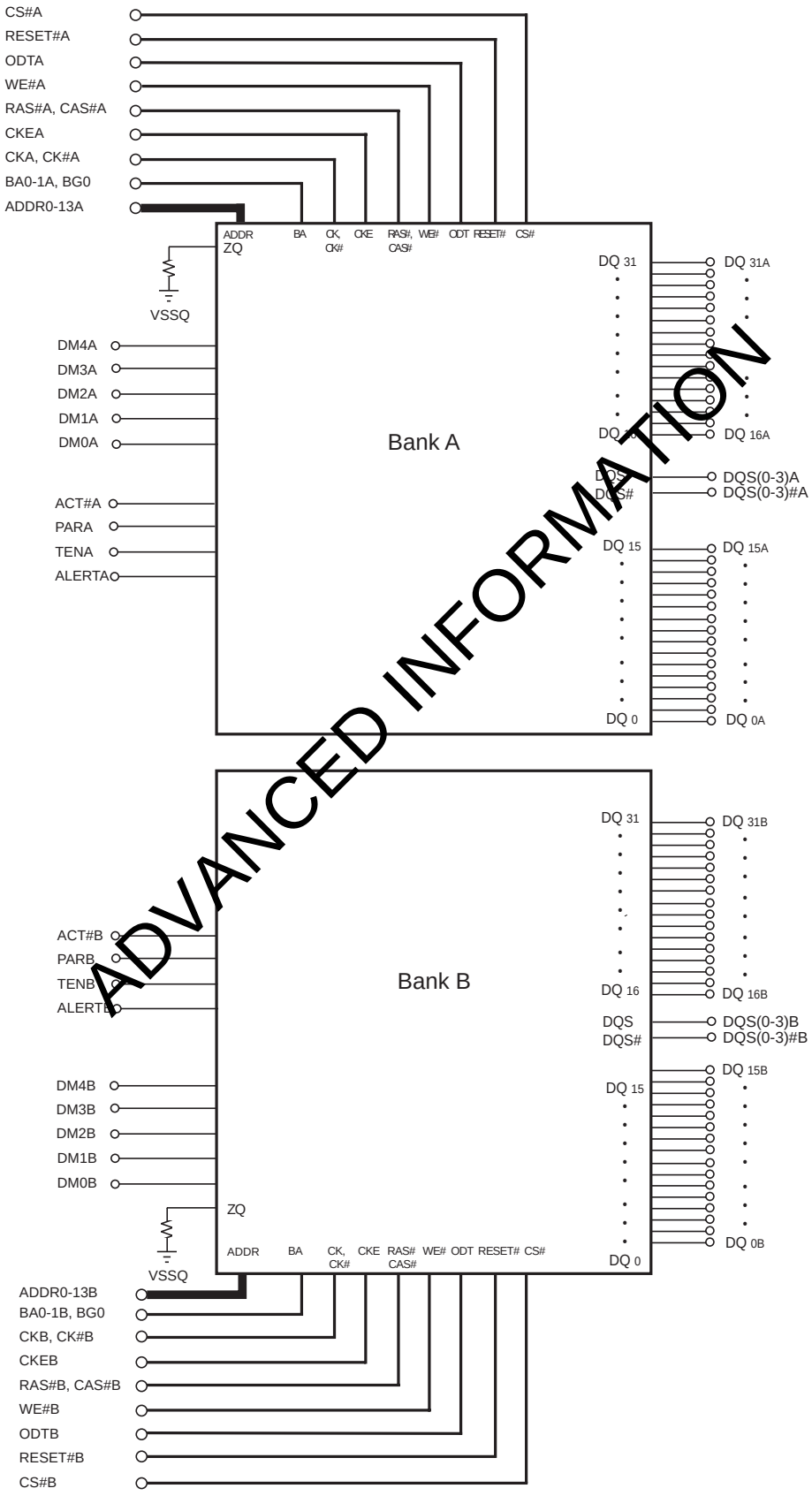


FIGURE 3: ST9D4512M72SBG0 EQUIVALENT FUNCTIONAL DIAGRAM

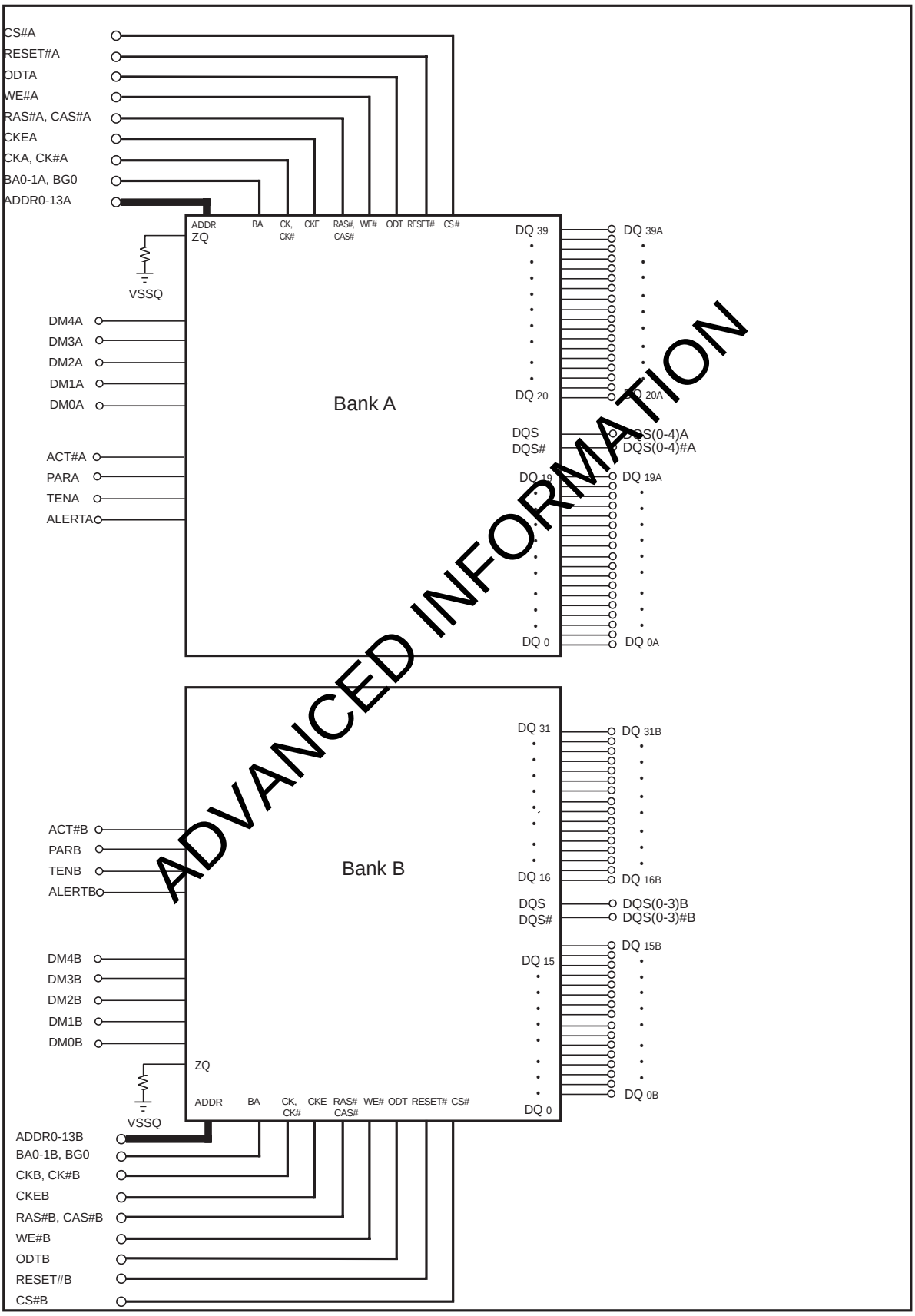


Figure 4: ST9D4512M40DBG0 Equivalent Functional Diagram

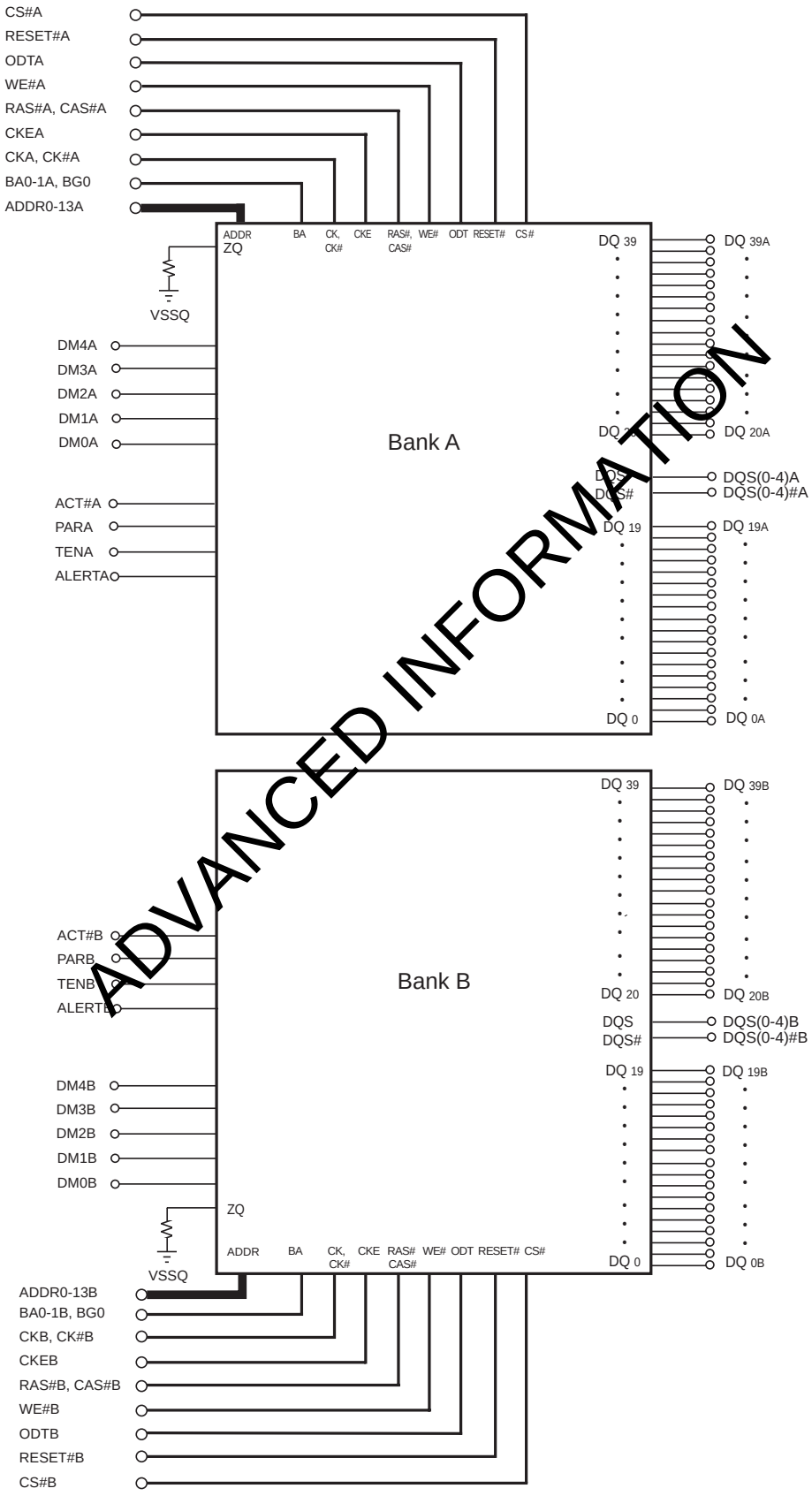


Figure 5: ST9D4512M32DBG0 Detailed Electrical Diagram

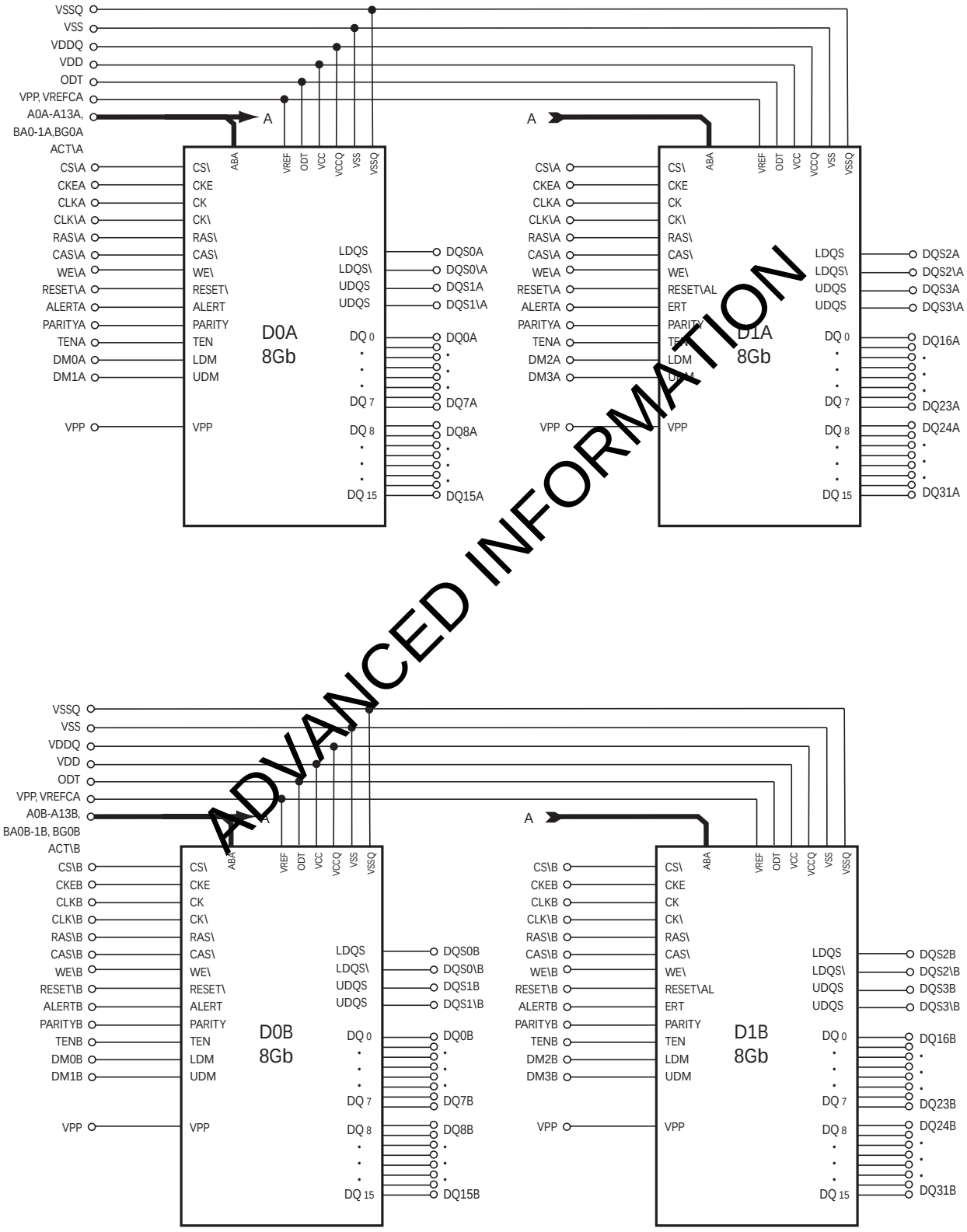


Figure 6: ST9D4512M72SBG0 Detailed Electrical Diagram

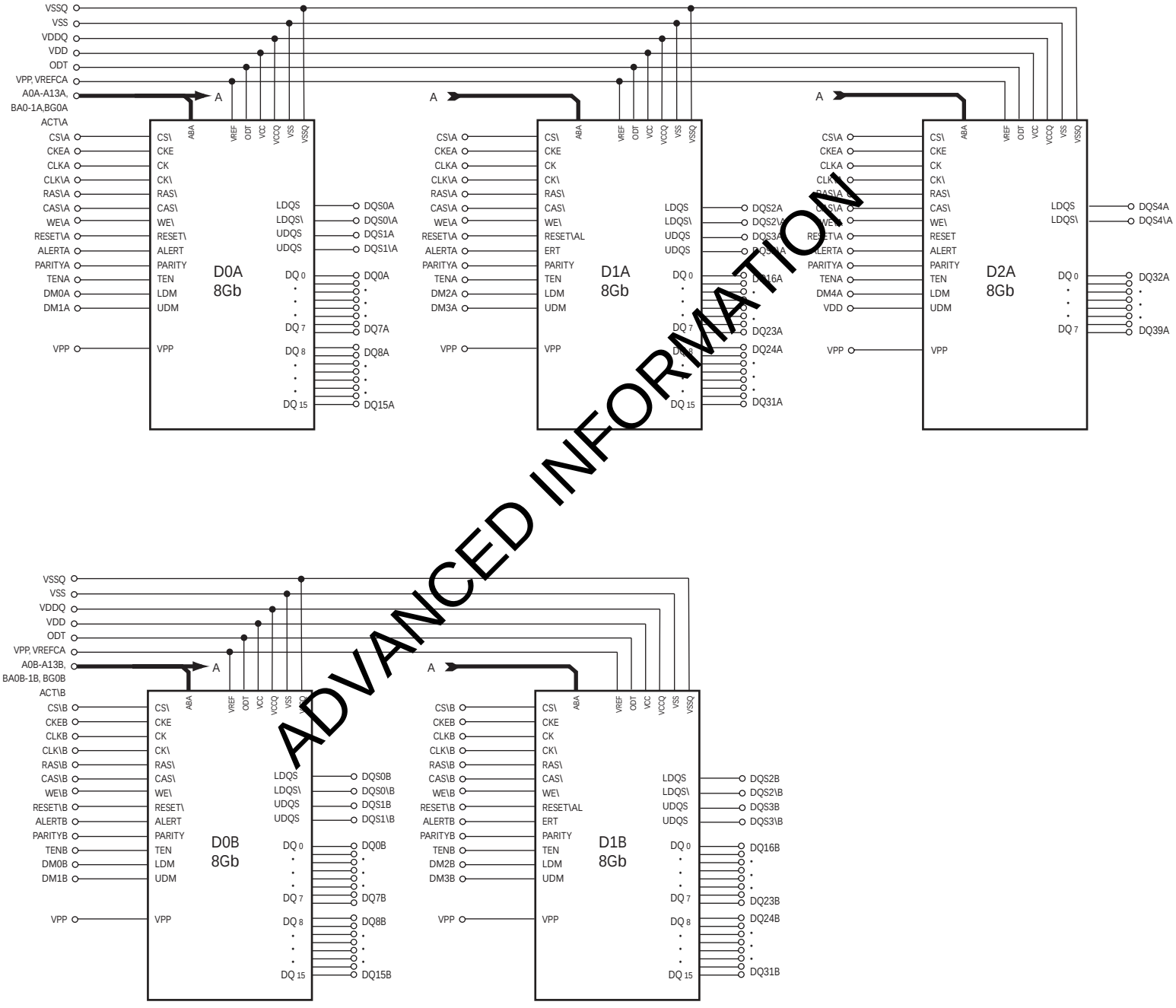


FIGURE 7: ST9D4512M40DBG0 DETAILED ELECTRICAL DIAGRAM

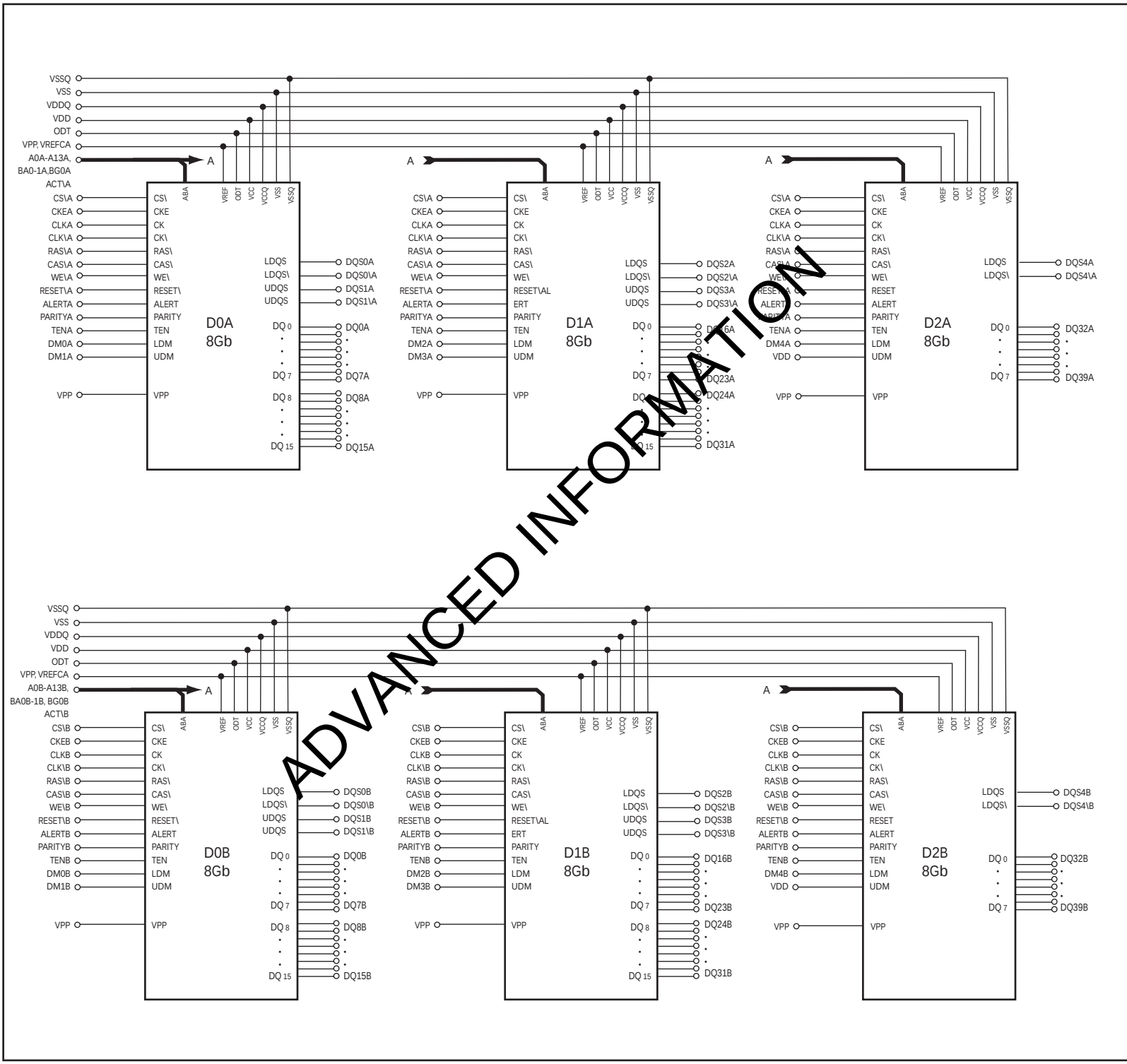
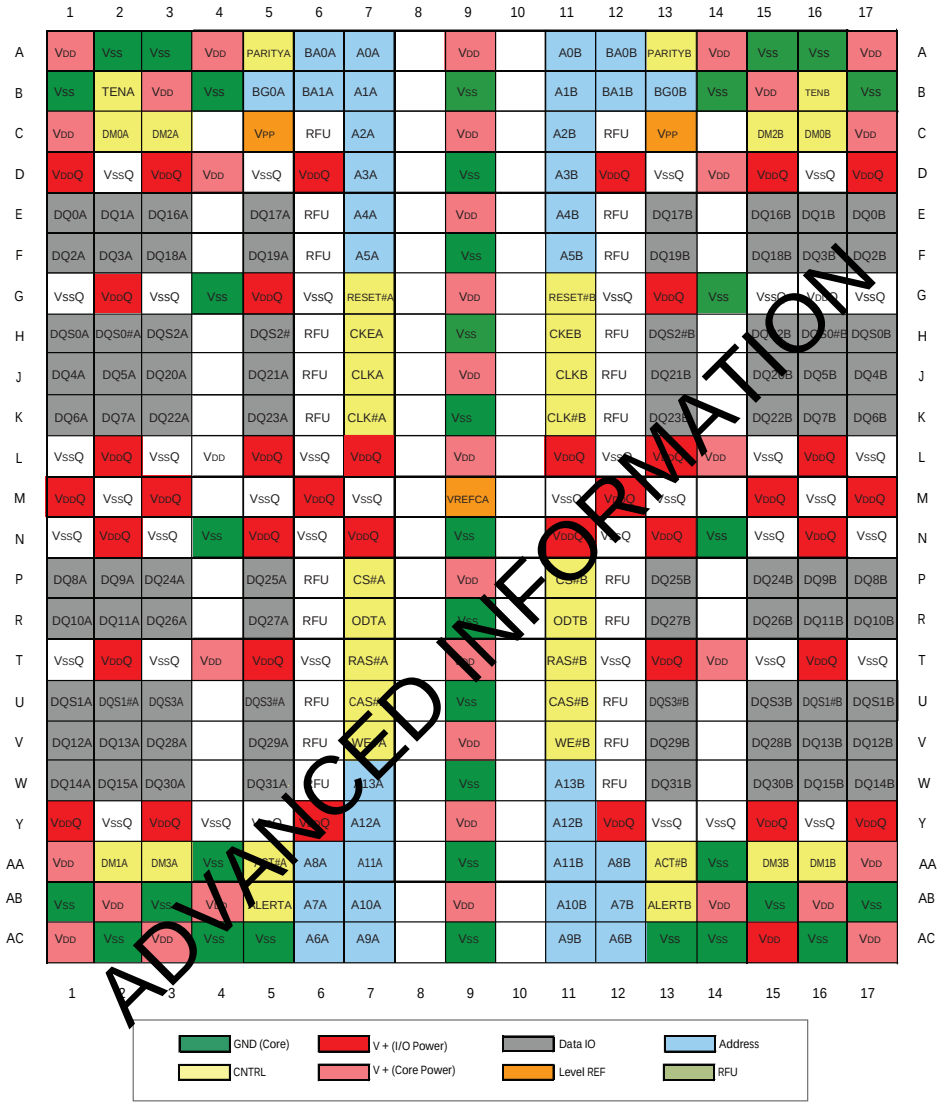


FIGURE 8: ST9D4512M32DBG0 BALL ASSIGNMENTS (TOP VIEW)



321BGA-0.80mm Pitch

FIGURE 9: ST9D4512M72SBG0 BALL ASSIGNMENTS (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VDD	VSS	VSS	VDD	PARITYA	BA0A	A0A		VDD		A0B	BA0B	PARITYB	VDD	VSS	VSS	VDD	A
B	VSS	TENA	VDD	VSS	BG0A	BA1A	A1A		VSS		A1B	BA1B	BG0B	VSS	VDD	TENB	VSS	B
C	VDD	DM0A	DM2A		VPP	DM4A	A2A		VDD		A2B	VDD	VPP		DM2B	DM0B	VDD	C
D	VDDQ	VSSQ	VDDQ	VDD	VSSQ	VDDQ	A3A		VSS		A3B	VDDQ	VSSQ	VDD	VDDQ	VSSQ	VDDQ	D
E	DQ0A	DQ1A	DQ16A		DQ17A	DQ32A	A4A		VDD		A4B	RFU	DQ17B		DQ16B	DQ1B	DQ0B	E
F	DQ2A	DQ3A	DQ18A		DQ19A	DQ33A	A5A		VSS		A5B	RFU	DQ19B		DQ18B	DQ3B	DQ2B	F
G	VSSQ	VDDQ	VSSQ	VSS	VDDQ	VSSQ	RESET#A		VDD		RESET#B	VSSQ	VDDQ	VSS	VSSQ	VDDQ	VSSQ	G
H	DQS0A	DQS0#A	DQS2A		DQS2#	DQS4A	CKEA		VSS		CKEB	RFU	DQS2#B		DQS2B	DQS0#B	DQS0B	H
J	DQ4A	DQ5A	DQ20A		DQ21A	DQ34A	CLKA		VDD		CLKB	RFU	DQ21B		DQ20B	DQ5B	DQ4B	J
K	DQ6A	DQ7A	DQ22A		DQ23A	DQ35A	CLK#A		VSS		CLK#B	RFU	DQ23B		DQ22B	DQ7B	DQ6B	K
L	VSSQ	VDDQ	VSSQ	VDD	VDDQ	VSSQ	VDDQ		VDD		VDDQ	VSSQ	VDDQ	VDD	VSSQ	VDDQ	VSSQ	L
M	VDDQ	VSSQ	VDDQ		VSSQ	VDDQ	VSSQ		VREFCA		VSSQ	VDDQ	VSSQ		VDDQ	VSSQ	VDDQ	M
N	VSSQ	VDDQ	VSSQ	VSS	VDDQ	VSSQ	VDDQ		VSS		VDDQ	VSSQ	VDDQ	VSS	VSSQ	VDDQ	VSSQ	N
P	DQ8A	DQ9A	DQ24A		DQ25A	DQ36A	CS#A		VDD		CS#B	RFU	DQ25B		DQ24B	DQ9B	DQ8B	P
R	DQ10A	DQ11A	DQ26A		DQ27A	DQ37A	ODTA		VSS		ODTB	RFU	DQ27B		DQ26B	DQ11B	DQ10B	R
T	VSSQ	VDDQ	VSSQ	VDD	VDDQ	VSSQ	RAS#A		VDD		RAS#B	VSSQ	VDDQ	VDD	VSSQ	VDDQ	VSSQ	T
U	DQS1A	DQS1#A	DQS3A		DQS3#A	DQS5#A	CAS#A		VSS		CAS#B	RFU	DQS3#B		DQS3B	DQS1#B	DQS1B	U
V	DQ12A	DQ13A	DQ28A		DQ29A	DQ38A	WE#A		VDD		WE#B	RFU	DQ29B		DQ28B	DQ13B	DQ12B	V
W	DQ14A	DQ15A	DQ30A		DQ31A	DQ39A	A13A		VSS		A13B	RFU	DQ31B		DQ30B	DQ15B	DQ14B	W
Y	VDDQ	VSSQ	VDDQ	VSSQ	VSSQ	VDDQ	A12A		VDD		A12B	VDDQ	VSSQ	VSSQ	VDDQ	VSSQ	VDDQ	Y
AA	VDD	DM1A	DM3A	VSS	ACT#A	A8A	A11A		VSS		A11B	A8B	ACT#B	VSS	DM3B	DM1B	VDD	AA
AB	VSS	VDD	VSS	VDD	ALERT#A	A7A	A10A		VDD		A10B	A7B	ALERT#B	VDD	VSS	VDD	VSS	AB
AC	VDD	VSS	VDD	VSS	VSS	A6A	A9A		VSS		A9B	A6B	VSS	VSS	VDD	VSS	VDD	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

GND (Core) | V + (I/O Power) | Data IO | Address
CNTRL | V + (Core Power) | Level REF | RFU

321BGA-0.80mm Pitch

FIGURE 10: ST9D4512M40DBG0 BALL ASSIGNMENTS (TOP VIEW)

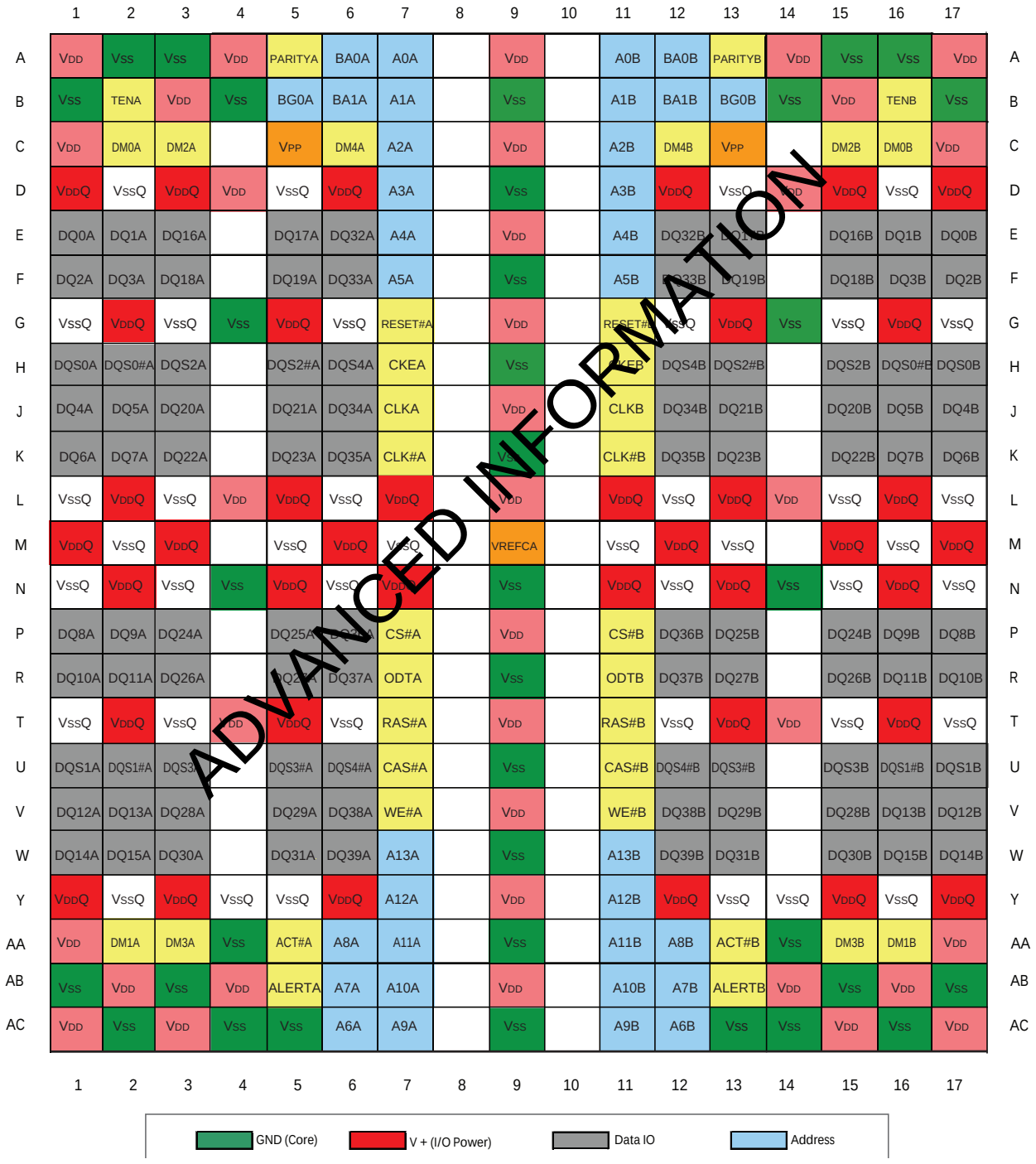


Table 3: Ball Descriptions

Symbol	Type	Description
A[9:0; A11:A13]	Input	Address inputs: Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions - see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	Command input: ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	Bank address inputs: Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[0]	Input	Bank group address inputs: Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	Stack address inputs: These inputs are used to select the second rank in stacked devices. These pins reserved for future use and not utilized on ST9D4512M72BG0 or ST9D4512M80BG0.
CK_t, CK_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

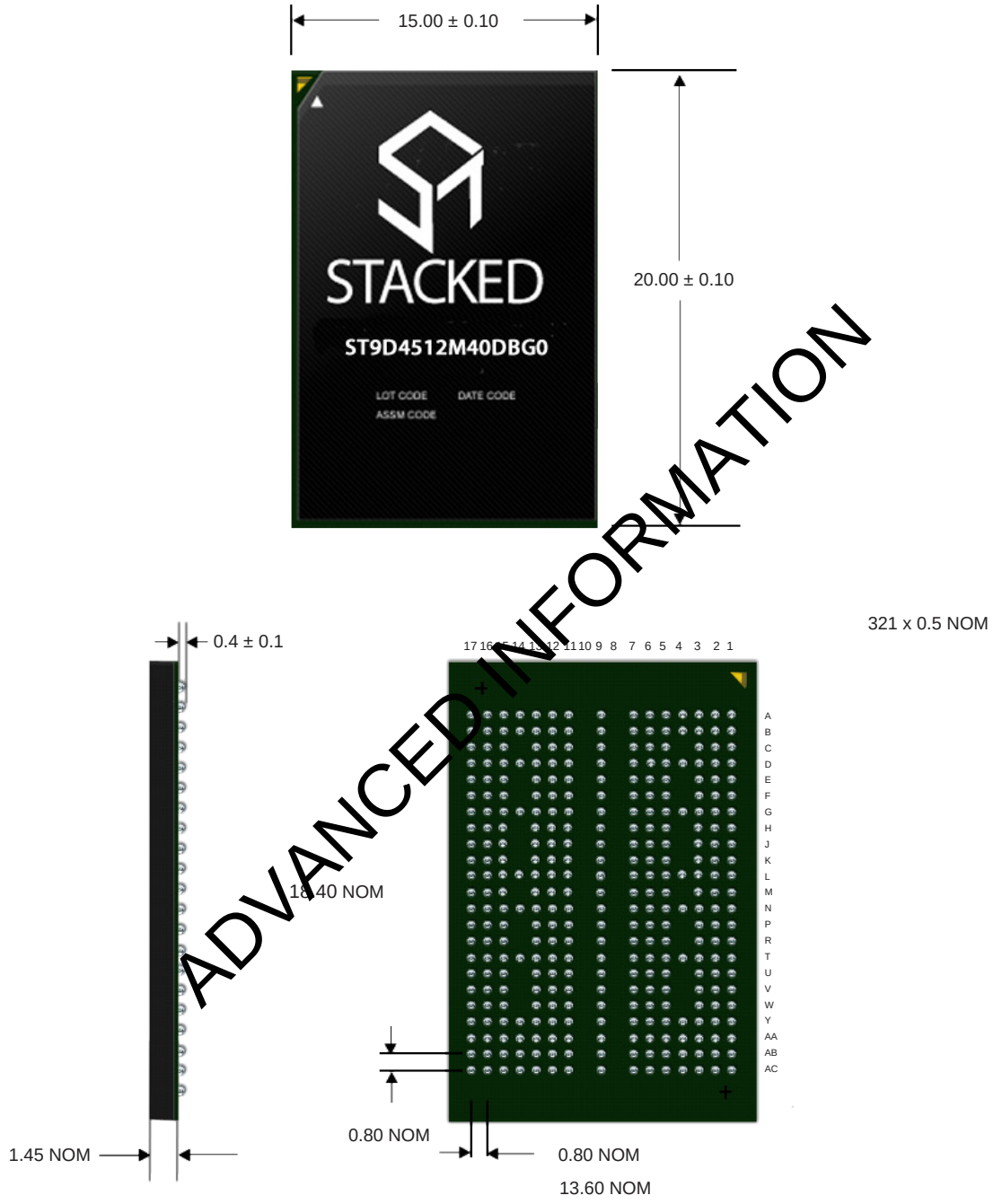
TABLE 3: BALL DESCRIPTIONS (CONTINUED)

Symbol	Type	Description
CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CS_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code.
DM[4:0]_n,	Input	**Input data mask:** DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS.
ODT	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (RTT) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for the x4 and x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PAR	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled, the parity signal covers all command and address inputs, including ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, A[17:0], A10/AP, A12/BC_n, BA[1:0], and BG[1:0] with C0, C1, and C2 on 3DS only devices. Control pins NOT covered by the parity signal are CS_n, CKE, and ODT. Unused address pins that are density- and configuration-specific should be treated internally as 0s by the DRAM parity logic. Command and address inputs will have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is LOW.
RAS_n/A16 CAS_n/A15, WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n and ACT_n) define the command and/or address being entered. See the ACT_n description in this table.
RESET_n	Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD
TEN	Input	**Connectivity test mode:** TEN is active when HIGH and inactive when LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD

Table 3: Ball Descriptions (Continued)

Symbol	Type	Description
DQ[39:0]	I/O	**Data input/output:** Bidirectional data bus. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. TT
DBI[4:0]_n,	I/O	**DBI input/output:** Data bus inversion. DBI_n is an input/output signal used for data bus inversion. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings.
DQS5:0]_t, DQS[5:0]_c,	I/O	**Data strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
V_{DD}	Supply	**Power supply:** 1.2V ±0.060V.
V_{DDQ}	Supply	**DQ power supply:** 1.2V ±0.060V.
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V/+0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present but has no function.

Figure 11: BG0 Package Dimensions



Note: All dimensions in mm

State Diagram

This state diagram provides an overview of the state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and certain other events are not captured in full detail.

FIGURE 12: SIMPLIFIED STATE DIAGRAM

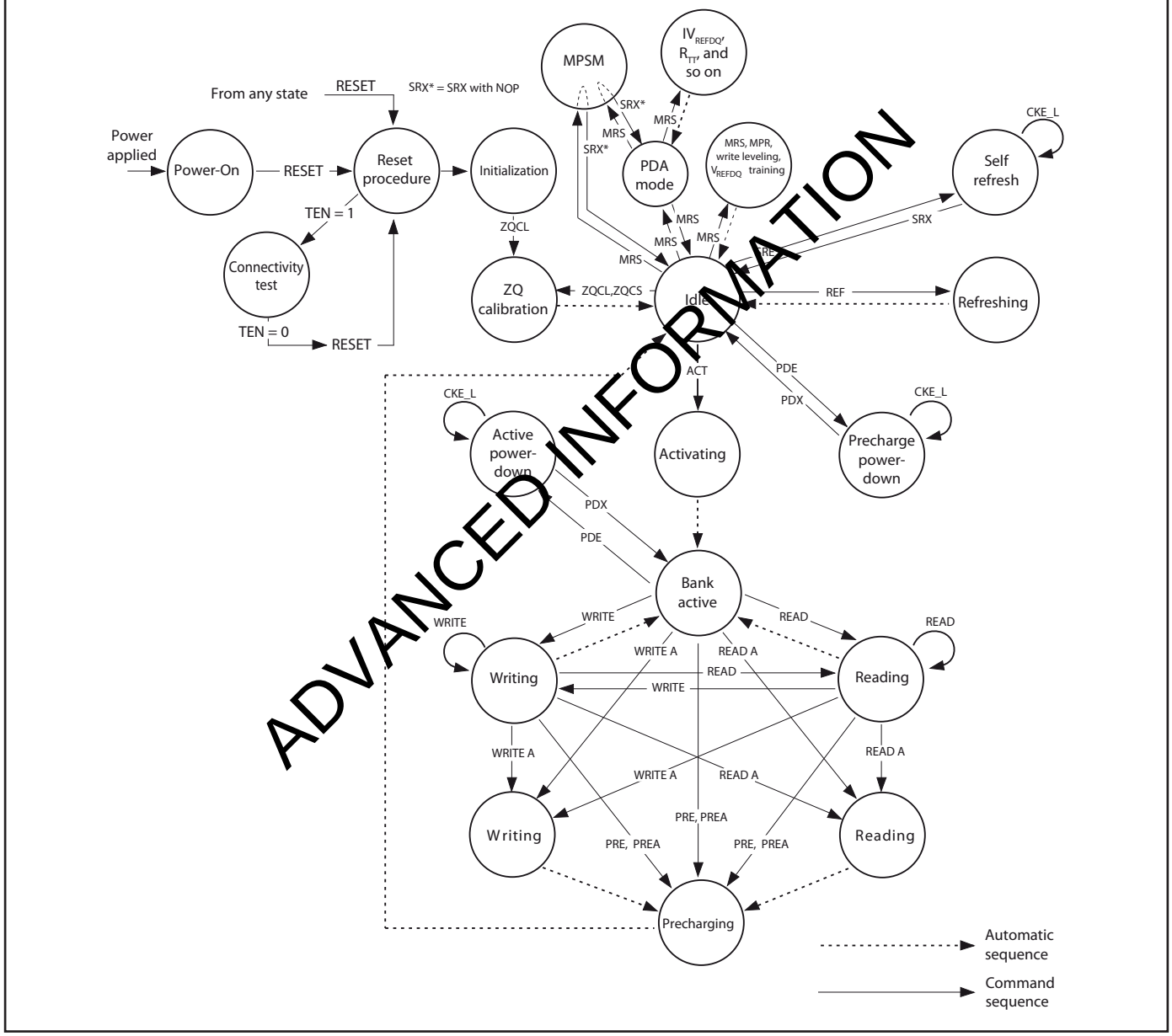


Table 4: State Diagram Command Definitions

Command	Description
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Note: 1. See the Command Truth Table for more details.

Functional Description

This DDR4 SDRAM Module is a high-speed dynamic random-access memory internally configured as eight banks in 2 bank groups. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8n-bit-wide, four-clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one half clock cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registering an
ACTIVE command, then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed; BG0 selects the bank group, BA[1:0] select the bank, and A[15:0] selects the row. The address bits registered coincident with the READ or WRITE command select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized. The following provides detailed information covering device reset and initialization, register definitions, command descriptions, and device operation.

NOTE: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.
To ensure proper device function, the power-up and reset initialization default values
for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable

Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability. Although "unlimited" row accesses to the same row is allowed within the refresh period; excessive row accesses to the same row over a long term can result in degraded operation.

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	
T_{STG}	Storage temperature	-55	150	°C	2

Notes:
1. VDD and VDDQ must be within 300mV of each other at all times, and VREF must not be greater than 0.6 × VDDQ. When VDD and VDDQ are <500mV, VREF can be ≤300mV.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to the JESD51-2 standard.
3. VPP must be equal to or greater than VDD/VDDQ at all times when powered.

DRAM Component Operating Temperature Range

Operating temperature, TOPER, is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JEDEC document JESD51-2.

Table 6: Temperature Range

Symbol	Parameter	Min	Max	Unit	Notes
T_{OPER}	Normal operating temperature range	0	85	°C	1
	Extended temperature range (optional)>85	>85	95	°C	2

Notes:
1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The industrial temperature offering allows the case temperature to go below 0°C to -40°C.
2. 2. Some applications require operation of the commercial and industrial temperature DRAMs in the extended temperature range (between 85°C and 95°C case temperature). Full specifications are supported in this range, but the following additional conditions apply:
   - REFRESH commands must be doubled in frequency, reducing the refresh interval ^{t}REFI to 3.9µs. It is also possible to specify a component with 1X refresh (^{t}REFI to 7.8µs) in the extended temperature range.

Electrical Characteristics – AC and DC Operating Conditions

- If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range capability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

Electrical Characteristics – AC and DC Operating Conditions

Supply Operating Conditions

Table 7: Recommended Supply Operating Conditions

Symbol	Parameter	Rating			Unit	Notes
		Min	Typ	Max		
V_{DD}	Supply voltage	1.14	1.2	1.26	V	1, 2, 3, 4, 5
V_{DDQ}	Supply voltage for output	1.14	1.2	1.26	V	1, 2, 6
V_{PP}	Wordline supply voltage	2.375	2.5	2.750	V	7

Notes:
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. V_{DD} slew rate between 300mV and 80% of V_{DD},min shall be between 0.004 V/ms and 600 V/ms, 20 MHz band-limited measurement.
4. V_{DD} ramp time from 300mV to $V_{DD,min}$ shall be no longer than 200ms.
5. A stable valid V_{DD} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DD} provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.
6. A stable valid V_{DDQ} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±60mV (greater than 250 KHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.
7. A stable valid V_{PP} level is a set DC level (0 Hz to 250 KHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is final. AC noise of ±120mV (greater than 250 KHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.

Table 8: V_{DD} Slew Rate

Symbol	Min	Max	Unit	Notes
V_{DD_sl}	0.004	600	V/ms	1, 2
V_{DD_on}	–	200	ms	3

Notes:
1. Measurement made between 300mV and 80% V_{DD} (minimum level).
2. The DC bandwidth is limited to 20 MHz.
3. Maximum time to ramp V_{DD} from 300 mV to V_{DD} minimum.

Table 9: Leakage

Condition	Symbol	Min	Max	Unit	Notes
Input leakage (excluding ZQ and TEN)	I_{IN}	–4	4	µA	1
ZQ leakage	I_{ZQ}	–6	6	µA	2
TEN leakage	I_{TEN}	–12	20	µA	1, 2
V_{REFCA} leakage	I_{VREFCA}	–4	4	µA	3
Output leakage: $V_{OUT} = V_{DDQ}$	I_{OZpd}	–	10	µA	4
Output leakage: $V_{OUT} = V_{SSQ}$	I_{OZpu}	–50	–	µA	4, 5

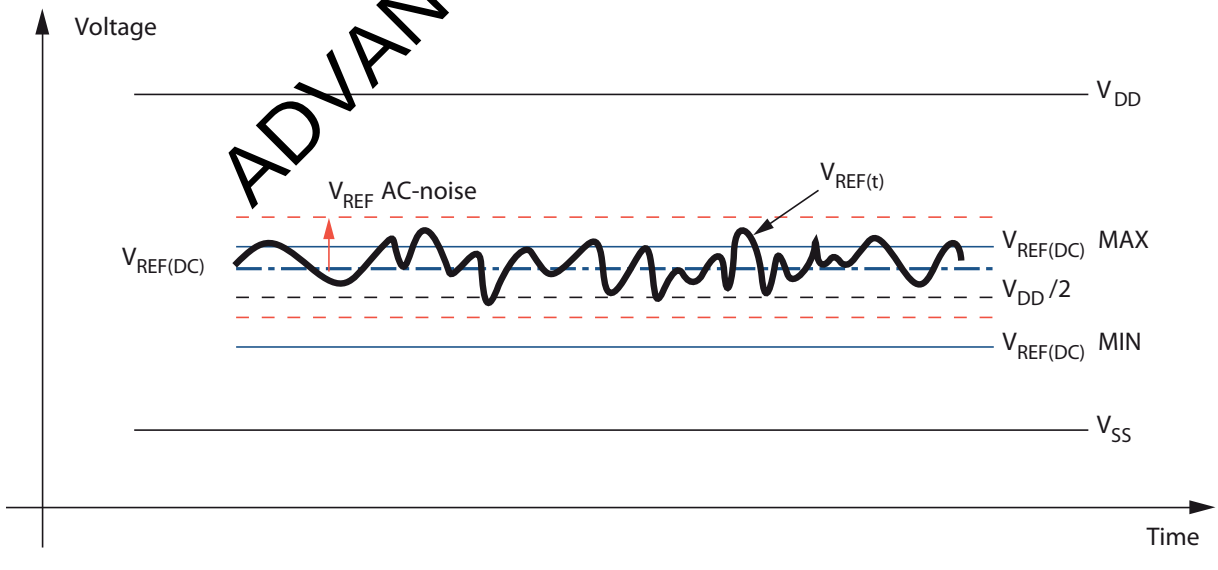
Notes:
1. Input under test 0V < VIN < 1.1V.
2. Additional leakage due to weak pull-down.
3. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level after initialization.
4. DQs are disabled.
5. ODT is disabled with the ODT input HIGH.

V_{REFCA} Supply

V_{REFCA} is to be supplied to the DRAM and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{REF(t)}$ as a function of time (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than ±1% V_{DD} for the AC-noise limit.

Figure 13: V_{REFDQ} Voltage Range



The voltage levels for setup and hold time measurements are dependent on V_{REF}. V_{REF} is understood as $V_{REF(DC)}$, as defined in the above figure. This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (±1% of V_{DD}) are included in DRAM timings and their associated deratings.

V_{REFDQ} Supply and Calibration Ranges

The device internally generates its own V_{REFDQ}. DRAM internal V_{REFDQ} specification parameters: voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level are used to help provide estimated values for the internal V_{REFDQ} and are not pass/fail limits. The voltage operating range specifies the minimum required range for DDR4 SDRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. A calibration sequence should be performed by the DRAM controller to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers.

TABLE 10: V_{REFDQ} SPECIFICATION

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Range 1 V_{REFDQ}	V_{REFDQ}	60%	–	92%	V_{DDQ}	1, 2
Range 2 V_{REFDQ}	V_{REFDQ}	45%	–	77%	V_{DDQ}	1, 2
V_{REF}	$V_{REF,step}$	0.5%	–0.65%	0.8%	V_{DDQ}	3
V_{REF}	V_{REF,set_tol}	–1.625%	0%	1.625%	V_{DDQ}	4, 5, 6,
		–0.15%	0%	0.15%	V_{DDQ}	4, 7, 8,
V_{REF}	$V_{REF,time}$	–	–	150	ns	9, 10, 11
V_{REF}	$V_{REF\_val\_tol}$	–0.15%	0%	0.15%	V_{DDQ}	12

Notes:
1. $V_{REF(DC)}$ voltage is referenced to $V_{DDQ(DC)}$. $V_{DDQ(DC)}$ is 1.2V.
2. DRAM range 1 or range 2 is set by the MRS6[6]6.
3. V_{REF} step size increment/decrement range. V_{REF} at DC level.
4. $V_{REF,new} = V_{REF,old} \pm n \times V_{REF,step}$; n = number of steps. If increment, use "+," if decrement, use "-."
5. For n >4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ - 1.625% × V_{DDQ}. The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 1.625% × V_{DDQ}.
6. Measured by recording the MIN and MAX values of the V_{REF} output over the range, drawing a straight line between those points, and comparing all other VREF output settings to that line.
7. For n ≤4, the minimum value of V_{REF} setting tolerance = $V_{REF,new}$ - 0.15% × V_{DDQ}. The maximum value of V_{REF} setting tolerance = $V_{REF,new}$ + 0.15% × V_{DDQ}.
8. Measured by recording the MIN and MAX values of the V_{REF} output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing all V_{REF} output settings to that line.
9. Time from MRS command to increment or decrement one step size for V_{REF}.
10. Time from MRS command to increment or decrement more than one step size up to the full range of V_{REF}.
11. If the V_{REF} monitor is enabled, V_{REF} must be derated by +10ns if DQ bus load is 0pF and an additional +15 ns/pF of DQ bus loading.
12. Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid qualifies the step times, which will be characterized at the component level.

V_{REFDQ} Ranges

MR6[6] selects range 1 (60% to 92.5% of V_{DDQ}) or range 2 (45% to 77.5% of V_{DDQ}), and MR6[5:0] sets the V_{REFDQ} level, as listed in the following table. The values in MR6[6:0] will update the V_{DDQ} range and level independent of MR6[7] setting. It is recommended MR6[7] be enabled when changing the settings in MR6[6:0], and it is highly recommended MR6[7] be enabled when changing the settings in MR6[6:0] multiple times during a calibration routine.

Electrical Characteristics – AC and DC Single-Ended Input Measurement Levels

Table 11: V_{REFDQ} Range and Levels

MR6[5:0]	MR6[6] 0 = Range 1	MR6[6] 1 = Range 2	MR6[5:0]	MR6[6] 0 = Range 1	MR6[6] 1 = Range 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	10 0000	91.20%	76.20%
01 0111	74.95%	59.95%	10 0001	91.85%	76.85%
01 1000	75.60%	60.60%	10 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 are reserved		

Electrical Characteristics – AC and DC Single-Ended Input Measurement Levels

RESET_n Input Levels

Table 12: RESET_n Input Levels (CMOS)

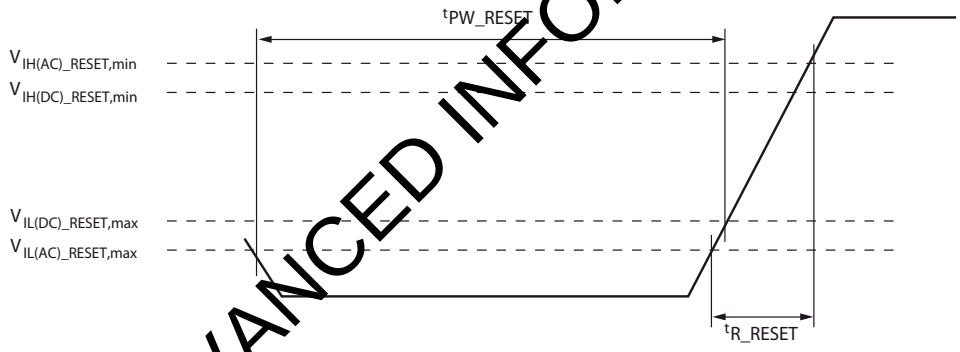
Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)\_RESET}$	$0.8 \times V_{DD}$	V_{DD}	V	1
DC input high voltage	$V_{IH(DC)\_RESET}$	$0.7 \times V_{DD}$	V_{DD}	V	2
DC input low voltage	$V_{IL(DC)\_RESET}$	V_{SS}	$0.3 \times V_{DD}$	V	3

Table 12: RESET_n Input Levels (CMOS) (Continued)

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	$V_{IL(AC)\_RESET}$	V_{SS}	$0.2 \times V_{DD}$	V	4
Rising time	$^{t}R\_RESET$	–	1	µs	5
RESET pulse width after power-up	$^{t}PW\_RESET\_S$	1	–	µs	6, 7
RESET pulse width during power-up	$^{t}PW\_RESET\_L$	200	–	µs	6

Notes:
1. Overshoot should not exceed the VIN shown in the Absolute Maximum Ratings table.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above $V_{IH(DC)\_RESET}$, otherwise operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. After RESET_n is registered LOW, the RESET_n level must be maintained below $V_{IL(DC)\_RESET}$ during tPW_RESET, otherwise the DRAM may not be reset.
4. Undershoot should not exceed the VIN shown in the Absolute Maximum Ratings table.
5. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
6. RESET is destructive to data contents.
7. See RESET Procedure at Power Stable Condition figure.

Figure 14: RESET_n Input Slew Rate Definition



Command/Address Input Levels

Table 13: Command and Address Input Levels: DDR4-1600 Through DDR4-2400

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 100	$V_{DD}5$	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 75	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 75	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	$V_{SS}5$	V_{REF} - 100	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	$0.49 \times V_{DD}$	$0.51 \times V_{DD}$	V	4

Notes:
1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet tIS timings and $V_{IL}/V_{IH(DC)}$ to meet tIH timings. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than
4. ±1% V_{DD} (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 14: Command and Address Input Levels: DDR4-2666

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 90	V_{DD}5	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 65	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	V_{SS}5	V_{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	0.49 × V_{DD}	0.49 × V_{DD}	V	4

Notes:
1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet tIS timings and $V_{IL}/V_{IH(AC)}$ to meet ^{t}IH timings.
4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% VDD (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 15: Command and Address Input Levels: DDR4-2933 and DDR4-3200

Parameter	Symbol	Min	Max	Unit	Note
AC input high voltage	$V_{IH(AC)}$	V_{REF} + 90	V_{DD}5	mV	1, 2, 3
DC input high voltage	$V_{IH(DC)}$	V_{REF} + 65	V_{DD}	mV	1, 2
DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 65	mV	1, 2
AC input low voltage	$V_{IL(AC)}$	V_{SS}5	V_{REF} - 90	mV	1, 2, 3
Reference voltage for CMD/ADDR inputs	$V_{REFFCA(DC)}$	0.49 × V_{DD}	0.49 × V_{DD}	V	4

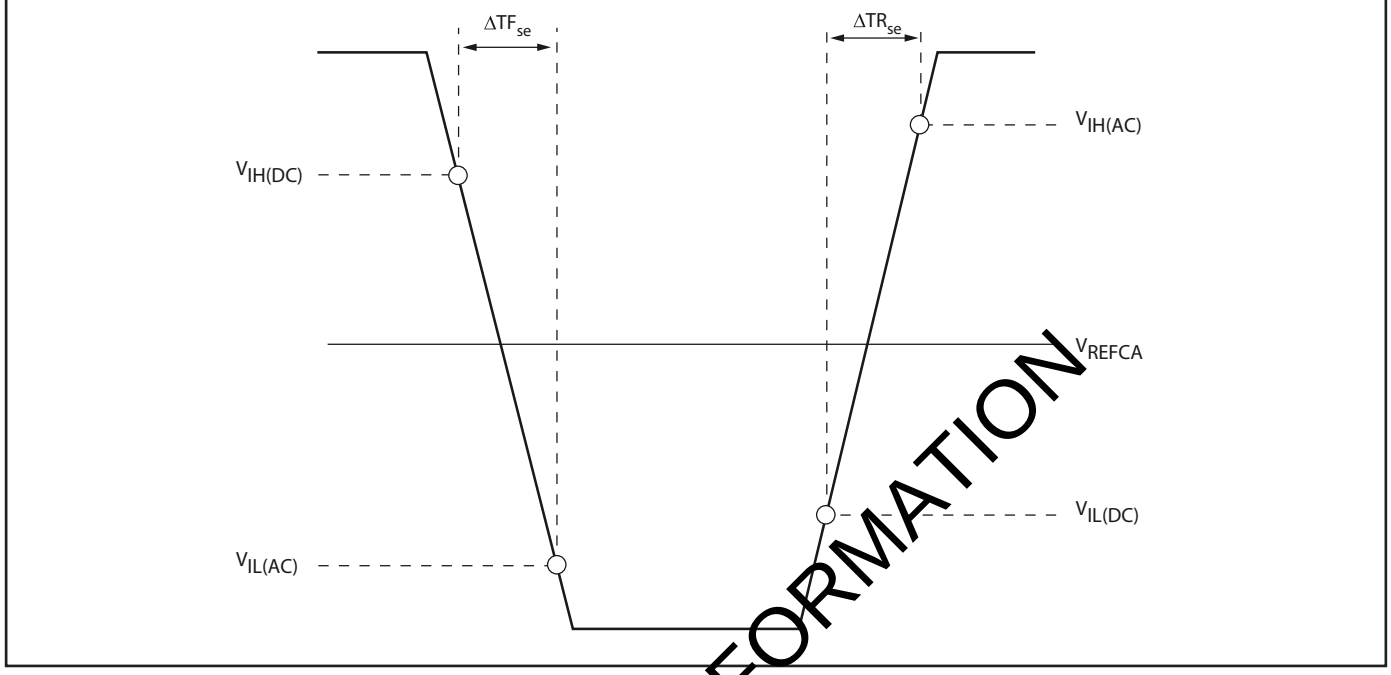
Notes:
1. For input except RESET_n. $V_{REF} = V_{REFCA(DC)}$.
2. $V_{REF} = V_{REFCA(DC)}$.
3. Input signal must meet $V_{IL}/V_{IH(AC)}$ to meet tIS timings and $V_{IL}/V_{IH(AC)}$ to meet ^{t}IH timings.
4. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REFCA(DC)}$ by more than ±1% V_{DD} (for reference: approximately ±12mV).
5. Refer to "Overshoot and Undershoot Specifications."

Table 16: Single-Ended Input Slew Rates

Parameter	Symbol	Min	Max	Unit	Note
Single-ended input slew rate – CA	SR_{CA}	1.0	7.0	V/ns	1, 2, 3, 4

Notes:
1. For input except RESET_n.
2. $V_{REF} = V_{REFCA(DC)}$.
3. ^{t}IS/^{t}IH timings assume SRCA = 1V/ns.
4. Measured between $V_{IH(AC)}$ and $V_{IL(AC)}$ for falling edges and between $V_{IL(AC)}$ and $V_{IH(AC)}$ for rising edges

Figure 15: Single-Ended Input Slew Rate Definition



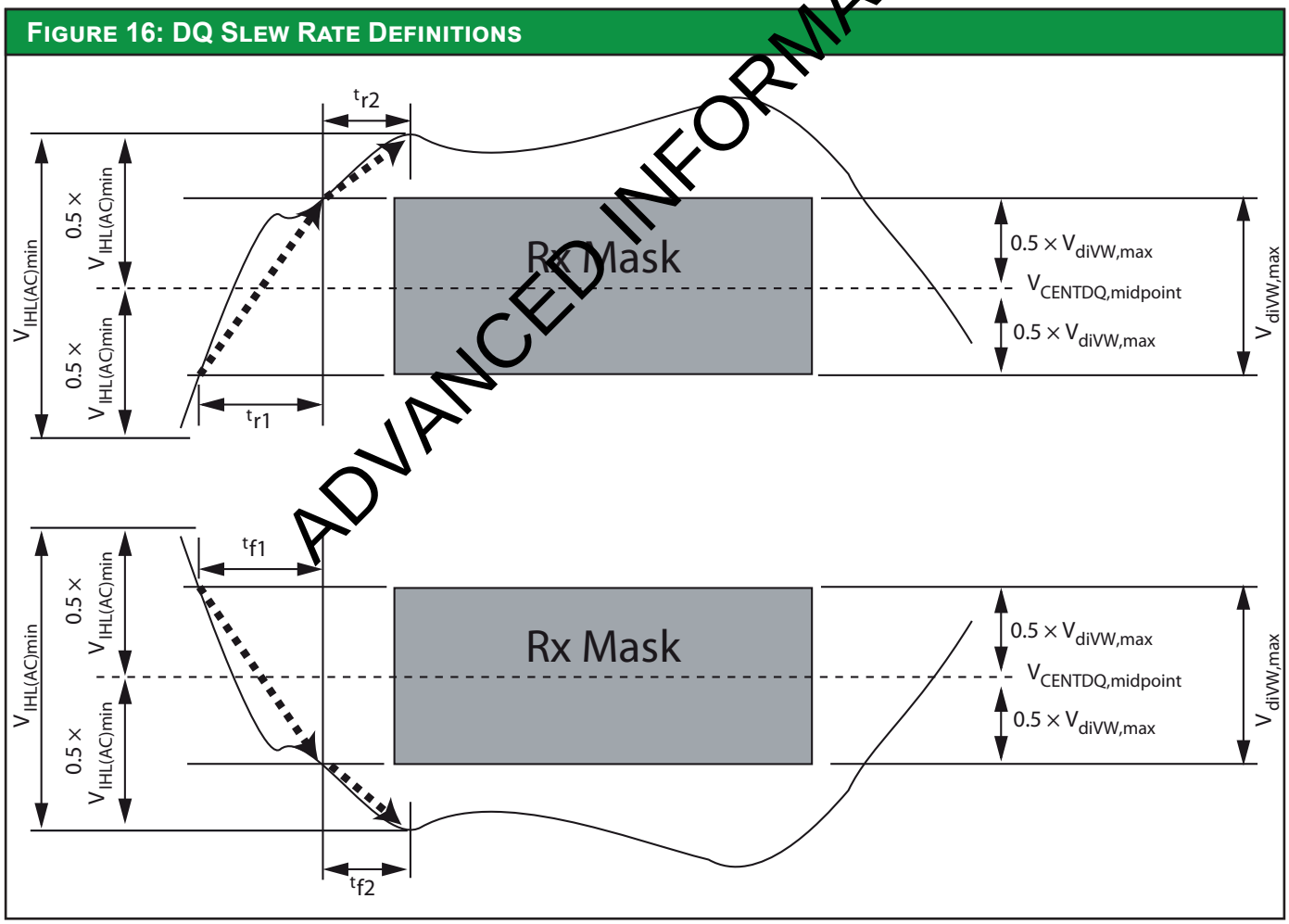
Data Receiver Input Requirements

The following parameters apply to the data receiver Rx MASK operation detailed in the Write Timing section, Data Strobe-to-Data Relationship.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement oints for a rising edge are shown in the figure below. A LOW-to-HIGH transition time, tr1, is measured from $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the last transition through $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$; tr2 is measured from the last transition through $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the first transition through the $0.5 \times V_{IHL(AC)min}$ above $V_{CENTDQ,midpoint}$.

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a rising edge are shown in the figure below. A HIGH-to-LOW transition time, tf1, is measured from $0.5 \times V_{diVW,max}$ above $V_{CENTDQ,midpoint}$ to the last transition through $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$; tf2 is measured from the last transition through $0.5 \times V_{diVW,max}$ below $V_{CENTDQ,midpoint}$ to the first transition through the $0.5 \times V_{IHL(AC)min}$ below $V_{CENTDQ,midpoint}$.

Figure 16: DQ Slew Rate Definitions



Notes:
1. Rising edge slew rate equation srr1 = $V_{diVW,max}/(^{t}r1)$.
2. Rising edge slew rate equation srr2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 \times {}^{t}r2)$.
3. Falling edge slew rate equation srf1 = $V_{diVW,max}/(^{t}f1)$.
4. Falling edge slew rate equation srf2 = $(V_{IHL(AC)min} - V_{diVW,max})/(2 \times {}^{t}f2)$.

TABLE 17: DQ INPUT RECEIVER SPECIFICATIONS

Note 1 applies to the entire table

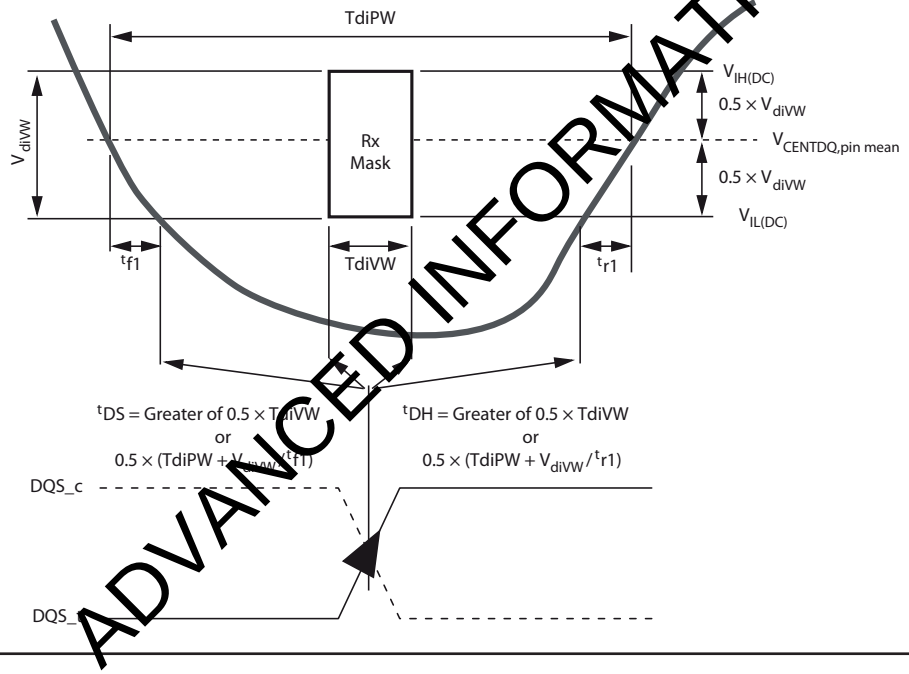
Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
V_{IN} Rx mask input peak-to-peak	V_{diVW}	–	136	–	130	–	120	–	115	–	110	mV	2, 3
DQ Rx input timing window	TdiVW	–	0.2	–	0.2	–	0.22	–	0.23	–	0.23	UI	2, 3
DQ AC input swing peak-to-peak	$V_{IHL(AC)}$	186	–	160	–	150	–	145	–	140	–	mV	4, 5
DQ input pulse width	TdiPW	0.58	–	0.58	–	0.58	–	0.58	–	0.58	–	UI	6
DQS-to-DQ Rx mask offset	^{t}DQS2DQ	–0.17	0.17	–0.17	0.17	–0.19	0.19	–0.22	0.22	–0.22	0.22	UI	7
DQ-to-DQ Rx mask offset	^{t}DQ2DQ	–	0.1	–	0.1	–	0.105	–	0.115	–	0.125	UI	8
Input slew rate over V_{diVW} if ^{t}CK ≥ 0.925ns	srr1, srf1	1	9	1	9	1	9	1	9	1	9	V/ns	9
Input slew rate over V_{diVW} if 0.935ns > ^{t}CK ≥ 0.625ns	srr1, srf1	–	–	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	9
Rising input slew rate over 1/2 $V_{IHL(AC)}$	srr2	srr2 ≥ srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	0.2 × srr1	9	V/ns	10
Falling input slew rate over 1/2 $V_{IHL(AC)}$	srf2	srf2 ≥ srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	0.2 × srf1	9	V/ns	10

Notes:
1. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW (MIN), $V_{diVW,max}$, and minimum slew rate limits, then either TdiVW (MIN) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.
2. Data Rx mask voltage and timing total input valid window where V_{diVW} is centered around $V_{CENTDQ,midpoint}$ after V_{REFDQ} training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER =1e- 16 when the Rx mask is not violated.
3. Defined over the DQ internal V_{REF} range 1.
4. Overshoot and undershoot specifications apply.
5. DQ input pulse signal swing into the receiver must meet or exceed $V_{IHL(AC)min}$. $V_{IHL(AC)min}$ is to be achieved on an UI basis when a rising and falling edge occur in the same UI (a valid TdiPW).
6. DQ minimum input pulse width defined at the $V_{CENTDQ,midpoint}$.

7. DQS-to-DQ Rx mask offset is skew between DQS and DQ within a nibble (x4) or word (x8, x16 [for x16, the upper and lower bytes are treated as separate x8s]) at the SDRAM balls over process, voltage, and temperature.
8. DQ-to-DQ Rx mask offset is skew between DQs within a nibble (x4) or word (x8, x16) at the SDRAM balls for a given component over process, voltage, and temperature.
9. Input slew rate over V_{diVW} mask centered at $V_{CENTDQ,midpoint}$. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
10 Input slew rate between VdiVW mask edge and $V_{IHL(AC)min}$ points.

The following figure shows the Rx mask relationship to the input timing specifications relative to system ^{t}DS and ^{t}DH. The classical definition for ^{t}DS/^{t}DH required a DQ rising and falling edges to not violate ^{t}DS and ^{t}DH relative to the DQS strobe at any time; however, with the Rx mask ^{t}DS and ^{t}DH can shift relative to the DQS strobe provided the input pulse width specification is satisfied and the Rx mask is not violated.

FIGURE 17: RX MASK RELATIVE TO ^{T}DS/^{T}DH



The following figure and table show an example of the worst case Rx mask required if the DQS and DQ pins do not have DRAM controller to DRAM write DQ training. The figure and table show that without DRAM write DQ training, the Rx mask would increase from 0.2UI to essentially 0.54UI. This would also be the minimum ^{t}DS and ^{t}DH required as well.

Figure 18: Rx Mask Without Write Training

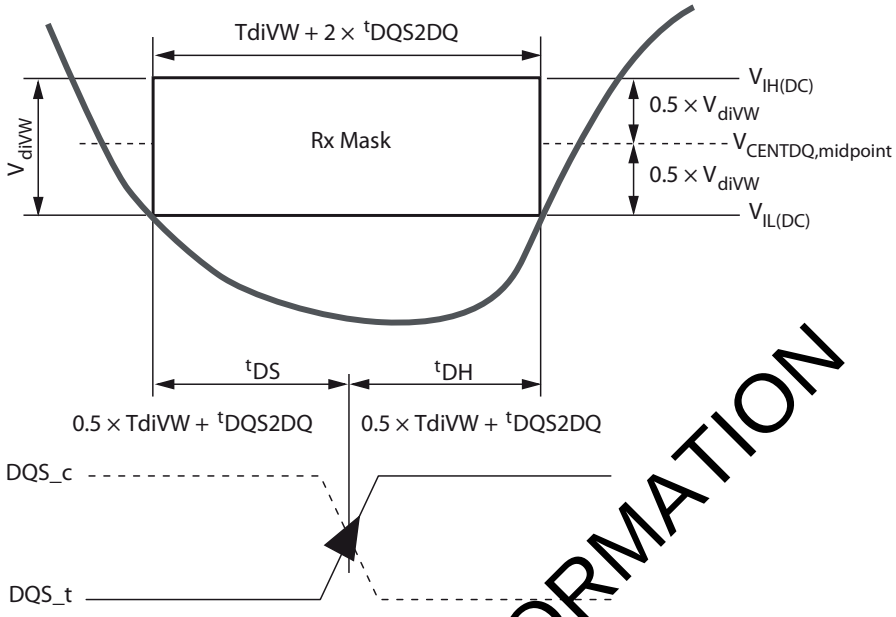


Table 18: Rx Mask and tDS/tDH Without Write Training

DDR4	$V_{IHL(AC)}$ (mV)	TdiPW (UI)	V_{diVW} (mV)	TdiVW (UI)	tDQS2DQ (UI)	tDQ2DQ (UI)	Rx Mask (ps)	tDS/tDH_No Training (ps)
1600	186	0.58	136	0.2	±0.17	0.1	125	338
1866	186	0.58	136	0.2	±0.17	0.1	107.1	289
2133	186	0.58	136	0.2	±0.17	0.1	3.84	253
2400	160	0.58	130	0.2	±0.17	0.1	83.3	225
2666	150	0.58	120	0.22	±0.19	0.105	82.5	225
2933	145	0.58	115	0.23	±0.22	0.115	78.4	228
3200	140	0.58	110	0.23	±0.22	0.125	71.8	209

Connectivity Test (CT) Mode Input Levels

Table 19: TEN Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
TEN AC input high voltage	$V_{IH(AC)\_TEN}$	$0.8 \times V_{DD}$	V_{DD}	V	1
TEN DC input high voltage	$V_{IH(DC)\_TEN}$	$0.7 \times V_{DD}$	V_{DD}	V	
TEN DC input low voltage	$V_{IL(DC)\_TEN}$	V_{SS}	$0.3 \times V_{DD}$	V	
TEN AC input low voltage	$V_{IL(AC)\_TEN}$	V_{SS}	$0.2 \times V_{DD}$	V	2
TEN falling time	tF_TEN	–	1 0	ns	

Table 19: TEN Input Levels (CMOS) (Continued)

Parameter	Symbol	Min	Max	Unit	Note
TEN rising time	^{t}R_TEN	–	1 0	ns	

Notes: 1. Overshoot should not exceed the VIN values in the Absolute Maximum Ratings table.
2. Undershoot should not exceed the VIN values in the Absolute Maximum Ratings table.

Figure 19: TEN Input Slew Rate Definition

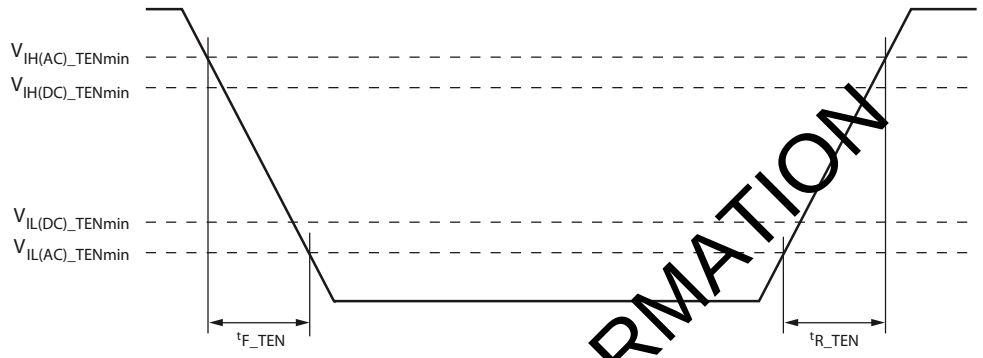


Table 20: CT Type-A Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipA AC input high voltage	$V_{IH(AC)}$	V_{REF} + 200	V_{DD1}[1]	V	2, 3
CTipA DC input high voltage	$V_{IH(DC)}$	V_{REF} + 150	V_{DD}	V	2, 3
CTipA DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 150	V	2, 3
CTipA AC input low voltage	$V_{IL(AC)}$	V_{SS1}[1]	V_{REF} - 200	V	2, 3
CTipA falling time	^{t}F_CTipA	–	5	ns	2
CTipA rising time	^{t}R_CTipA	–	5	ns	2

Notes: 1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-A inputs: CS_n, BG[1:0], BA[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_C, PAR.
3. $V_{REFCA} = 0.5 \times V_{DD}$.

Figure 20: CT Type-A Input Slew Rate Definition

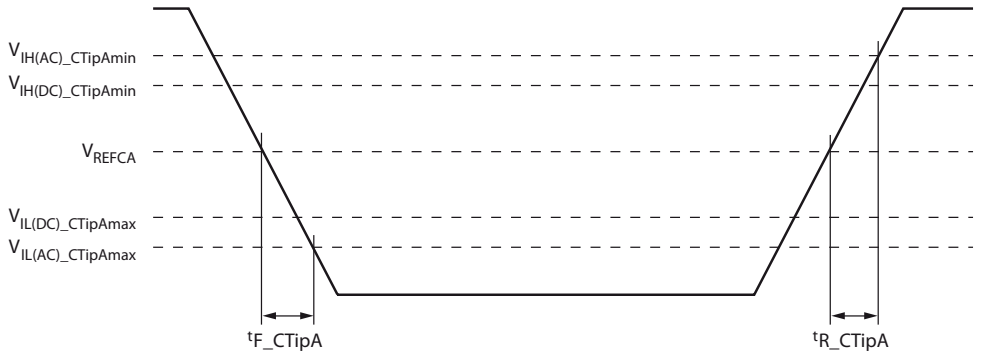


Table 21: CT Type-B Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipB AC input high voltage	$V_{IH(AC)}$	V_{REF} + 300	V_{DD1} [1]	V	2, 3
CTipB DC input high voltage	$V_{IH(DC)}$	V_{REF} + 200	V_{DD}	V	2, 3
CTipB DC input low voltage	$V_{IL(DC)}$	V_{SS}	V_{REF} - 200	V	2, 3
CTipB AC input low voltage	$V_{IL(AC)}$	V_{SS1} [1]	V_{REF} - 300	V	2, 3
CTipB falling time	$^{t}F\_CTipB$	–	V	ns	2
CTipB rising time	$^{t}R\_CTipB$	–	V	ns	2

Notes:
1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-B inputs: DML_n/DBIL_n, DMU_n/DBIU_n and DM_n/DBI_n.
3. V_{REFDQ} should be 0.5 × V_{DD}

Figure 21: CT Type-B Input Slew Rate Definition

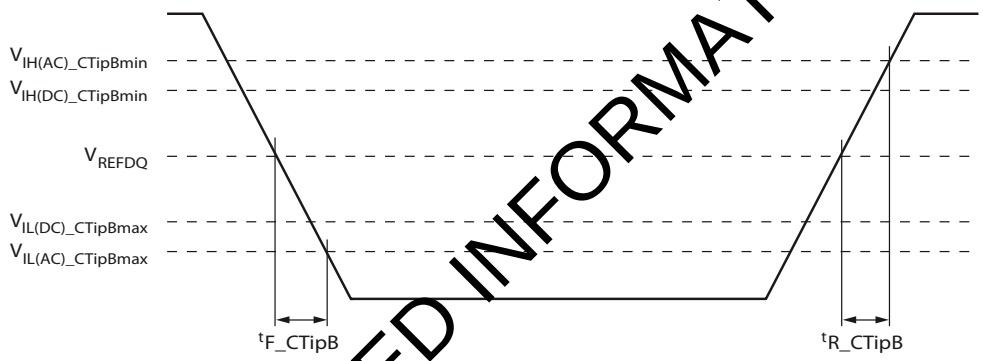


Table 22: CT Type-C Input Levels (CMOS)

Parameter	Symbol	Min	Max	Unit	Note
CTipC AC input high voltage	$V_{IH(AC)\_CTipC}$	0.8 × V_{DD}	V_{DD} [1]	V	2
CTipC DC input high voltage	$V_{IH(DC)\_CTipC}$	0.7 × V_{DD}	V_{DD}	V	2
CTipC DC input low voltage	$V_{IL(DC)\_CTipC}$	V_{SS}	0.3 × V_{DD}	V	2
CTipC AC input low voltage	$V_{IL(AC)\_CTipC}$	V_{SS} [1]	0.2 × V_{DD}	V	2
CTipC falling time	$^{t}F\_CTipC$	–	1 0	ns	2
CTipC rising time	$^{t}R\_CTipC$	–	1 0	ns	2

Notes:
1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-C inputs: Alert_n.

Figure 22: CT Type-C Input Slew Rate Definition

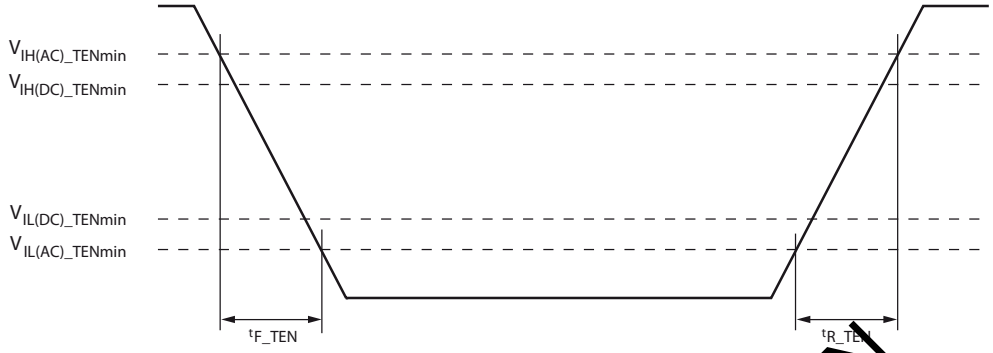
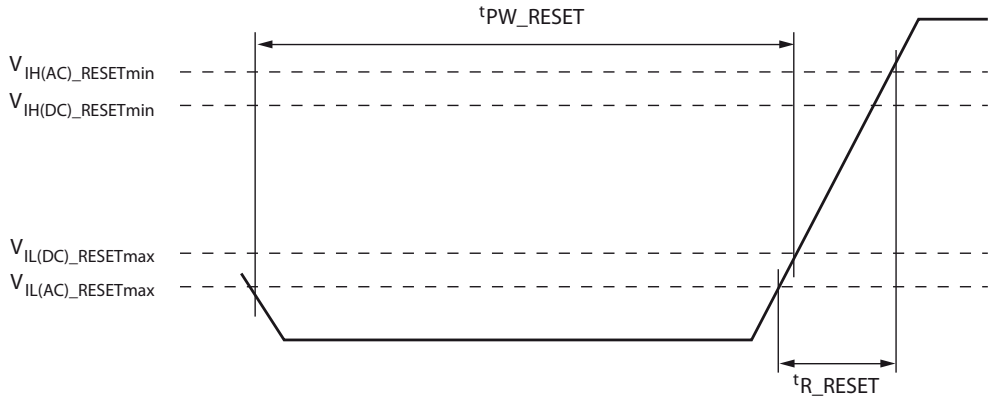


Table 23: CT Type-D Input Levels

Parameter	Symbol	Min	Max	Unit	Note
CTipD AC input high voltage	$V_{IH(AC)\_CTipD}$	$0.8 \times V_{DD}$	V_{DD}	V	4
CTipD DC input high voltage	$V_{IH(DC)\_CTipD}$	$0.7 \times V_{DD}$	V_{DD}	V	2
CTipD DC input low voltage	$V_{IL(DC)\_CTipD}$	V_{SS}	$0.3 \times V_{DD}$	V	1
CTipD AC input low voltage	$V_{IL(AC)\_CTipD}$	V_{SS}	$0.2 \times V_{DD}$	V	5
Rising time	$^{t}R\_RESET$	–	1	µs	3
RESET pulse width - after power-up	$^{t}PW\_RESET\_S$	1	–	µs	
RESET pulse width - during power-up	$^{t}PW\_RESET\_L$	200	–	µs	

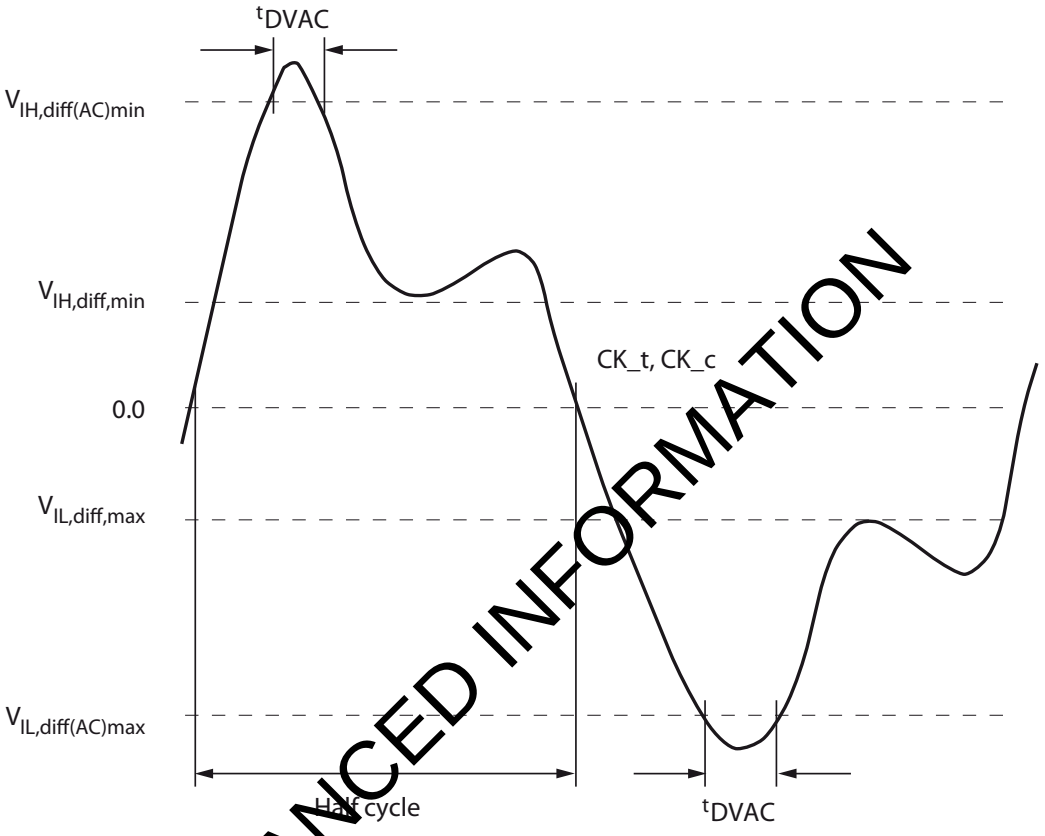
Notes:
1. After RESET_n is registered LOW, the RESET_n level must be maintained below $V_{IL(DC)\_RESET}$ during $^{t}PW\_RESET$, otherwise, the DRAM may not be reset.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above $V_{IH(DC)\_RESET}$, otherwise, operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
4. Overshoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
5. Undershoot should not exceed the V_{IN} values in the Absolute Maximum Ratings table.
6. CT Type-D inputs: RESET_n; same requirements as in normal mode.

Figure 23: CT Type-D Input Slew Rate Definition



Differential Inputs

Figure 24: Differential AC Swing and "Time Exceeding AC-Level" tDVAC



Notes: 1. Differential signal rising edge from $V_{IL,diff,max}$ to $V_{IH,diff(AC)min}$ must be monotonic slope.
2. Differential signal falling edge from $_{IH,diff,min}$ to $V_{IL,diff(AC)max}$ must be monotonic slope.

Table 24: Differential Input Swing Requirements for CK_t, CK_c

Parameter	Symbol	DDR4-1600 / 1866 / 2133 / 2400		DDR4-2666 / 2933 / 3200		Unit	Notes
		Min	Max	Min	Max		
Differential input high	V_{IHdiff}	0.150	Note 3	0.120	Note 3	V	1
Differential input low	V_{ILdiff}	Note 3	–0.150	Note 3	-0.120	V	1
Differential input high (AC)	$V_{IHdiff(AC)}$	$2 \times (_{IH(AC)} - V_{REF})$	Note 3	$2 \times (V_{IH(AC)} - V_{REF})$	Note 3	V	2
Differential input low (AC)	$V_{ILdiff(AC)}$	Note 3	$2 \times (V_{IL(AC)} - V_{REF})$	Note 3	$2 \times (V_{IL(AC)} - V_{REF})$	V	2

Notes: 1. Used to define a differential signal slew-rate.
2. For CK_t, CK_c use $V_{IH(AC)}$ and $V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
3. These values are not defined; however, the differential signals (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

TABLE 25: MINIMUM TIME AC TIME ^{T}DVAC FOR CK

Slew Rate (V/ns)	^{t}tDVAC (ps) at $\lvert V_{IH,diff(AC)}$ to $V_{IL,diff(AC)}\rvert$	
	200mV	TBDmV
>4.0	120	TBD
4.0	115	TBD
3.0	110	TBD
2.0	105	TBD
1.9	100	TBD
1.6	95	TBD
1.4	90	TBD
1.2	85	TBD
1.0	80	TBD
<1.0	80	TBD

Note: 1. Below $V_{IL(AC)}$.

Single-Ended Requirements for CK Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has to comply with certain requirements for single-ended signals. CK_t and CK_c have to reach approximately $V_{SEHmin}/V_{SEL,max}$, which are approximately equal to the AC levels $V_{IH(AC)}$ and $V_{IL(AC)}$ for ADD/CMD signals in every half-cycle. The applicable AC levels for ADD/CMD might differ per speed-bin, and so on. For example, if a value other than 100mV is used for ADD/CMD $V_{IH(AC)}$ and $V_{IL(AC)}$ signals, then these AC levels also apply for the singleended signals CK_t and CK_c.

While ADD/CMD signal requirements are with respect to V_{REFCA}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL,max}/V_{SEH,min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Figure 25: Single-Ended Requirements for CK

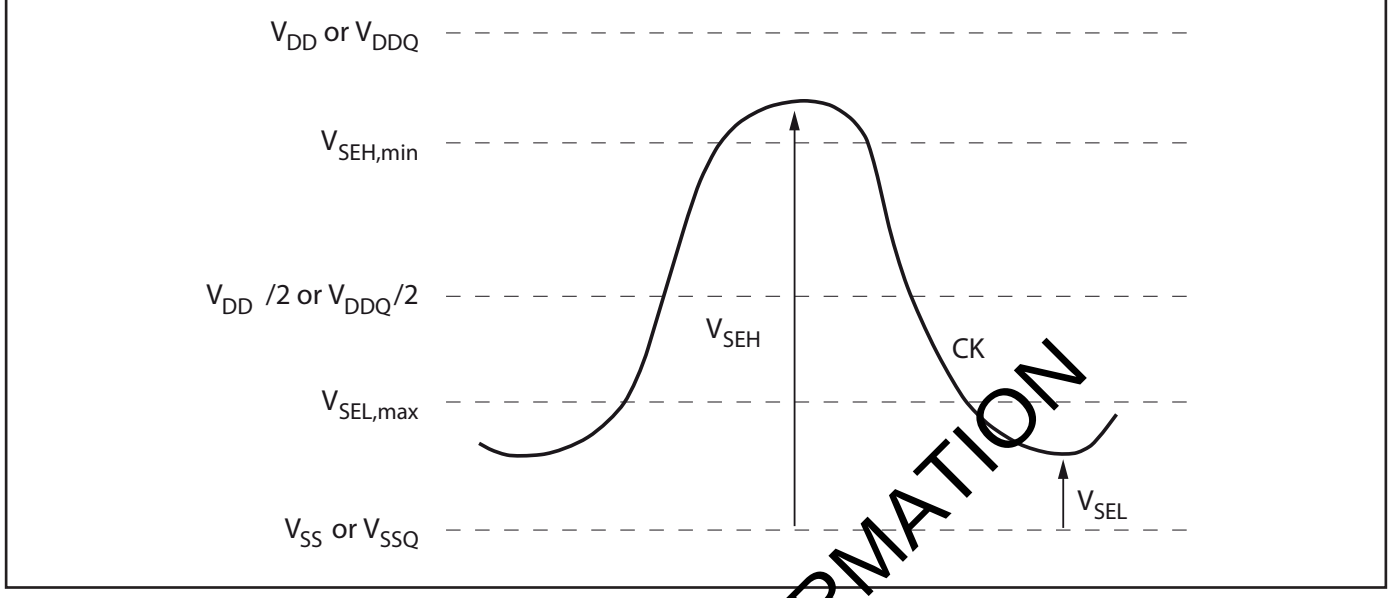


Table 26: Single-Ended Requirements for CK

Parameter	Symbol	DDR4-1600 / 1866 / 2133 / 2400		DDR4-2666 / 2933 / 3200		Unit	Notes
		Min	Max	Min	Max		
Single-ended high level for CK_t, CK_c	V_{SEH}	$V_{DD}/2$ + 0.100	Note 3	$V_{DD}/2$ + 0.90	Note 3	V	1, 2
Single-ended low level for CK_t, CK_c	V_{SEL}	Note 3	$V_{DD}/2$ - 0.100	Note 3	$V_{DD}/2$ - 0.90	V	1, 2

Notes:
1. For CK_t, CK_c use $V_{IH(AC)}$ and $V_{IL(AC)}$ of ADD/CMD and V_{REFCA}.
2. ADDR/CMD $V_{IH(AC)}$ and $V_{IL(AC)}$ based on V_{REFCA}.
3. These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, $V_{IH(DC)max}$ and $V_{IL(DC)min}$ for single-ended signals as well as the limitations for overshoot and undershoot.

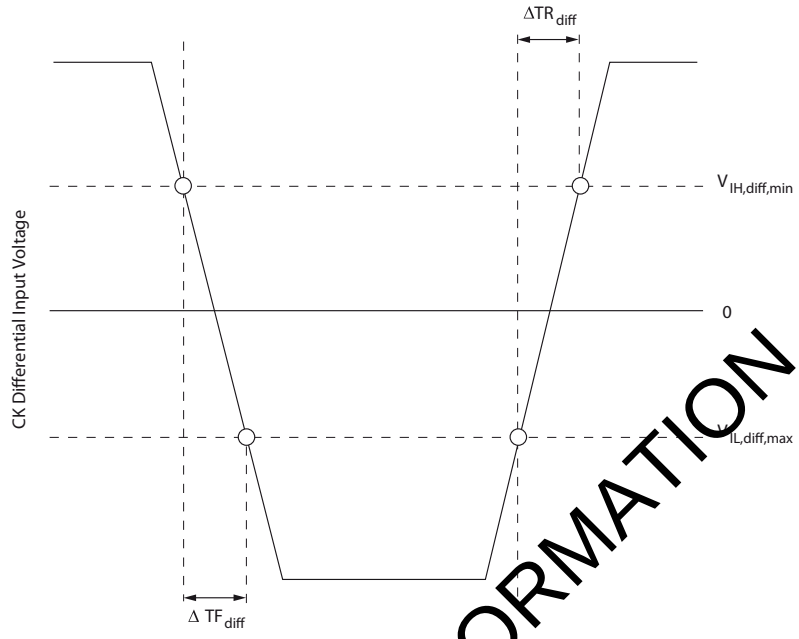
Slew Rate Definitions for CK Differential Input Signals

Table 27: CK Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge	$V_{IL,diff,max}$	$V_{IH,diff,min}$	$\lvert V_{IH,diff,min} - V_{IL,diff,max}\rvert / \Delta TR_{diff}$
Differential input slew rate for falling edge	$V_{IH,diff,min}$	$V_{IL,diff,max}$	$\lvert V_{IH,diff,min} - V_{IL,diff,max}\rvert / \Delta TR_{diff}$

Note: 1. The differential signal CK_t, CK_c must be monotonic between these thresholds.

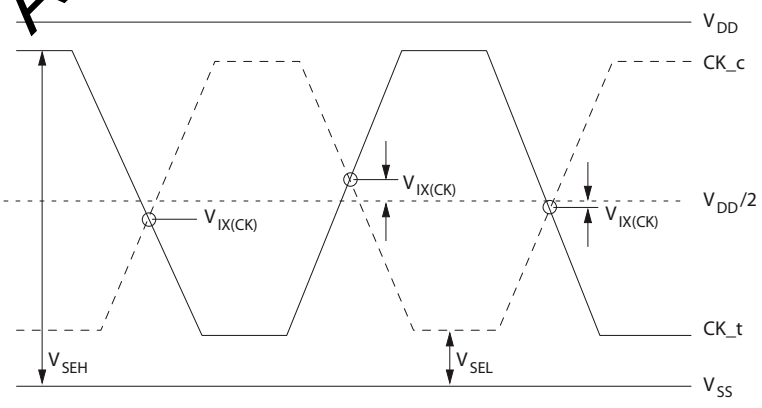
Figure 26: Differential Input Slew Rate Definition for CK_t, CK_c



CK Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signal CK_t, CK_c must meet the requirements shown below. The differential input cross point voltage $V_{IX(CK)}$ is measured from the actual cross point of true and complement signals to the midlevel between V_{DD} and VSS.

Figure 27: $V_{IX(CK)}$ Definition



Electrical Characteristics – AC and DC Differential Input Measurement Levels

Table 28: Cross Point Voltage For CK Differential Input Signals at DDR4-1600 through DDR4-2400

Parameter	Sym	Input Level	DDR4-1600, 1866, 2133		DDR4-2400	
			Min	Max	Min	Max
Differential input cross point voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{IX(CK)}$	$V_{SEH} > V_{DD}/2 + 145mV$	N/A	120mV	N/A	120mV
		$V_{DD}/2 + 100mV \le V_{SEH} \le V_{DD}/2 + 145mV$	N/A	$(V_{SEH} - V_{DD}/2) - 25mV$	N/A	$(V_{SEH} - V_{DD}/2) - 25mV$
		$V_{DD}/2 - 145mV \le V_{SEL} \le V_{DD}/2 - 100mV$	$-(V_{DD}/2-V_{SEL}) + 25mV$	N/A	$-(V_{DD}/2-V_{SEL}) + 25mV$	N/A
		$V_{SEL} \le V_{DD}/2 - 145mV$	–120mV	N/A	–120mV	N/A

Table 29: Cross Point Voltage For CK Differential Input Signals at DDR4-2666 through DDR4-3200

Parameter	Sym	Input Level	DDR4-2666		DDR4-2933, 3200	
			Min	Max	Min	Max
Differential input cross point voltage relative to $V_{DD}/2$ for CK_t, CK_c	$V_{IX(CK)}$	$V_{SEH} > V_{DD}/2 + 135mV$	N/A	110mV	N/A	110mV
		$V_{DD}/2 + 90mV \le V_{SEH} \le V_{DD}/2 + 135mV$	N/A	$(V_{SEH} - V_{DD}/2) - 30mV$	N/A	$(V_{SEH} - V_{DD}/2) - 30mV$
		$V_{DD}/2 - 135mV \le V_{SEL} \le V_{DD}/2 - 90mV$	$-(V_{DD}/2-V_{SEL}) + 30mV$	N/A	$-(V_{DD}/2-V_{SEL}) + 30mV$	N/A
		$V_{SEL} \le V_{DD}/2 - 135mV$	–110mV	N/A	–110mV	N/A

DQS Differential Input Signal Definition and Swing Requirements

Figure 28: Differential Input Signal Definition for DQS_t, DQS_c

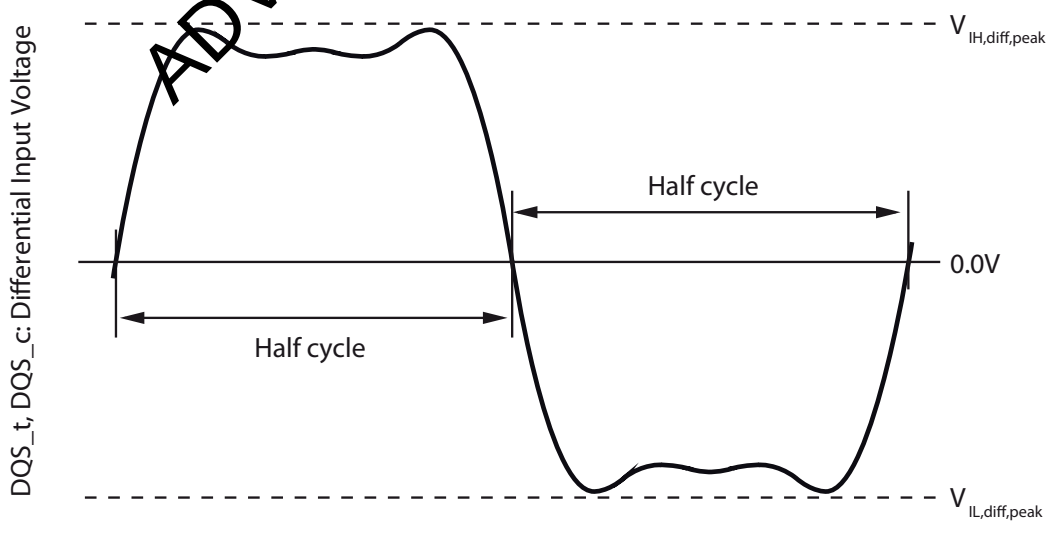


Table 30: DDR4-1600 through DDR4-2400 Differential Input Swing Requirements for DQS_t, DQS_c

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	186	V_{DDQ}	160	V_{DDQ}	mV	1 , 2
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–186	V_{SSQ}	–160	mV	1 , 2

Notes:
1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

Table 31: DDR4-2633 through DDR4-3200 Differential Input Swing Requirements for DQS_t, DQS_c

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	150V	V_{DDQ}	145V	V_{DDQ}	140	V_{DDQ}	mV	1 , 2
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–150	V_{SSQ}	–145	V_{SSQ}	–140	mV	1 , 2

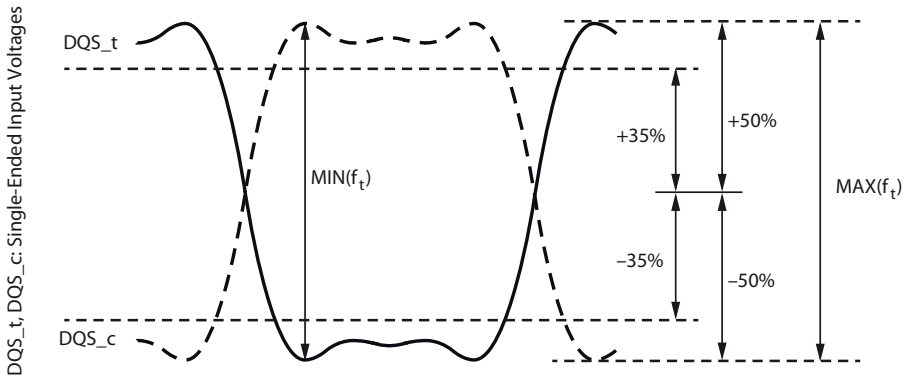
Notes:
1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

The peak voltage of the DQS signals are calculated using the following equations:

$V_{IH,dif,Peak}$ voltage = MAX(ft)
$V_{IL,dif,Peak}$ voltage = MIN(ft)
(ft) = DQS_t, DQS_c.

The MAX(f(t)) or MIN(f(t)) used to determine the midpoint from which to reference the 35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.

Figure 29: DQS_t, DQS_c Input Peak Voltage Calculation and Range of Exempt non-Monotonic Signaling



DQS Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet $V_{IX\_DQS,ratio}$ in the table below. The differential input cross point voltage V_{IX_DQS} ($V_{IX\_DQS\_FR}$ and $V_{IX\_DQS\_RF}$) is measured from the actual cross point of DQS_t, DQS_c relative to the $V_{DQS,mid}$ of the DQS_t and DQS_c signals.

$V_{DQS,mid}$ is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by V_{DQS_trans}. V_{DQS_trans} is the difference between the lowest horizontal tangent above $V_{DQS,mid}$ of the transitioning DQS signals and the highest horizontal tangent below $V_{DQS,mid}$ of the transitioning DQS signals. A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within ±35% of the midpoint of either $V_{IH.DIFF.Peak}$ voltage (DQS_t rising) or $V_{IL.DIFF.Peak}$ voltage (DQS_c rising), as shown in the figure below.

A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in the figure below), and a ring-back's horizontal tangent is derived from its positive slope to zero slope transition (point B in the figure below) and is not a valid horizontal tangent; a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in the figure below), and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in the figure below) and is not a valid horizontal tangent.

Figure 30: V_{IXDQS} Definition

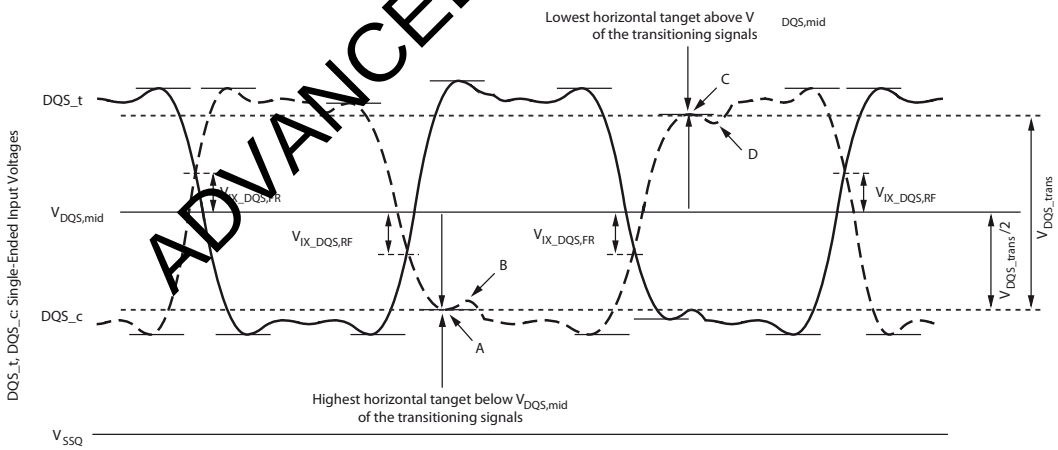


Table 32: Cross Point Voltage For Differential Input Signals DQS

Parameter	Symbol	DDR4-1600, 1866, 2133, 2400, 2666, 2933, 3200		Unit	Notes
		Min	Max		
DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	$V_{IX\_DQS,ratio}$	–	25	%	1, 2

Table 32: Cross Point Voltage For Differential Input Signals DQS (Continued)

Parameter	Symbol	DDR4-1600, 1866, 2133, 2400, 2666, 2933, 3200 Min	Max	Unit	Notes
$V_{DQS,mid}$ to $V_{cent(midpoint)}$ offset	V_{DQS,mid_to_Vcent}	–	Note 3	mV	2

Notes:
1. VIX_DQS,ratio is DQS VIX crossing (VIX_DQS,FR or VIX_DQS,RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQS,midd of the transitioning DQS signals and the highest horizontal tangent below VDQS,mid of the transitioning DQS signals.
2. VDQS,mid will be similar to the VREFDQ internal setting value (Vcent(midpoint) offset) obtained during VREF Training if the DQS and DQs drivers and paths are matched.
3. The maximum limit shall not exceed the smaller of VIH,diff,DQS minimum limit or 50mV.

Slew Rate Definitions for DQS Differential Input Signals

Table 33: DQS Differential Input Slew Rate Definition

Description	Measured From	To	Defined by
Differential input slew rate for rising edge	$V_{IL,diff,DQS}$	$V_{IH,diff,DQS}$	$\lvert V_{IH,diff,DQS} - V_{IL,diff,DQS}\rvert / \Delta TR_{diff}$
Differential input slew rate for falling edge	$V_{IH,diff,DQS}$	$V_{IL,diff,DQS}$	$\lvert V_{IHdiffDQS} - V_{IL,diff,DQS}\rvert / \Delta TR_{diff}$

Note: 1. The differential signal DQS_t, DQS_c must be monotonic between these thresholds.

Figure 31: Differential Input Slew Rate and Input Level Definition for DQS_t, DQS_c

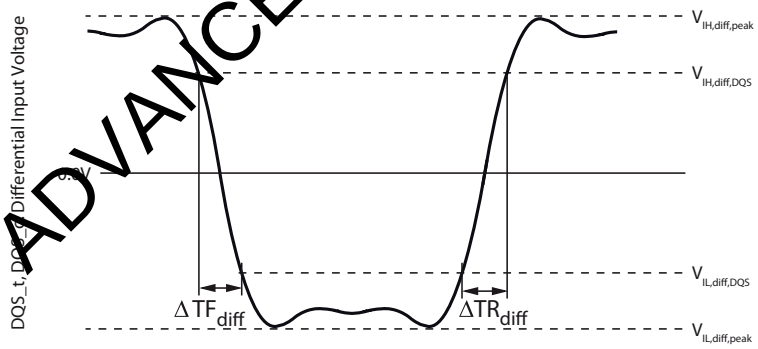


Table 34: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c

Parameter	Symbol	DDR4-1600, 1866, 2133 Min	DDR4-1600, 1866, 2133 Max	DDR4-2400 Min	DDR4-2400 Max	Unit	Notes
Peak differential input high voltage	$V_{IH,diff,peak}$	186	V_{DDQ}	160	V_{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	136	–	130	–	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	–	–136	–	–130	mV	2, 3

Table 34: DDR4-1600 through DDR4-2400 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c (Continued)

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max		
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–186	V_{SSQ}	–160	mV	1
DQS differential input slew rate	SRIdiff	3.0	18	3.0	18	V/ns	4, 5

Notes:
1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
4. Differential input slew rate for rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|\Delta TR_{diff}$.
5. 5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|\Delta TR_{diff}$.

Table 35: DDR4-2666 through DDR4-3200 Differential Input Slew Rate and Input Levels for DQS_t, DQS_c

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Peak differential input high voltage	$V_{IH,diff,peak}$	150	V_{DDQ}	145	V_{DDQ}	140	V_{DDQ}	mV	1
Differential input high voltage	$V_{IH,diff,DQS}$	120	–	115	–	110	–	mV	2, 3
Differential input low voltage	$V_{IL,diff,DQS}$	–	–120	–	–115	–	–110	mV	2, 3
Peak differential input low voltage	$V_{IL,diff,peak}$	V_{SSQ}	–150	V_{SSQ}	–145	V_{SSQ}	–140	mV	1
DQS differential input slew rate		3.0	18	3.0	18	3.0	18	V/ns	4, 5

Notes:
1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Differential signal rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ must be monotonic slope.
3. Differential signal falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ must be monotonic slope.
4. Differential input slew rate for rising edge from $V_{IL,diff,DQS}$ to $V_{IH,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|\Delta TR_{diff}$.
5. Differential input slew rate for falling edge from $V_{IH,diff,DQS}$ to $V_{IL,diff,DQS}$ is defined by $|V_{IL,diff,min} - V_{IH,diff,max}|\Delta TF_{diff}$.

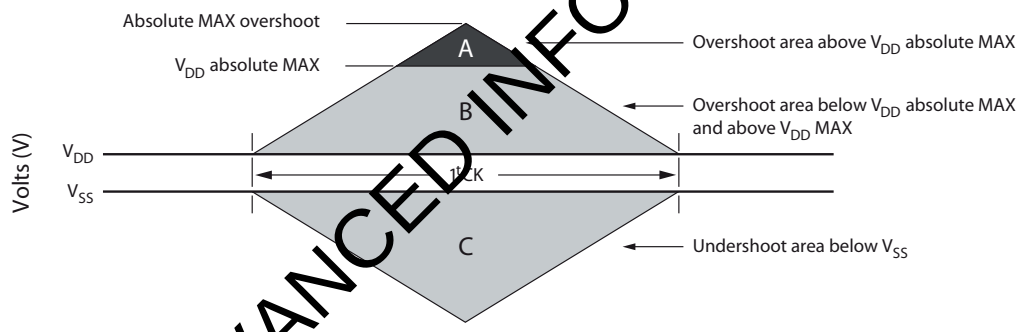
Electrical Characteristics – Overshoot and Undershoot Specifications

Address, Command, and Control Overshoot and Undershoot Specifications

Table 36: ADDR, CMD, CNTL Overshoot and Undershoot/Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
Address and control pins (A[17:0], BG[1:0], BA[1:0], CS_n, RAS_n, CAS_n, WE_n, CKE, ODT, C2-0)							
Area A: Maximum peak amplitude above V_{DD} absolute MAX	0.06	0.06	0.06	0.06	TBD	TBD	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	TBD	TBD	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SS}	0.30	0.30	0.30	0.30	TBD	TBD	V
Area A maximum overshoot area per 1^tCK	0.0083	0.0071	0.0062	0.0055	TBD	TBD	V/ns
Area B maximum overshoot area per 1^tCK	0.2550	0.2185	0.1914	0.1699	TBD	TBD	V/ns
Area C maximum undershoot area per 1^tCK	0.2644	0.2265	0.1984	0.1762	TBD	TBD	V/ns

Figure 32: ADDR, CMD, CNTL Overshoot and Undershoot Definition

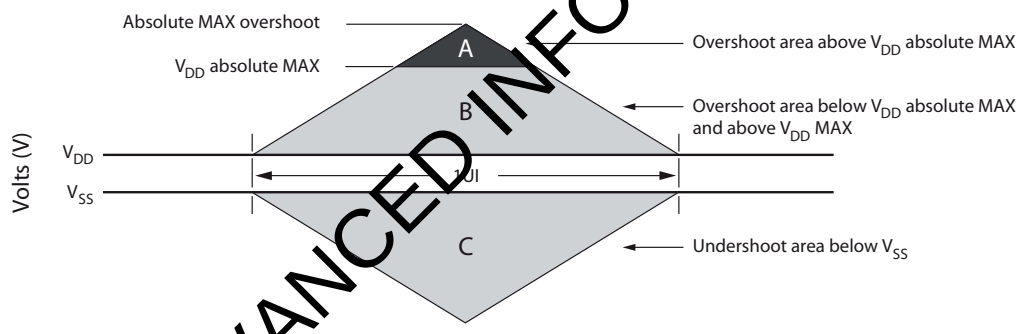


Clock Overshoot and Undershoot Specifications

Table 37: CK Overshoot and Undershoot/ Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
CK_t, CK_c							
Area A: Maximum peak amplitude above V_{DD} absolute MAX	0.06	0.06	0.06	0.06	TBD	TBD	V
Area B: Amplitude allowed between V_{DD} and V_{DD} absolute MAX	0.24	0.24	0.24	0.24	TBD	TBD	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SS}	0.30	0.30	0.30	0.30	TBD	TBD	V
Area A maximum overshoot area per 1UI	0.0038	0.0032	0.0028	0.0025	TBD	TBD	V/ns
Area B maximum overshoot area per 1UI	0.1125	0.0964	0.0844	0.0750	TBD	TBD	V/ns
Area C maximum undershoot area per 1UI	0.1144	0.0980	0.0858	0.0762	TBD	TBD	V/ns

Figure 33: CK Overshoot and Undershoot Definition

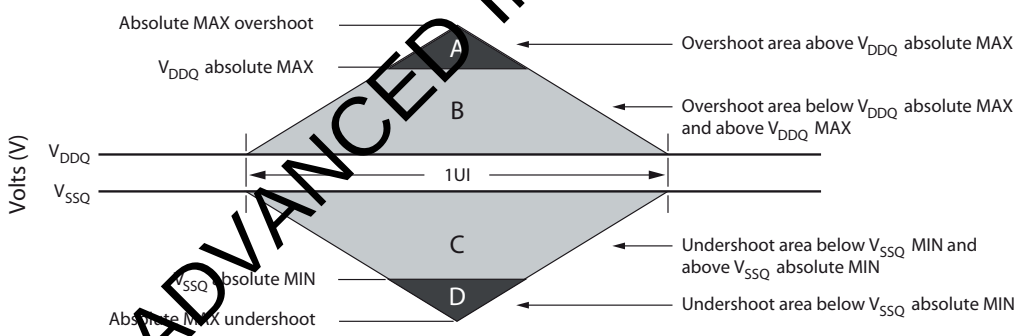


Data, Strobe, and Mask Overshoot and Undershoot Specifications

Table 38: Data, Strobe, and Mask Overshoot and Undershoot/ Specifications

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	Unit
Data, Strobe, and Mask							
Area A: Maximum peak amplitude above V_{DDQ} absolute MAX	0.16	0.16	0.16	0.16	TBD	TBD	V
Area B: Amplitude allowed between V_{DDQ} and V_{DDQ} absolute MAX	0.24	0.24	0.24	0.24	TBD	TBD	V
Area C: Maximum peak amplitude allowed for undershoot below V_{SSQ}	0.30	0.30	0.30	0.30	TBD	TBD	V
Area D: Maximum peak amplitude below V_{SSQ} absolute MIN	0.10	0.10	0.10	0.10	TBD	TBD	V
Area A maximum overshoot area per 1UI	0.0150	0.0129	0.0113	0.0100	TBD	TBD	V/ns
Area B maximum overshoot area per 1UI	0.1050	0.0900	0.0788	0.0700	TBD	TBD	V/ns
Area C maximum undershoot area per 1UI	0.1050	0.0900	0.0788	0.0700	TBD	TBD	V/ns
Area D maximum undershoot area per 1UI	0.0150	0.0129	0.0113	0.0100	TBD	TBD	V/ns

Figure 34: Data, Strobe, and Mask Overshoot and Undershoot Definition



Electrical Characteristics – AC and DC Output Measurement Levels

Single-Ended Outputs

Table 39: Single-Ended Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	$1.1 \times V_{DDQ}$	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	$0.5 \times V_{DDQ}$	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	$(0.7 + 0.15) \times V_{DDQ}$	V

Electrical Characteristics – AC and DC Output Measurement Levels

Table 39: Single-Ended Output Levels (Continued)

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	$(0.7 - 0.15) \times V_{DDQ}$	V

Note: 1. The swing of ±0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for singleended signals.

Table 40: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)]} / \Delta TR_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)]} / \Delta TF_{se}$

Figure 35: Single-ended Output Slew Rate Definition

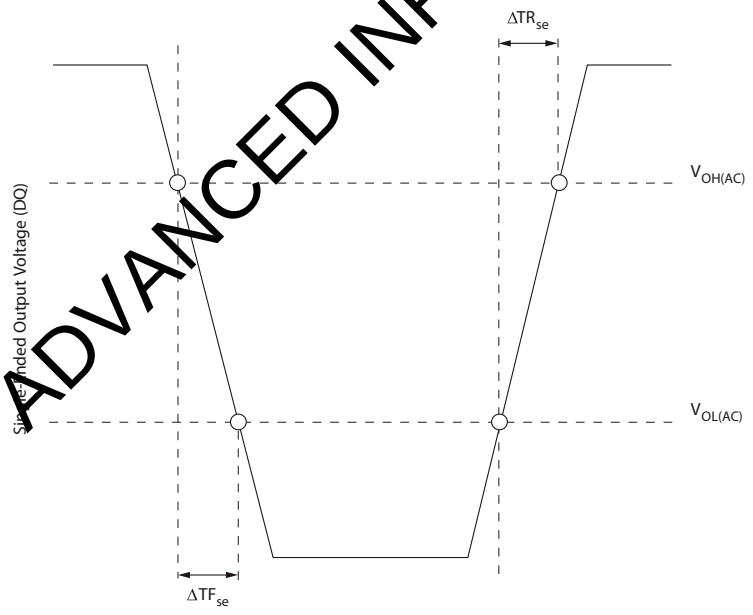


Table 41: Single-Ended Output Slew Rate

For $R_{ON} = R_{ZQ}/7$

Parameter	Symbol	DDR4-1333 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Single-ended output slew rate	SRQ_{se}	4	9	4	9	4	9	V/ns

Notes:
1. SR = slew rate; Q = query output; se = single-ended signals
2. In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane:
   - Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are static (they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from LOW-to-HIGH or HIGH-to-LOW, respectively). For the remaining DQ signal switching into the opposite direction, the standard maximum limit of 9 V/ns applies.

Differential Outputs

Table 42: Differential Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC differential output high measurement level (for output slew rate)	$V_{OH,diff(AC)}$	$0.3 \times V_{DDQ}$	V
AC differential output low measurement level (for output slew rate)	$V_{OL,diff(AC)}$	$-0.3 \times V_{DDQ}$	V

Note: 1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 43: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)]}/\Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)]}/\Delta TF_{diff}$

Figure 36: Differential Output Slew Rate Definition

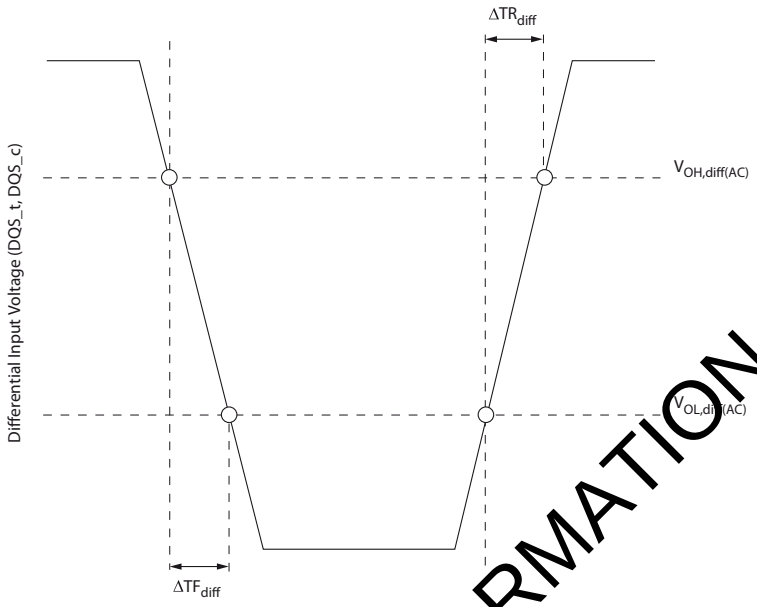


Table 44: Differential Output Slew Rate

For $R_{ON} = R_{ZQ}/7$

Parameter	Symbol	DDR4-1333 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQ_{diff}	8	18	8	18	8	18	V/ns

Note: 1. SR = slew rate; Q = query output; diff = differential signals.

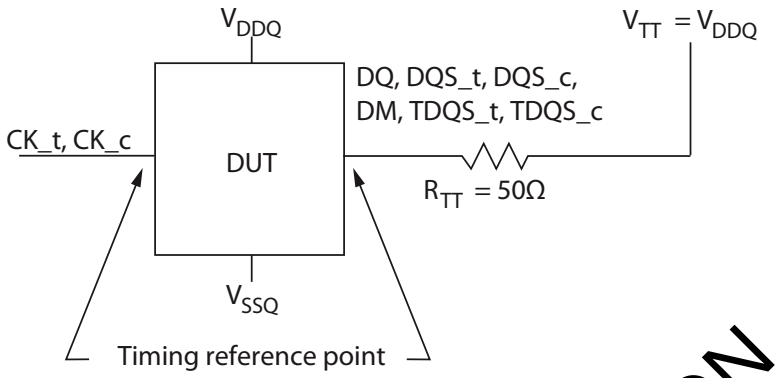
Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to $V_{TT} = V_{DDQ}$ and driver impedance of RZQ/7 for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing paraeter values of the device. The maximum DC High level of Output signal = $1.0 * V_{DDQ}$, the minimum DC Low level of Output signal = $\{ 34 / (34 + 50) \} * V_{DDQ} = 0.4 * V_{DDQ}$

The nominal reference level of an Output signal can be approximated by the following: The center of maximum DC High and minimum DC Low = $\{ (1 + 0.4) / 2 \} * V_{DDQ} = 0.7 * V_{DDQ}$. The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 37: Reference Load For AC Timing and Output Slew Rate



Connectivity Test Mode Output Levels

Table 45: Connectivity Test Mode Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	$1.1 \times V_{DDQ}$	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	$0.5 \times V_{DDQ}$	V
DC output below measurement level (for IV curve linearity)	$V_{OB(DC)}$	$0.2 \times V_{DDQ}$	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	$V_{TT} + (0.1 \times V_{DDQ})$	V
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	$V_{TT} - (0.1 \times V_{DDQ})$	V

Note: 1. Driver impedance of $R_{ZQ}/7$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Figure 38: Connectivity Test Mode Reference Test Load

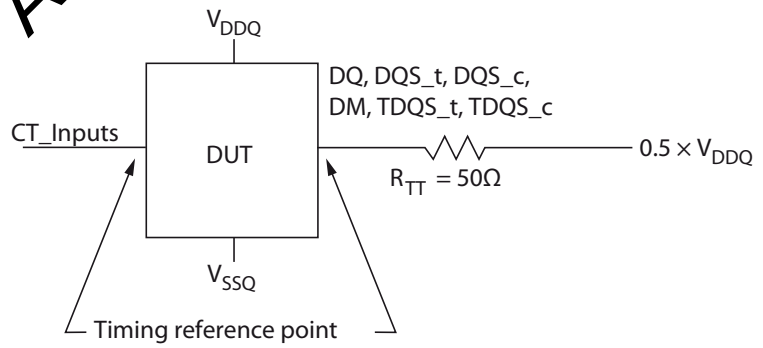


Figure 39: Connectivity Test Mode Output Slew Rate Definition

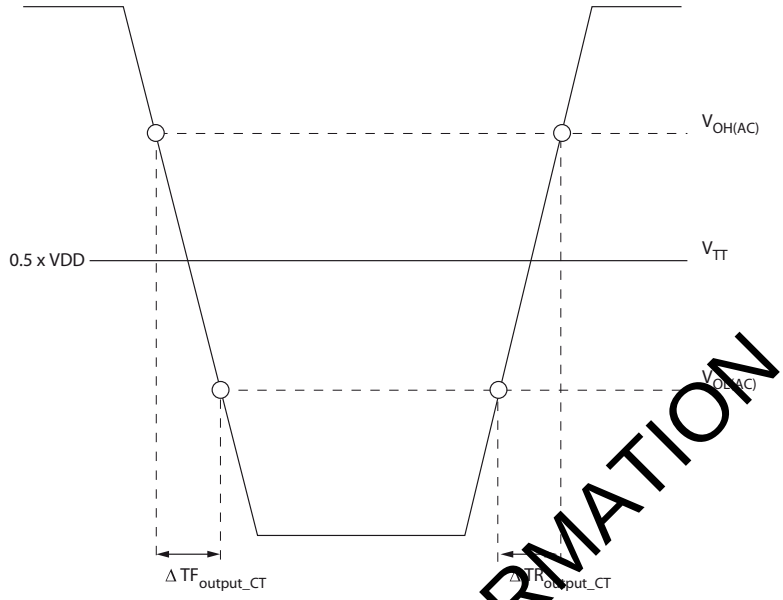


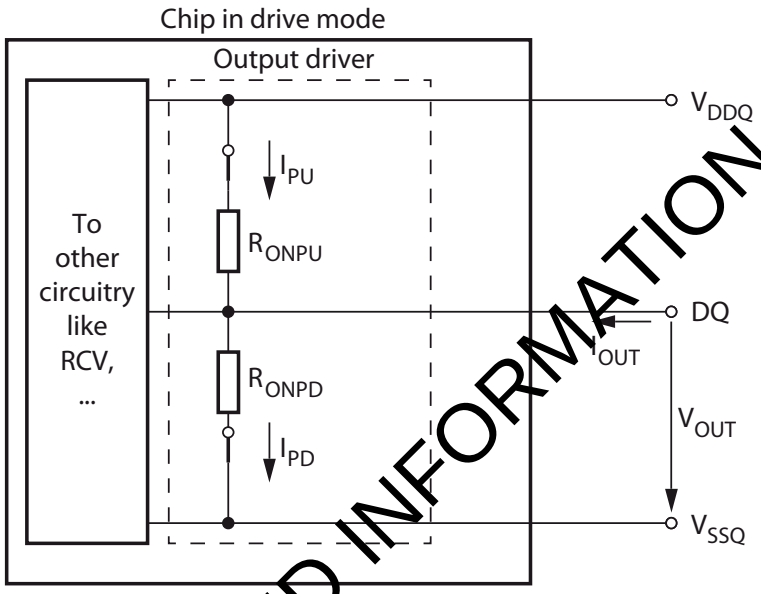
Table 46: Connectivity Test Mode Output Slew Rate

Parameter	Symbol	DDR4-1333 / 1866 / 2133 / 2400		DDR4-2666		DDR4-2933 / 3200		Unit
		Min	Max	Min	Max	Min	Max	
Output signal falling time	TF_output_CT	–	10	–	10	–	10	ns/V
Output signal rising time	TR_output_CT	–	10	–	10	–	10	ns/V

Output Driver Electrical Characteristics

The DDR4 driver supports two R_{ON} values. These R_{ON} values are referred to as strong mode (low R_{ON}: 34Ω) and weak mode (high R_{ON}: 48Ω). A functional representation of the output buffer is shown in the figure below.

Figure 40: Output Driver: Definition of Voltages and Currents



The output driver impedance, R_{ON}, is determined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON(34)} = R_{ZQ}/7$, or $R_{ON(48)} = R_{ZQ}/5$. This provides either a nominal 34.3Ω ±10% or 48Ω ±10% with nominal R_{ZQ} = 240Ω.

The individual pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}) are defined as follows:

R_{ONPu} when R_{ONPd} is off:

$$R_{ONPU} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{|I_{OUT}|}$$

Electrical Characteristics – AC and DC Output Driver Characteristics

Table 47: Strong Mode (34Ω) Output Driver Electrical Characteristics

Assumes R_{ZQ} = 240Ω; Entire operating temperature range after proper ZQ calibration

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Nim	Max	Unit	Notes
34Ω	R_{ON34PD}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2, 3
	R_{ON34PU}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1.0	1.25	$R_{ZQ}/7$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
Mismatch between DQ to DQ within byte variation pull-up, MM_{PUdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–10	–	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MMP_{PDdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–	–	10	%	1, 2, 3, 4, 6, 7
Mismatch between pull-up and pull-down, MM_{PUPD}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–	–	10	%	1, 2, 3, 4, 6, 7

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Micron recommends calibrating pull-down and pull-up output driver impedances at 0.8 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at 0.5 × V_{DDQ} and 1.1 V_{DDQ}.
4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure both R_{ONPU} and R_{ONPD} at 0.8 × V_{DDQ} separately; RON,nom is the nominal R_{ON} value.

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

6. RON variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:

$$MM_{PUDD} = \frac{R_{ONPU,\,max} - R_{ONPU,\,min}}{R_{ON,nom}} \times 100$$

$$MM_{PDDD} = \frac{R_{ONPU,\,max} - R_{ONPU,\,min}}{R_{ON,nom}} \times 100$$

7. The lower and upper bytes of a x16 are each treated on a per byte basis.
8. For IT and AT devices, the minimum values are derated by 9% when the device operates between –40°C and 0°C (TC).

Table 48: Weak Mode (48Ω) Output Driver Electrical Characteristics

Assumes R_{ZQ} = 240Ω; Entire operating temperature range after proper ZQ calibration

$R_{ON,nom}$	Resistor	V_{OUT}	Min	Nim	Max	Unit	Notes
48Ω	R_{ON34PD}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2, 3
	R_{ON34PU}	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1.0	1.25	$R_{ZQ}/5$	1, 2, 3
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/5$	1, 2, 3
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1.0	1.1	$R_{ZQ}/5$	1, 2, 3
Mismatch between DQ to DQ within byte variation pull-up, MM_{PUdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–10	–	10	%	1, 2, 3, 4, 5
Mismatch between DQ to DQ within byte variation pull-down, MM_{PDdd}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–	–	10	%	1, 2, 3, 4, 6. 7
Mismatch between pull-up and pull-down, MM_{PUPD}		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	–	–	10	%	1, 2, 3, 4, 6. 7

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Micron recommends calibrating pull-down and pull-up output driver impedances at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity specification shown above; for example, calibration at $0.5 \times V_{DDQ}$ and $1.1\ V_{DDQ}$.
4. DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. Measurement definition for mismatch between pull-up and pull-down, MM_{PUPD}: Measure both R_{ONPU} and R_{ONPD} at $0.8 \times V_{DDQ}$ separately; RON,nom is the nominal R_{ON} value:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ON,nom}} \times 100$$

6. RON variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c:

$$MM_{PUDD} = \frac{R_{ONPU,\,max} - R_{ONPU,\,min}}{R_{ON,nom}} \times 100$$

$$MM_{PDDD} = \frac{R_{ONPU,\,max} - R_{ONPU,\,min}}{R_{ON,nom}} \times 100$$

7. The lower and upper bytes of a x16 are each treated on a per byte basis.
8. For IT and AT devices, the minimum values are derated by 9% when the device operates between –40°C and 0°C (TC).

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@ calibration)$; $V_{DD} = V_{DDQ}$

Table 49: Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
R_{ONPU} @ $V_{OH(DC)}$	0.6 - $dR_{ON}dTH \times \lvert\Delta T\rvert$ - $dR_{ON}dVH \times \lvert\Delta V\rvert$	1.1 _ $dR_{ON}dTH \times \lvert\Delta T\rvert$ + $dR_{ON}dVH \times \lvert\Delta V\rvert$	$R_{ZQ}/6$
R_{ON} @ $V_{OM(DC)}$	0.9 - $dR_{ON}dTM \times \lvert\Delta T\rvert$ - $dR_{ON}dVM \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTM \times \lvert\Delta T\rvert$ + $dR_{ON}dVM \times \lvert\Delta V\rvert$	$R_{ZQ}/6$
R_{ONPD} @ $V_{OL(DC)}$	0.6 - $dR_{ON}dTL \times \lvert\Delta T\rvert$ - $dR_{ON}dVL \times \lvert\Delta V\rvert$	1.1 + $dR_{ON}dTL \times \lvert\Delta T\rvert$ + $dR_{ON}dVL \times \lvert\Delta V\rvert$	$R_{ZQ}/6$

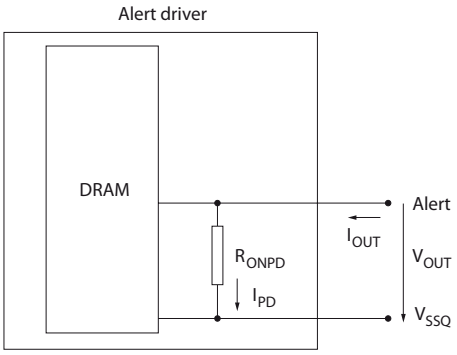
Table 50: Output Driver Voltage and Temperature Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV

Alert Driver

A functional representation of the alert output buffer is shown in the figure below. Output driver impedance, R_{ON}, is defined as follows.

Figure 41: Alert Driver



R_{ONPD} when R_{ONPU} is off:

$$R_{ONPD} = \frac{V_{OUT}}{\lvert I_{OUT} \rvert}$$

Electrical Characteristics – On-Die Termination Characteristics

Table 51: Alert Driver Voltage

$R_{ON,nom}$	Register	V_{OUT}	Min	Nom	Max	Unit
N/A	R_{ONPD}	$V_{OL(DC)} = 0.1 \times V_{DDQ}$	0.3	N/A	1.2	$R_{ZQ}/7$
		$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.4	N/A	1.12	$R_{ZQ}/7$
		$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.4	N/A	1.4	$R_{ZQ}/7$

Electrical Characteristics – On-Die Termination Characteristics

ODT Levels and I-V Characteristics

On-die termination (ODT) effective resistance settings are defined and can be selected by any or all of the following options:

- MR1[10:8] ($R_{TT(NOM)}$): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.
- MR2[11:9] ($R_{TT(WR)}$): Disable, 240 ohms,120 ohms, and 80 ohms.
- MR5[8:6] ($R_{TT(Park)}$): Disable, 240 ohms, 120 ohms, 80 ohms, 60 ohms, 48 ohms, 40 ohms, and 34 ohms.

ODT is applied to the following inputs:

- x4: DQ, DM_n, DQS_t, and DQS_c inputs.
- x8: DQ, DM_n, DQS_t, DQS_c, TDQS_t, and TDQS_c inputs.
- x16: DQ, LDM_n, UDM_n, LDQS_t, LDQS_c, UDQS_t, and UDQS_c inputs.

A functional representation of ODT is shown in the figure below.

Figure 42: ODT Definition of Voltages and Currents

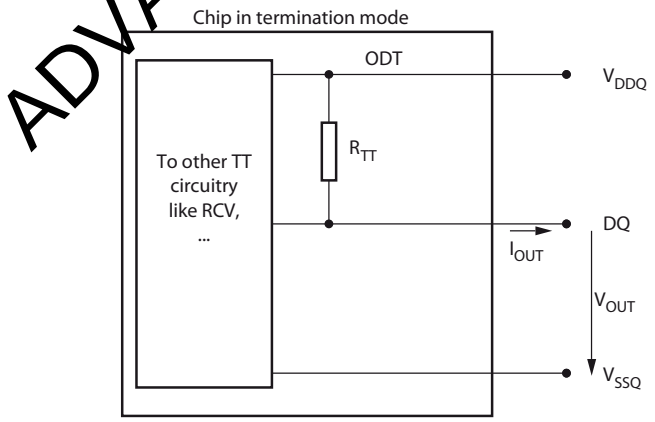


Table 52: ODT DC Characteristics

R_{TT}	V_{OUT}	Min	Nom	Max	Unit	Notes
240 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	R_{ZQ}	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	R_{ZQ}	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	R_{ZQ}	1, 2, 3
120 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/2$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/2$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/2$	1, 2, 3
80 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/3$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/3$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/3$	1, 2, 3
60 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/4$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/4$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/4$	1, 2, 3
48 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1, 2, 3
40 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/6$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/6$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/6$	1, 2, 3
34 ohm	$V_{OL(DC)} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1, 2, 3
	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1, 2, 3
	$V_{OH(DC)} = 1.1 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1, 2, 3
DQ-to-DQ mismatch within byte	$V_{OM(DC)} = 0.8 \times V_{DDQ}$	0	–	10	%	1, 2, 4, 5, 6

Notes:
1. The tolerance limits are specified after calibration to 240 ohm ±1% resistor with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see ODT Temperature and Voltage Sensitivity.
2. Micron recommends calibrating pull-up ODT resistors at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity specification shown here.
3. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and $V_{SSQ} = V_{SS}$.
4. The DQ-to-DQ mismatch within byte variation for a given component including DQS_t and DQS_c.
5. RTT variance range ratio to R_{TT} nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-to-DQ mismatch} = \frac{R_{TT(MAX)} - R_{TT(MIN)}}{R_{TT(NOM)}} \times 100$$

6. DQ-to-DQ mismatch for a x16 device is treated as two separate bytes.
7. For IT and AT devices, the minimum values are derated by 9% when the device operates between –40°C and 0°C (TC).

ODT Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following equations and tables.

$\Delta T = T - T(@\ calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@\ calibration)$; $V_{DD} = V_{DDQ}$

Table 53: ODT Sensitivity Definitions

Parameter	Min	Max	Unit
$R_{TT}@$	$0.9 - dR_{TT}dT \times \lvert\Delta T\rvert - dR_{TT}dV \times \lvert\Delta V\rvert$	$1.6 + dR_{TT}dTH \times \lvert\Delta T\rvert + dR_{TT}dVH \times \lvert\Delta V\rvert$	R_{ZQ}/n

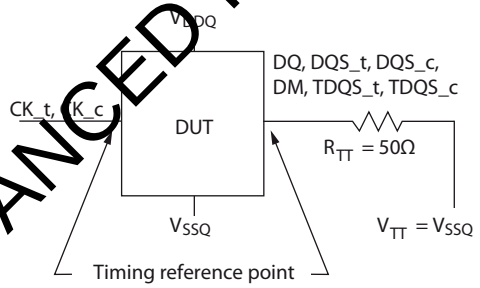
Table 54: ODT Voltage and Temperature Sensitivity

Parameter	Min	Max	Unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

Figure 43: ODT Timing Reference Load



ODT Timing Definitions and Waveforms

Definitions for ^{t}ADC, ^{t}AONAS, and ^{t}AOFAS are provided in the Table 122 (page 292) and shown in Figure 230 (page 293) and Figure 232 (page 294). Measurement reference settings are provided in the subsequent Table 123 (page 292).

The ^{t}ADC for the dynamic ODT case and read disable ODT cases are represented by ^{t}ADC of Direct ODT Control case.

Table 55: ODT Timing Definitions

Parameter	Begin Point Definition	End Point Definition	Figure
^{t}ADC	Rising edge of CK_t, CK_c defined by the end point of DODTLoff	Extrapolated point at $V_{RTT,nom}$	Figure 230 (page 293)
	Rising edge of CK_t, CK_c defined by the end point of DODTLon	Extrapolated point at V_{SSQ}	Figure 230 (page 293)
	Rising edge of CK_t, CK_c defined by the end point of ODTLcnw	Extrapolated point at $V_{RTT,nom}$	Figure 231 (page 293)
	Rising edge of CK_t, CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at V_{SSQ}	Figure 231 (page 293)
^{t}AONAS	Rising edge of CK_t, CK_c with ODT being first registered HIGH	Extrapolated point at V_{SSQ}	Figure 232 (page 294)
^{t}AOFAS	Rising edge of CK_t, CK_c with ODT being first registered LOW	Extrapolated point at $V_{RTT,nom}$	Figure 232 (page 294)

Table 56: Reference Settings for ODT Timing Measurements

Measure Parameter	$R_{TT(Park)}$	$R_{TT(NOM)}$	$R_{TT(WR)}$	VSW1	VSW2	Note
^{t}ADC	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 4
	–	$R_{ZQ}/7$ (34Ω)	High-Z	0.20V	0.40V	1, 3, 5
^{t}AONAS	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 6
^{t}AOFAS	Disable	$R_{ZQ}/7$ (34Ω)	–	0.20V	0.40V	1, 2, 6

Notes:
1. MR settings are as follows: MR1 has A10 = 1, A9 = 1, A8 = 1 for $R_{TT(NOM)}$ setting; MR5 has A8 = 0, A7 = 0, A6 = 0 for $R_{TT(Park)}$ setting; and MR2 has A11 = 0, A10 = 1, A9 = 1 for $R_{TT(WR)}$ setting.
2. ODT state change is controlled by ODT pin.
3. ODT state change is controlled by a WRITE command.
4. Refer to Figure 230 (page 293).
5. Refer to Figure 231 (page 293).
6. Refer to Figure 232 (page 294).

FIGURE 44: ^{T}ADC DEFINITION WITH DIRECT ODT CONTROL

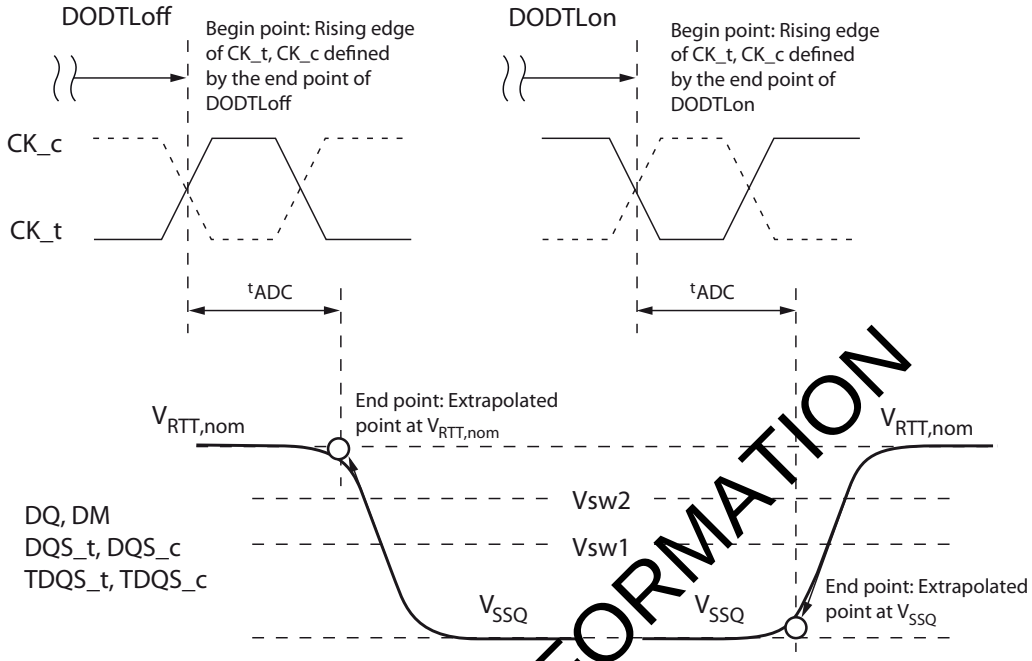


FIGURE 45: ^{T}ADC DEFINITION WITH DYNAMIC ODT CONTROL

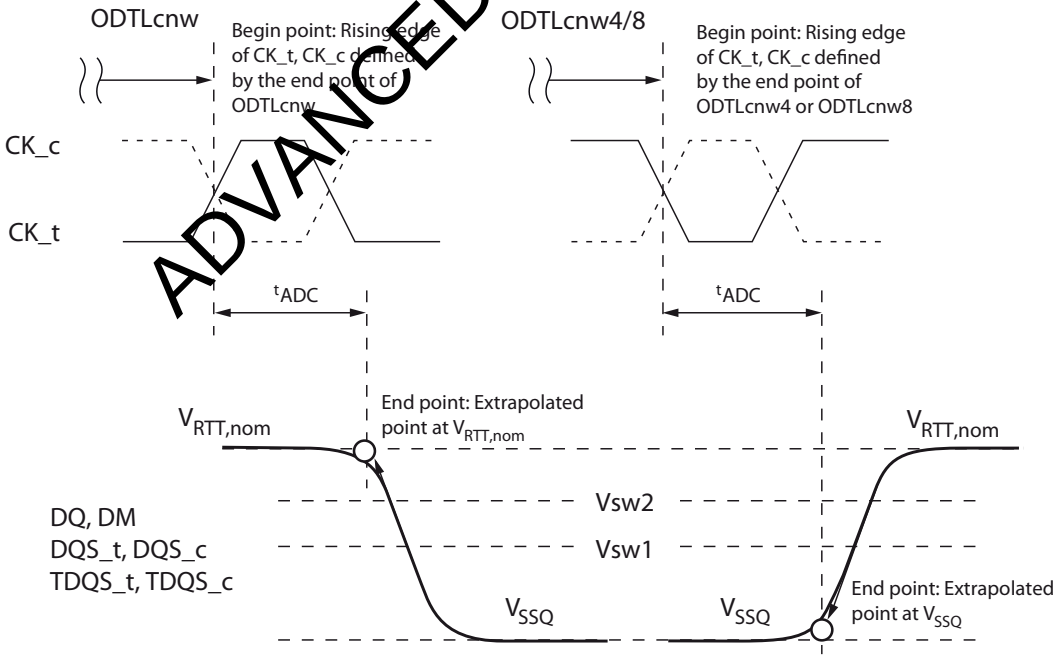


FIGURE 46: TAOFAS AND TAONAS DEFINITIONS

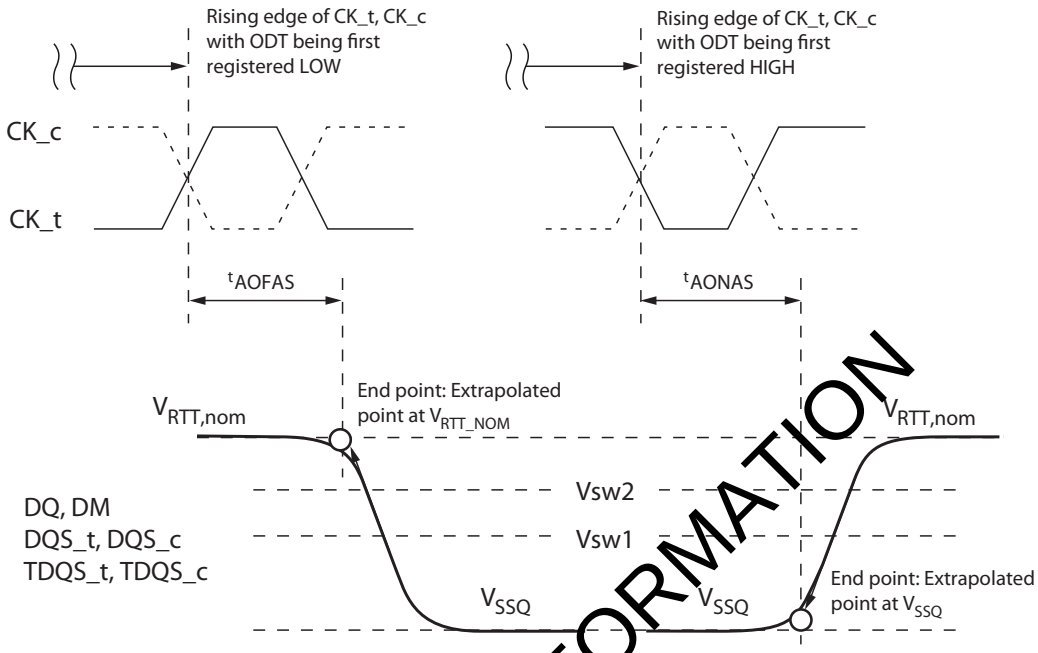


TABLE 57: DRAM PACKAGE ELECTRICAL SPECIFICATIONS

Parameter		Symbol	1600, 1866		2133, 2400		2666, 3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input/ output	Zpkg	Z_{IO}	45	85	45	85	TBD	TBD	ohm	1, 2, 4
	Package delay	Td_{IO}	14	45	14	45	TBD	TBD	ps	1, 3, 4
	Lpkg	L_{IO}	–	3.4	–	3.4	TBD	TBD	nH	
	Cpkg	C_{IO}	–	0.82	–	0.82	TBD	TBD	pF	
DQSL_t/ DQSL_c/ DQSU_t/ DQSU_c	Zpkg	$Z_{IO\ DQS}$	45	85	45	85	TBD	TBD	ohm	1, 2
	Package delay	$Td_{IO\ DQS}$	14	45	14	45	TBD	TBD	ps	1, 3
	Lpkg	$L_{IO\ DQS}$	–	3.4	–	3.4	TBD	TBD	nH	
	Cpkg	$C_{IO\ DQS}$	–	0.82	–	0.82	TBD	TBD	pF	
DQSL_t/ DQSL_c, DQSU_t/ DQSU_c,	Delta Zpkg	$DZ_{IO\ DQS}$	–	10	–	10	TBD	TBD	ohm	1, 2, 3
	Delta delay	$DTd_{IO\ DQS}$	–	5	–	5	TBD	TBD	ps	1, 3, 6
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	50	90	50	90	TBD	TBD	ohm	1, 2, 8
	Package delay	$Td_{I\ CTRL}$	14	42	14	42	TBD	TBD	ps	1, 3, 8
	Lpkg	$L_{I\ CTRL}$	–	3.4	–	3.4	TBD	TBD	nH	
	Cpkg	$C_{I\ CTRL}$	–	0.7	–	0.7	TBD	TBD	pF	
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	50	90	50	90	TBD	TBD	ohm	1, 2, 7
	Package delay	$Td_{I\ ADD\ CMD}$	14	52	14	52	TBD	TBD	ps	1, 3, 7
	Lpkg	$L_{I\ ADD\ CMD}$	–	3.9	–	3.9	TBD	TBD	nH	
	Cpkg	$C_{I\ ADD\ CMD}$	–	0.86	–	0.86	TBD	TBD	pF	
CK_t, CK_c	Zpkg	Z_{CK}	50	90	50	90	TBD	TBD	ohm	1, 2
	Package delay	Td_{CK}	14	42	14	42	TBD	TBD	ps	1, 3
	Delta Zpkg	DZ_{DCK}	–	10	–	10	TBD	TBD	ohm	1, 2, 5
	Delta delay	DTd_{DCK}	–	5	–	5	TBD	TBD	ps	1, 3, 5
Input CLK	Lpkg	$L_{I\ CLK}$	–	3.4	–	3.4	TBD	TBD	nH	
	Cpkg	$C_{I\ CLK}$	–	0.7	–	0.7	TBD	TBD	pF	
ZQ Zpkg		$Z_{O\ ZQ}$	40	100	40	100	TBD	TBD	ohm	1, 2
ZQ delay		$Td_{O\ ZQ}$	20	90	20	90	TBD	TBD	ps	1, 3
ALERT Zpkg		$Z_{O\ ALERT}$	40	100	40	100	TBD	TBD	ohm	1, 2
ALERT delay		$Td_{O\ ALERT}$	20	55	20	55	TBD	TBD	ps	1, 3

Notes:
1. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die, not pin, side.
2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).
3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
4. Z_{IO} and Td_{IO} apply to DQ, DM, DQS_c, DQS_t, TDQS_t, and TDQS_c.
5. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
6. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
7. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.
8. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
10. It is assumed that Lpkg can be approximated as Lpkg = Z_O × Td.
11. It is assumed that Cpkg can be approximated as Cpkg = Td/Z_O.

Table 58: Pad Input/Output Capacitance

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400, 2666		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{IO}	0.55	1.4	0.55	1.15	0.55	1.15	pF	1, 2, 3
Input capacitance: CK_t and CK_c	C_{CK}	0.2	0.8	0.2	0.7	0.2	0.7	pF	1, 2, 3, 4
Input capacitance delta: CK_t and CK_c	C_{DCK}	0	0.05	0	0.05	0	0.05	pF	1, 2, 3, 5
Input/output capacitance delta: DQS_t and DQS_c	C_{DDQS}	0	0.05	0	0.05	0	0.05	pF	1, 3
Input capacitance: CTRL, ADD, CMD input-only pins	C_{I}	0.2	0.8	0.2	0.7	0.2	0.7	pF	1, 3, 6
Input capacitance delta: All CTRL input-only pins	C_{DI_CTRL}	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 3, 7
Input capacitance delta: All ADD/CMD input-only pins	$C_{DI\_ADD\_CMD}$	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 3, 8, 9
Input/output capacitance delta: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{DIO}	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 10, 11
Input/output capacitance: ALERT pin	C_{ALERT}	0.5	1.5	0.5	1.5	0.5	1.5	pF	1, 3
Input/output capacitance: ZQ pin	C_{ZQ}	0.5	2.3	0.5	2.3	0.5	2.3	pF	1, 3, 12
Input/output capacitance: TEN pin	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	pF	1, 3, 13

Notes:
1. Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to a production test; it is verified by design and characterization. The capacitance is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). $V_{DD} = V_{DDQ} = 1.5V$, $V_{BIAS} = V_{DD}/2$ and on-die termination off.
3. This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.
4. $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS\_t) + C_{IO}(DQS\_c))$.
5. Absolute value of C_{IO} (DQS_t), C_{IO} (DQS_c)
6. Absolute value of CCK_t, CCK_c
7. C_I applies to ODT, CS_n, CKE, A[15:0], BA[1:0], RAS_n, CAS_n, and WE_n.
8. CD_{I_CTRL} applies to ODT, CS_n, and CKE.
9. $CD_{I\_CTRL} = C_I(CTRL) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$.
10. $C_{DI\_ADD\_CMD}$ applies to A[15:0], BA1:0], RAS_n, CAS_n and WE_n.
11. $C_{DI\_ADD\_CMD} = C_I(ADD\_CMD) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$.
12. Maximum external load capacitance on ZQ pin: 5pF.
13. Only applicable if TEN pin does not have an internal pull-up.

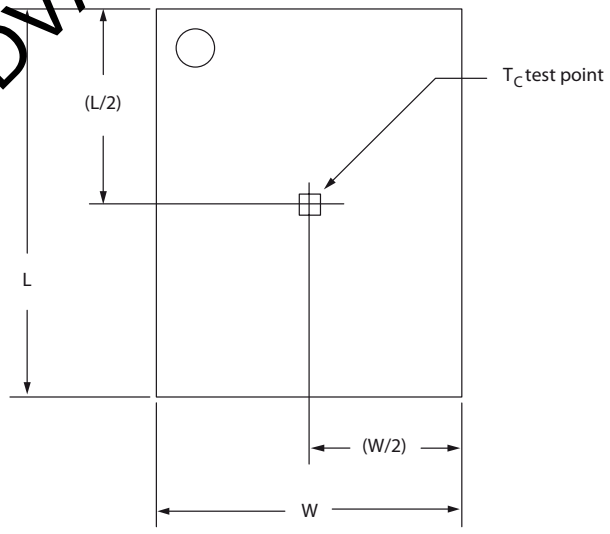
Thermal Characteristics

Table 59: Thermal Characteristics

Parameter/Condition		Value	Units	Symbol	Notes
Operating case temperature: Commercial		0 to 85	°C	T_C	1, 2, 3
		0 to 95	°C	T_C	1, 2, 3, 4
Operating case temperature: Industrial		–40 to 85	°C	T_C	1, 2, 3
		–40 to 95	°C	T_C	1, 2, 3, 4
Operating case temperature: Automotive		–40 to 85	°C	T_C	1, 2, 3
		–40 to 105	°C	T_C	1, 2, 3, 4
Junction-to-case (TOP) Die Rev A	78-ball "HX"	4.4	°C/W	ΘJC	5
	96-ball "HA"	3.6			
Junction-to-case (TOP) Die Rev B	78-ball "RH"	TBD	°C/W	ΘJC	5
	96-ball "GE"	TBD			

Notes:
1. MAX operating case temperature. T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate.
5. The thermal resistance data is based off of a number of samples from multiple lots and should be viewed as a typical number.

Figure 47: Thermal Measurement Point



Current Specifications – Measurement Conditions

I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

I_{DD}, I_{PP}, and I_{DDQ} measurement conditions, such as test load and patterns, are defined in this section.

- I_{DD} currents (I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD7}, and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the device under test grouped together. I_{PP} and I_{DDQ} currents are not included in I_{DD} currents.
- I_{PP} currents are I_{PPSB} for standby cases (I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD8}); I_{PP0} for active cases (I_{DD0},I_{DD1}, I_{DD4R}, I_{DD4W}); I_{PP5B} and I_{PP6N} for self refresh cases (I_{DD6N}, I_{DD6E}, I_{DD6R}), and I_{PP7}. These have the same definitions as the I_{DD} currents referenced but are measured on the V_{PP} supply.
- I_{DDQ} currents (I_{DDQ2NT} and I_{DDQ4R}) are measured as time-averaged currents with V_{DDQ} balls of the device under test grouped together. I_{DD} current is not included in I_{DDQ} currents.

Note: I_{DDQ} values cannot be directly used to calculate the I/O power of the device. They can be used to support correlation of simulated I/O power to actual I/O power. In DRAM module application, I_{DDQ} cannot be measured separately because V_{DD} and V_{DDQ} are using a merged-power layer in the module PCB.

The following definitions apply for I_{DD}, I_{DDP} and I_{DDQ} measurements.

- "0" and "LOW" are defined as $V_{IN} \leq V_{IL(AC)max}$
- "1" and "HIGH" are defined as $V_{IN} \leq V_{IH(AC)min}$
- "Midlevel" is defined as inputs $V_{REF} = V_{DD}/2$
- Timings used for I_{DD}, I_{DDP} and I_{DDQ} measurement-loop patterns are provided in the Current Test Definition and Patterns section.
- Basic I_{DD}, I_{PP}, and I_{DDQ} measurement conditions are described in the Current Test Definition and Patterns section.
- Detailed I_{DD}, I_{PP}, and I_{DDQ} measurement-loop patterns are described in the Current Test Definition and Patterns section.
- Current measurements are done after properly initializing the device. This includes, but is not limited to, setting:
  $R_{ON} = R_{ZQ}/7$ (34 ohm in MR1);
  Qoff = 0B (output buffer enabled in MR1);
  $R_{TT(NOM)} = R_{ZQ}/6$ (40 ohm in MR1);
  $R_{TT(WR)} = R_{ZQ}/2$ (120 ohm in MR2);
  $R_{TT(Park)}$ = disabled;
  TDQS feature disabled in MR1; CRC disabled in MR2; CA parity feature disabled in MR3; Gear-down mode disabled in MR3; Read/Write DBI disabled in MR5; DM disabled in MR5
- Define D = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D_n = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

Note: The measurement-loop patterns must be executed at least once before actual current measurements can be taken.

Figure 48: Measurement Setup and Test Load for I_{DDx}, I_{DDPx}, and I_{DDQx}

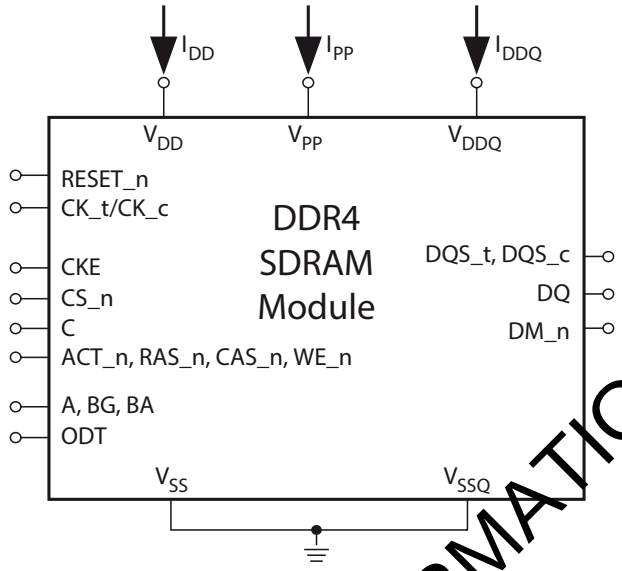
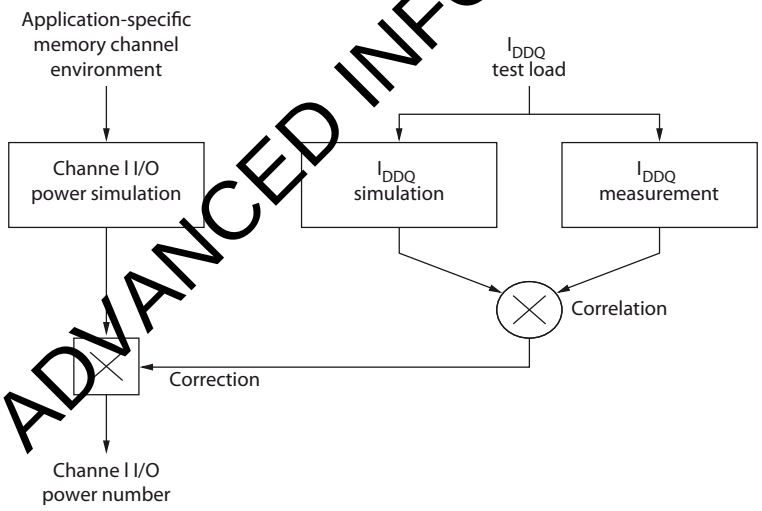


Figure 49: Correlation: Simulated Channel I/O Power to Actual Channel I/O Power



Note: 1. Supported by I_{DDQ} measurement.

I_{DD} Definitions

Table 60: Basic I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, *n*RC, *n*RAS, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: V_{DDQ}; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the I_{DD0} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD0} Measurement-Loop Pattern table

TABLE 60: BASIC I_{DD}, I_{PP}, AND I_{DDQ} MEASUREMENT CONDITIONS (CONTINUED)

Symbol	Description
I_{PP0}	**Operating One Bank Active-Precharge I_{PP} Current (AL = 0)** Same conditions as I_{DD0} above
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, CL: see the previous table; BL: 8;[1, 5] AL: 0; CS_n: HIGH between ACT, RD, and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the I_{DD1} Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Output buffer and R_{TT}: enabled in mode registers;[2] ODT Signal: stable at 0; Pattern details: see the I_{DD1} Measurement-Loop Pattern table
I_{DD2N}	**Precharge Standby Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{DD2NT}	**Precharge Standby ODT Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank gropup address, bank address inputs: partially toggling according to the I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern table; Data I/O: V_{SSQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: toggling according to the I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern table; Pattern details: see the I_{DD2NT} and I_{DDQ2NT} Measurement-Loop Pattern table
I_{DDQ2NT}	**Precharge Standby ODT I_{DDQ} Current** Has the same definition as I_{DD2NT} above, with the exception of measuring I_{DDQ} current instead of I_{DD} current
I_{DD2P}	**Precharge Power-Down Current** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{DD2Q}	**Precharge Quiet Standby Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0
I_{DD3N}	**Active Standby Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{PPSB}	**Active Standby I_{PPSB} Current (AL = 0)** Same conditions as I_{DD3N} above
I_{DD3P}	**Active Power-Down Current (AL = 0)** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0

TABLE 60: BASIC I_{DD}, I_{PP}, AND I_{DDQ} MEASUREMENT CONDITIONS (CONTINUED)

Symbol	Description
I_{DD4R}	**Operating Burst Read Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[15] AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table); Output buffer and R_{TT}: Enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table
I_{DDQ4R}	**Operating Burst Read I_{DDQ} Current** Has the same definition as I_{DD4R}, with the exception of measuring I_{DDQ} current instead of I_{DD} current
I_{DD4W}	**Operating Burst Write Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4W} Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the I_{DD4W} Measurement-Loop Pattern table; DM: stable at 0; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see I_{DD4W} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers (see note2); ODT signal: stable at HIGH; Pattern details: see the I_{DD4W} Measurement-Loop Pattern table
I_{DD5B}	**Burst Refresh Current (1X REF)** CKE: HIGH; External clock: on; ^{t}CK, CL, *n*RFC: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD5B} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: REF command every *n*RFC (see the I_{DD5B} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers[2]; ODT signal: stable at 0; Pattern details: see the I_{DD5B} Measurement-Loop Pattern table
I_{PP5B}	**Burst Refresh Current (1X REF)** Same conditions as I_{DD5B} above
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** T_C: 0–85°C; Auto self refresh (ASR): disabled;[3] Self refresh temperature range (SRT): normal;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{PP6N}	**Self Refresh I_{PP} Current: Normal Temperature Range** Same conditions as I_{DD6N} above
I_{DD6E}	**Self Refresh Current: Extended Temperature Range[4]** T_C: 0–95°C; Auto self refresh (ASR): disabled[4]; Self refresh temperature range (SRT): extended;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, group bank address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{DD6R}	**Self Refresh Current: Reduced Temperature Range** T_C: 0–45°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): reduced;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel

TABLE 60: BASIC I_{DD}, I_{PP}, AND I_{DDQ} MEASUREMENT CONDITIONS (CONTINUED)

Symbol	Description
I_{DD7}	**Operating Bank Interleave Read Current** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, *n*RRD, *n*FAW, CL: see the previous table; BL: 8; [15] AL: CL - 1; CS_n: HIGH between ACT and RDA; Command, address, group bank adress, bank address inputs: partially toggling according to the I_{DD7} Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the I_{DD7} Measurement-Loop Pattern table; DM: stable at 1; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the I_{DD7} Measurement-Loop Pattern table; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD7} Measurement-Loop Pattern table
I_{PP7}	**Operating Bank Interleave Read I_{pp} Current** Same conditions as I_{DD7} above
I_{DD8}	**Maximum Power Down Current** Place DRAM in MPSM then CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: Enabled in mode registers; [2]ODT signal: stable at 0

Notes:
1. Burst length: BL8 fixed by MRS: set MR0[1:0] 00.
2. Output buffer enable: set MR1[12] 0 (output buffer enabled); set MR1[2:1] 00 (R_{ON} = R_{ZQ}/7); $R_{TT(NOM)}$ enable: set MR1[10:8] 011 (RZQ/6); $R_{TT(WR)}$ enable: set MR2[11:9] 001 (R_{ZQ}/2), and $R_{TT(Park)}$ enable: set MR5[8:6] 000 (disabled).
3. Auto self refresh (ASR): set MR2[6] 0 to disable or MR2[6] 1 to enable feature.
4. Self refresh temperature range (SRT): set MR2[7] 0 for normal or MR2[7] 1 for extended temperature range.
5. READ burst type: Nibble sequential, set MR0[3] 0.

Current Specifications – Patterns and Test Conditions

Current Test Definitions and Patterns

TABLE 61: I_{DD0} AND I_{PP0} MEASUREMENT-LOOP PATTERN[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1, 2	D, D	1	1	1	1	1	0	0	0	0	0	0	0	0	0	–
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			*n*RAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary															
		1	1 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		2	2 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	5 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	6 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	7 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	8 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	9 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	10 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	11 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	12 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	13 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	14 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	15	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes:
1. DQS_t, DQS_c are V_{DDQ}.
2. BG1 is a "Don't Care" for x16 devices.
3. DQ signals are V_{DDQ}.
4. For x4 and x8 only.

TABLE 62: I_{DD1} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 1...4 until *n*RCD - AL - 1; truncate if necessary															
			*n*RCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			*n*RAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	
			...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary															
		1	1 × *n*RC + 0	ACT	0	0	0	1	1	0	1	0	0	0	0	0	0	0	–
			1 × *n*RC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1 × *n*RC + 3, 4	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern *n*RC + 1...4 until 1 × *n*RC + *n*RAS - 1; truncate if necessary															
			1 × *n*RC +*n*RCD - AL	RD	0	1	1	0	1	0	1	1	0	0	0	0	0	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00
			...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary															
			1 × *n*RC + *n*RAS	PRE	0	1	0	1	0	0	1	1	0	0	0	0	0	0	
			...	Repeat pattern *n*RC + 1...4 until 2 × *n*RC - 1; truncate if necessary															
		2	2 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	5 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	6 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	7 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	8 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	9 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	10 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	11 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	12 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	13 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	14 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	15 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.

TABLE 63: I_{DD2N}, I_{DD3N}, AND I_{PP3P} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. DQ signals are V_{DDQ}.

TABLE 64: I_{DD2NT} AND I_{DDQ2NT} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{SSQ}.
2. DQ signals are V_{SSQ}.

TABLE 65: I_{DD4R} AND I_{DDQ4R} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			2, 3	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
		1	4	RD	0	1	1	0	1	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6, 7	D_n, D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes:
1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. Burst sequence driven on each DQ signal by a READ command. Outside burst operation, DQ signals are V_{DDQ}.

TABLE 66: I_{DD4W} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Com-mand	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			2, 3	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		1	4	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			6, 7	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes: 1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.

TABLE 67: I_{DD4Wc} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][3]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D8 = CRC
			1, 2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			3, 4	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		1	5	WR	0	1	1	0	0	1	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00 D8 = CRC
			6, 7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
			8, 9	D_n, D_n	1	1	1	1	0	1	3	3	0	0	0	7	F	0	
		2	10–14	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	15–19	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	20–24	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	25–29	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	30–34	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	35–39	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	40–44	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
		9	45–49	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
		10	50–54	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
		11	55–59	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
		12	60–64	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
		13	65–69	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
		14	70–74	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
		15	75–79	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															

Notes:
1. Pattern provided for reference only.
2. DQS_t, DQS_c are V_{DDQ} when not toggling.
3. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.

TABLE 68: I_{DD5B} MEASUREMENT-LOOP PATTERN[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	–
		2	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			4	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			5–8	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 1 instead															
			9–12	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 2 instead															
			13–16	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 3 instead															
			17–20	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 1 instead															
			21–24	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 2 instead															
			25–28	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 3 instead															
			29–32	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 0 instead															
			33–36	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 0 instead[4]															
			37–40	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 1 instead[4]															
			41–44	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 2 instead[4]															
			45–48	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 3 instead[4]															
			49–52	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 1 instead[4]															
			53–56	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 2 instead[4]															
			57–60	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 3 instead[4]															
			61–64	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 0 instead[4]															
		2	65...*n*RFC - 1	Repeat sub-loop 1; truncate if necessary															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. DQ signals are V_{DDQ}.

TABLE 69: I_{DD7} MEASUREMENT-LOOP PATTERN[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			1	RDA	0	1	1	0	1	0	0	0	0	0	1	0	0	0	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	–
			3	D_n	1	1	1	1	1	0	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 2...3 until *n*RRD - 1, if *n*RRD > 4. Truncate if necessary															
		1	*n*RRD	ACT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	–
			*n*RRD+1	RDA	0	1	1	0	1	0	1	1	0	0	1	0	0	0	
			...	Repeat pattern 2...3 until 2 × *n*RRD - 1, if *n*RRD > 4. Truncate if necessary															
		2	2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	4 × *n*RRD	Repeat pattern 2...3 until *n*FAW - 1, if *n*FAW > 4 × *n*RRD. Truncate if necessary															
		5	*n*FAW	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		9	*n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		10	2 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead															
		11	2 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead															
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead															
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead															
		14	2 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		15	3 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead															
		16	3 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead															
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead															
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead															
		19	3 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4															
		20	4 × *n*FAW	Repeat pattern 2...3 until *n*RC - 1, if *n*RC > 4 × *n*FAW. Truncate if necessary															

Notes: 1. DQS_t, DQS_c are V_{DDQ}.
2. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.

I_{DD} Specifications

Table 70: Timings used for I_{DD}, I_{PP}, and I_{DDQ} Measurement-Loop Patterns

Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400			DDR4-2666			DDR4-3200			Unit
		10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	15-15-15	16-16-16	17-17-17	17-17-17	18-18-18	19-19-19	20-20-20	22-22-22	24-24-24	
tCK		1.25			1.071			0.937			0.833			0.75			0.625			ns
CL		10	11	12	12	13	14	14	15	16	15	16	17	17	18	19	20	22	24	CK
CWL		9	11	11	10	12	12	11	14	14	12	16	16	14	18	18	16	20	20	CK
*n*RCD		10	11	12	12	13	14	14	15	16	15	16	17	17	18	19	20	22	24	CK
*n*RC		38	39	40	44	45	46	50	51	52	54	55	57	60	61	62	72	74	76	CK
*n*RP		10	11	12	12	13	14	14	15	16	15	16	17	17	18	19	20	22	24	CK
*n*RAS		28			32			36			39			43			52			CK
*n*FAW	x4[1]	16			16			16			16			16			16			CK
	x8	20			22			23			26			28			34			CK
	x16	28			28			32			36			40			48			CK
*n*RRD_S	x4	4			4			4			4			4			4			CK
	x8	4			4			4			4			4			4			CK
	x16	5			5			6			7			7			9			CK
*n*RRD_L	x4	5			5			6			6			7			8			CK
	x8	5			5			6			6			7			8			CK
	x16	6			6			7			8			9			11			CK
*n*CCD_S		4			4			4			4			4			4			CK
*n*CCD_L		5			5			6			6			7			8			CK
*n*WTR_S		2			3			3			3			4			4			CK
*n*WTR_L		6			7			8			9			10			12			CK
*n*RFC 2Gb		128			150			171			193			214			256			CK
*n*RFC 4Gb		208			243			278			313			347			416			CK
*n*RFC 8Gb		280			327			374			421			467			560			CK
*n*RFC 16Gb		440			514			587			660			733			880			CK

Current Specifications – Limits

TABLE 71: I_{DD}, I_{PP}, AND I_{DDQ} CURRENT LIMITS

Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
I_{DD0}: One bank ACTIVATE-to-PRE-CHARGE current	264	264	272	280	mA mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	18.4	18.4	18.4	18.4	mA mA
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	312	312	320	326	mA mA
I_{DD2N}: Precharge standby current	176	176	184	200	mA
I_{DD2NT}: Precharge standby ODT current	240	240	256	276	mA mA
I_{DD2P}: Precharge power-down current	120	120	120	128	mA
I_{DD2Q}: Precharge quiet standby current	156	156	156	164	mA
I_{DD3N}: Active standby current	244	244	252	268	mA
I_{PP3N}: Active standby I_{PP} current	12	12	12	12	mA
I_{DD3P}: Active power-down current	176	176	176	176	mA
I_{DD4R}: Burst read current	800	800	860	920	mA mA
I_{DD4W}: Burst write current	984	984	1104	1256	mA mA
I_{DD5B}: Burst refresh current (1X REF)	760	760	760	768	mA mA
I_{PP5B}: Burst refresh I_{PP} current (1X REF)	88	88	88	88	mA mA
I_{DD6N}: Self refresh current; 0–85°C[1]	80	80	80	80	mA
I_{DD6E}: Self refresh current; 0–95°C[2]	108	108	108	108	mA
I_{DD6R}: Self refresh current; 0–45C[3, 4]	40	40	40	40	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	36	36	36	36	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	40	40	40	40	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	64	64	64	64	mA
I_{DD7}: Bank interleave read current	920	920	960	1000	mA mA
I_{PP7}: Bank interleave read I_{PP} current	48	48	56	64	mA mA
I_{DD8}: Maximum power-down current	72	72	72	72	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A7 = 0; manual mode with extended temperature range of operation (0–95°C).

3. Applicable for MR2 settings A7 = 0 and A7 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. IDD6R and IDD6A values are typical.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1} , current changes by approximately +4%.
7. When additive latency is enabled for I_{DD2N} , current changes by approximately +0.6%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately 0%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –44%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +14%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +0.6%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When read DBI is enabled for I_{DDQ4R}, current changes by approximately –35%.
16. When additive latency is enabled for I_{DD4W}, current changes by approximately +1%.
17. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
18. When write CRC is enabled for I_{DD4W}, current changes by approximately –8% (2133/2400), –5% (1600/1866).
19. When CA parity is enabled for I_{DD4W}, current changes by approximately +8%.
20. When 2X REF is enabled for I_{DD5B}, current changes by approximately –14%.
21. When 4X REF is enabled for I_{DD5B}, current changes by approximately –33%.
22. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
23. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6}, and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.

TABLE 72: I_{DD}, I_{PP}, AND I_{DDQ} CURRENT LIMITS DDR4-2666 THROUGH DDR4-3200

Symbol	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	240	260	260	280	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	14.4	14.4	14.4	14.4	mA
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	280	300	300	320	mA
I_{DD2N}: Precharge standby current	160	168	180	200	mA
I_{DD2NT}: Precharge standby ODT current	220	240	240	280	mA
I_{DD2P}: Precharge power-down current	108	108	116	136	mA
I_{DD2Q}: Precharge quiet standby current	140	140	148	160	mA
I_{DD3N}: Active standby current	220	220	240	260	mA
I_{PP3N}: Active standby I_{PP} current	12	12	12	12	mA
I_{DD3P}: Active power-down current	160	160	160	160	mA

TABLE 72: I_{DD}, I_{PP}, AND I_{DDQ} CURRENT LIMITS (CONTINUED)

Symbol	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Unit
I_{DD4R}: Burst read current	720	780	820	900	mA
I_{DD4W}: Burst write current	880	1000	1140	1240	mA
I_{DD5B}: Burst refresh current (1X REF)	680	680	700	700	mA
I_{PP5B}: Burst refresh IPP_{PP}current (1X REF)	100	100	100	100	mA
I_{DD6N}: Self refresh current; 0–85°C [1]	72	72	72	72	mA
I_{DD6E}: Self refresh current; 0–95°C [2]	96	96	96	96	mA
I_{DD6R}: Self refresh current; 0–45C [3, 4]	48	48	48	48	mA
I_{DD6A}: Auto self refresh current (25°C) [4]	36	36	36	36	mA
I_{DD6A}: Auto self refresh current (45°C) [4]	48	48	48	48	mA
I_{DD6A}: Auto self refresh current (75°C) [4]	72	72	72	72	mA
I_{DD7}: Bank interleave read current	820	860	900	940	mA
I_{PP7}: Bank interleave read I_{PP} current	48	56	64	64	mA
I_{DD8}: Maximum power-down current	52	64	64	64	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A7 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A7 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. IDD6R and IDD6A values are typical.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for $_{IDD1}$, current changes by approximately +4%.
7. When additive latency is enabled for I_{DD2N} , current changes by approximately +0.6%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately 0%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –44%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +14%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +0.6%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When read DBI is enabled for I_{DD4R}, current changes by approximately 0%.
15. When read DBI is enabled for I_{DDQ4R}, current changes by approximately – 35%.
16. When additive latency is enabled for I_{DD4W}, current changes by approximately +1% (x16).

17. When write DBI is enabled for I_{DD4W}, current changes by approximately 0%.
18. When write CRC is enabled for I_{DD4W}, current changes by approximately –8% (2133/2400), –5% (1600/1866).
19. When CA parity is enabled for I_{DD4W}, current changes by approximately +8%
20. When 2X REF is enabled for I_{DD5B}, current changes by approximately –14%.
21. When 4X REF is enabled for I_{DD5B}, current changes by approximately –33%.
22. IPP0 test and limit is applicable for I_{DD0} and I_{DD1} conditions.
23. IPP3N test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6}, and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.

Speed Bin Tables

TABLE 73: DDR4-1600 SPEED BINS AND OPERATING CONDITIONS

DDR4-1600 Speed Bin					-125		
CL-*n*RCD-*n*RP					12-12-12		
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		15.00	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		–	^{t}AA (MAX) + 2*n*CK	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		15.00	–	ns
PRECHARGE command period			^{t}RP		15.00	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		35	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: non-DBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
Supported CL settings					10, 12		*n*CK
Supported CL settings with read DBI					12, 14		*n*CK
Supported CWL settings					9, 11		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. The DRAM supports 13.5ns with CL9 operation at defined clock rates.

Table 74: DDR4-1866 Speed Bins and Operating Conditions

DDR4-1866 Speed Bin					-107		
CL-*n*RCD-*n*RP					14-14-14		
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		15.00	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA (MIN) + 2*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		15.00	–	ns
PRECHARGE command period			^{t}RP		15.00	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		34	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[6]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[6]		1.5	1.6	ns
CL = 10	CL = 12	CWL = 11	^{t}CK[6]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[6]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[6]		1.25	<1.5	ns
CL = 12	CL = 14	CWL = 10, 12	^{t}CK[6]		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[6]		Reserved		ns
CL = 14	CL = 16	CWL = 10, 12	^{t}CK[6]		1.071	<1.25	ns
Supported CL settings					10, 12, 14		*n*CK
Supported CL settings with read DBI					12, 14, 16		*n*CK
Supported CWL settings					9–12		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. 12.85ns is the minimum value of ^{t}AA and tRP when operating at DDR4-1866 at ^{t}CK(AVG) MIN = 1.071ns and is only a reference that does not consider the down binning strategy that 12.5ns supports.
5. 13.92ns is the minimum value of ^{t}AA and ^{t}RP when operating at DDR4-1866 at ^{t}CK(AVG) MIN = 1.071ns and is only a reference that does not consider the down binning strategy that 13.75ns supports.
6. ^{t}CK(AVG) MIN.
7. The DRAM supports 13.5ns with CL9 operation and 13.75ns with CL11 operation at defined clock rates.

Table 75: DDR4-2133 Speed Bins and Operating Conditions

DDR4-2133 Speed Bin					-093		
CL-*n*RCD-*n*RP					16-16-16		
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		15.00	18	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA(MIN) + 3*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		15.00	–	ns
PRECHARGE command period			^{t}RP		15.00	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		33	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]		1.5	1.6	
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 14	CL = 16	CWL = 10, 12	^{t}CK[4]		1.071	<1.25	ns
CL = 14	CL = 17	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 16	CL = 19	CWL = 11, 14	^{t}CK[4]		0.937	<1.071	ns
Supported CL settings					10, 12, 14, 16		*n*CK
Supported CL settings with read DBI					12, 14, 16, 19		*n*CK
Supported CWL settings					9, 10, 11, 12, 14		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. The DRAM supports 13.5ns with CL9 operation and 13.75ns with CL11 operation 13.92ns with CL13 operation at defined clock rates.
6. If the clock period is less than 0.938ns and greater than or equal to 0.937ns, timing parameters that are derived off the clock will use 0.938ns as its reference. For example, if ^{t}CK (MIN) = 0.938ns and ^{t}RP = 14.06ns, then ^{t}RP would require 15*n*CKs (14.06ns/ 0.938ns), but if ^{t}CK (MIN) = 0.937ns and ^{t}RP = 14.06ns, then ^{t}RP would still require 15*n*CKs (14.06ns/ 0.938ns) and not 16nCKs (14.06ns/ 0.937ns).

Table 76: DDR4-2400 Speed Bins and Operating Conditions

DDR4-2400 Speed Bin					-083		
CL-*n*RCD-*n*RP							
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		14.16	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA(MIN) + 3*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		14.16	–	ns
PRECHARGE command period			^{t}RP		14.16	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
CL = 12	CL = 14	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[4]		1.071	<1.25	ns
CL = 14	CL = 16	CWL = 10, 12	^{t}CK[4]		1.071	<1.25	ns
CL = 14	CL = 17	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	^{t}CK[4]		0.937	<1.071	ns
CL = 16	CL = 19	CWL = 11, 14	^{t}CK[4]		0.937	<1.071	ns
CL = 15	CL = 18	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 16	CL = 19	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 17	CL = 20	CWL = 12, 16	^{t}CK[4]		0.833	<0.937	ns
CL = 18	CL = 21	CWL = 12, 16	^{t}CK[4]		0.833	<0.937	ns
Supported CL Settings					10–18		*n*CK
Supported CL settings with read DBI					12–16, 18–21		*n*CK
Supported CWL settings					9, 10, 11, 12, 14, 16		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. If the clock period is less than 0.938ns and greater than or equal to 0.937ns, timing parameters that are derived off the clock will use 0.938ns as its reference. For example, if

^{t}CK (MIN) = 0.938ns and ^{t}RP = 14.06ns, then ^{t}RP would require 15*n*CKs (14.06ns/ 0.938ns), but if ^{t}CK (MIN) = 0.937ns and ^{t}RP = 14.06ns, then ^{t}RP would still require 15*n*CKs (14.06ns/ 0.938ns) and not 16*n*CKs (14.06ns/ 0.937ns).

TABLE 77: DDR4-2666 SPEED BINS AND OPERATING CONDITIONS

DDR4-2666 Speed Bin					**-075**		
CL-*n*RCD-*n*RP					**19-19-19**		
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		14.25[5]	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA(MIN) + 3*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		14.16	–	ns
PRECHARGE command period			^{t}RP		14.16	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]				ns
CL = 10	CL = 12	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]				ns
CL = 12	CL = 14	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[4]				ns
CL = 14	CL = 16	CWL = 10, 12	^{t}CK[4]				ns
CL = 14	CL = 17	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	^{t}CK[4]				ns
CL = 16	CL = 19	CWL = 11, 14	^{t}CK[4]				ns
CL = 15	CL = 18	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 16	CL = 19	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 17	CL = 20	CWL = 12, 16	^{t}CK[4]				ns
CL = 18	CL = 21	CWL = 12, 16	^{t}CK[4]				ns
CL = 17	CL = 20	CWL = 14, 18	^{t}CK[4]		Reserved		ns
CL = 18	CL = 21	CWL = 14, 18	^{t}CK[4]		Reserved		ns
CL = 19	CL = 22	CWL = 14, 18	^{t}CK[4]				ns
CL = 20	CL = 23	CWL = 14, 18	^{t}CK[4]				ns
Supported CL settings					10, 12-–20		*n*CK
Supported CL settings with read DBI					12, 14-–16, 18-–23		*n*CK

Table 77: DDR4-2666 Speed Bins and Operating Conditions (Continued)

DDR4-2666 Speed Bin			-075		
CL-*n*RCD-*n*RP			19-19-19		
Parameter	**Symbol**		**Min**	**Max**	**Unit**
Supported CWL settings			9, 10, 11, 12, 14, 16, 18		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. The DRAM supports 13.92ns with CL13 operation, 14.07ns with CL15 operation, and 14.16ns with CL17 operation at defined clock rates.
6. If the clock period is less than 0.938ns and greater than or equal to 0.937ns, timing parameters that are derived off the clock will use 0.938ns as its reference. For example, if ^{t}CK (MIN) = 0.938ns and ^{t}RP = 14.06ns, then ^{t}RP would require 15*n*CKs (14.06ns/ 0.938ns), but if ^{t}CK (MIN) = 0.937ns and ^{t}RP = 14.06ns, then ^{t}RP would still require 15*n*CKs (14.06ns/ 0.938ns) and not 16*n*CKs (14.06ns/ 0.937ns).

Table 78 DDR4-2933 Speed Bins and Operating Conditions

DDR4-2933 Speed Bin					-068D		
CL-*n*RCD-*n*RP					22-22-22		
Parameter			**Symbol**		**Min**	**Max**	**Unit**
Internal READ command to first data			^{t}AA		15	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA(MIN) + 4*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		15	–	ns
PRECHARGE command period			^{t}RP		15	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		32	9 x ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
CL = 12	CL = 14	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[4]		Reserved		ns

TABLE 78: DDR4-2933 SPEED BINS AND OPERATING CONDITIONS (CONTINUED)

DDR4-2933 Speed Bin				-068D		
CL-*n*RCD-*n*RP				22-22-22		
Parameter			**Symbol**	**Min**	**Max**	**Unit**
CL = 14	CL = 16	CWL = 10, 12	$^{t}CK^{4}$	1.071	<1.25	ns
CL = 14	CL = 17	CWL = 11, 14	$^{t}CK^{4}$	Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	$^{t}CK^{4}$	Reserved		ns
CL = 16	CL = 19	CWL = 11, 14	$^{t}CK^{4}$	0.937	<1.071	ns
CL = 15	CL = 18	CWL = 12, 16	$^{t}CK^{4}$	Reserved		ns
CL = 16	CL = 19	CWL = 12, 16	$^{t}CK^{4}$	Reserved		ns
CL = 17	CL = 20	CWL = 12, 16	$^{t}CK^{4}$	Reserved		ns
CL = 18	CL = 21	CWL = 12, 16	$^{t}CK^{4}$	0.833	<0.937	ns
CL = 17	CL = 20	CWL = 14, 18	$^{t}CK^{4}$	Reserved		ns
CL = 18	CL = 21	CWL = 14, 18	$^{t}CK^{4}$	Reserved		ns
CL = 19	CL = 22	CWL = 14, 18	$^{t}CK^{4}$	0.750	<0.833	ns
CL = 20	CL = 23	CWL = 14, 18	$^{t}CK^{4}$	0.750	<0.833	ns
CL = 19	CL = 23	CWL = 16, 20	$^{t}CK^{4}$	Reserved		ns
CL = 20	CL = 24	CWL = 16, 20	$^{t}CK^{4}$	Reserved		ns
CL = 21	CL = 26	CWL = 16, 20	$^{t}CK^{4}$	Reserved		ns
CL = 22	CL = 26	CWL = 16, 20	$^{t}CK^{4}$	0.682	<0.750	ns
Supported CL settings				10, 12, 14, 16, 18, 20		*n*CK
Supported CL settings with read DBI				12, 14, 16, 19, 21 23, 26		*n*CK
Supported CWL settings				9, 10, 11, 12, 14, 15, 16, 18, 20		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. The DRAM supports 13.5ns with CL9 operation.
6. If the clock period is less than 0.938ns and greater than or equal to 0.937ns, timing parameters that are derived off the clock will use 0.938ns as its reference. For example, if ^{t}CK (MIN) = 0.938ns and ^{t}RP = 14.06ns, then tRP would require 15*n*CKs (14.06ns/ 0.938ns), but if ^{t}CK (MIN) = 0.937ns and ^{t}RP = 14.06ns, then ^{t}RP would still require 15*n*CKs (14.06ns/ 0.938ns) and not 16*n*CKs (14.06ns/ 0.937ns).

Table 79: DDR4-3200 Speed Bins and Operating Conditions

DDR4-3200 Speed Bin					-062		
CL-*n*RCD-*n*RP					24-24-24		
Parameter			Symbol		Min	Max	Unit
Internal READ command to first data			^{t}AA		15	18.00	ns
Internal READ command to first data with read DBI enabled			^{t}AA_DBI		^{t}AA(MIN) + 4*n*CK	–	ns
ACTIVATE to internal READ or WRITE delay time			^{t}RCD		15	–	ns
PRECHARGE command period			^{t}RP		15	–	ns
ACTIVATE-to-PRECHARGE command period			^{t}RAS		32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period			^{t}RC		^{t}RAS + ^{t}RP	–	ns
READ: nonDBI	**READ: DBI**	**WRITE**	**Symbol**		**Min**	**Max**	**Unit**
CL = 9	CL = 11	CWL = 9	^{t}CK[4]		Reserved		ns
CL = 10	CL = 12	CWL = 9	^{t}CK[4]		1.5	1.6	ns
CL = 10	CL = 12	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 11	CL = 13	CWL = 9, 11	^{t}CK[4]		Reserved		ns
CL = 12	CL = 14	CWL = 9, 11	^{t}CK[4]		1.25	<1.5	ns
CL = 12	CL = 14	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 13	CL = 15	CWL = 10, 12	^{t}CK[4]		Reserved		ns
CL = 14	CL = 16	CWL = 10, 12	^{t}CK[4]		1.071	<1.25	ns
CL = 14	CL = 17	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 15	CL = 18	CWL = 11, 14	^{t}CK[4]		Reserved		ns
CL = 16	CL = 19	CWL = 11, 14	^{t}CK[4]		0.937	<1.071	ns
CL = 15	CL = 18	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 16	CL = 19	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 17	CL = 20	CWL = 12, 16	^{t}CK[4]		Reserved		ns
CL = 18	CL = 21	CWL = 12, 16	^{t}CK[4]		0.833	<0.937	ns
CL = 17	CL = 20	CWL = 14, 18	^{t}CK[4]		Reserved		ns
CL = 18	CL = 21	CWL = 14, 18	^{t}CK[4]		Reserved		ns
CL = 19	CL = 22	CWL = 14, 18	^{t}CK[4]		0.750	<0.833	ns
CL = 20	CL = 23	CWL = 14, 18	^{t}CK[4]		0.750	<0.833	ns
CL = 20	CL = 24	CWL = 16, 20	^{t}CK[4]		Reserved		ns
CL = 22	CL = 26	CWL = 16, 20	^{t}CK[4]		Reserved		ns
CL = 24	CL = 28	CWL = 16, 20	^{t}CK[4]		0.625	<0.750	ns
Supported CL settings					9–20, 22, 24		*n*Ck
Supported CL settings with read DBI					12, 14, 16, 19, 21, 23, 28		*n*Ck

Table 79: DDR4-3200 Speed Bins and Operating Conditions (Continued)				
DDR4-3200 Speed Bin		**-062**		
CL-*n*RCD-*n*RP		**24-24-24**		
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Supported CWL settings		9, 10, 11, 12, 14, 16, 18, 20		*n*CK

Notes:
1. Speed Bin table is only valid with DLL enabled and gear-down mode disabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to programmed value of CL.
4. ^{t}CK(AVG) MIN.
5. The DRAM supports 13.5ns with CL9 operation.
6. If the clock period is less than 0.938ns and greater than or equal to 0.937ns, timing parameters that are derived off the clock will use 0.938ns as its reference. For example, if ^{t}CK (MIN) = 0.938ns and ^{t}RP = 14.06ns, then ^{t}RP would require 15*n*CKs (14.06ns/ 0.938ns), but if ^{t}CK (MIN) = 0.937ns and ^{t}RP = 14.06ns, then ^{t}RP would still require 15*n*CKs (14.06ns/ 0.938ns) and not 16*n*CKs (14.06ns/ 0.937ns).

Refresh Parameters By Device Density

TABLE 80: REFRESH PARAMETERS

Parameter	Symbol			Unit	Notes
REF command to ACT or REF command time	^{t}RFC (All bank groups)		350	ns	
Average periodic refresh interval	^{t}REFI	0°C ≤ T_C ≤ 85°C	7.8	µs	
		0°C < T_C ≤ 95°C	3.9	µs	

Electrical Characteristics and AC Timing Parameters

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Clock Timing												
Clock period average (DLL off mode)		^{t}CK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Clock period average		^{t}CK (AVG, DLL_ON)	1.25	1.6	1.071	1.6	0.937	1.6	0.833	1.6	ns	14
High pulse width average		^{t}CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	CK	
Low pulse width average		^{t}CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	Ck	
Clock period jitter	Total	^{t}JITper_tot	–63	63	–54	54	–47	47	–42	42	ps	
	Deterministic	^{t}JITper_dj	–31	31	–27	27	–23	23	–21	21	ps	
	DLL locking	^{t}JITper_lck	–50	50	–43	43	–38	38	–33	33	ps	
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper_tot MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper_tot MAX								ps	
Clock absolute high pulse width (includes duty cycle jitter)		^{t}CH (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Clock absolute low pulse width (includes duty cycle jitter)		^{t}CL (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Cycle-to-cycle jitter	Total	^{t}JITcc _tot	125		107		94		83		ps	
	Deterministic	^{t}JITcc _dj	63		54		47		42		ps	
	DLL locking	^{t}JITcc,lck	100		86		75		67		ps	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across	2 cycles	^{t}ERR2per	–92	92	–79	79	–69	69	–61	61	ps	
	3 cycles	^{t}ERR3per	–109	109	–94	94	–82	82	–73	73	ps	
	4 cycles	^{t}ERR4per	–121	121	–104	104	–91	91	–81	81	ps	
	5 cycles	^{t}ERR5per	–131	131	–112	112	–98	98	–87	87	ps	
	6 cycles	^{t}ERR6per	–139	139	–119	119	–104	104	–92	92	ps	
	7 cycles	^{t}ERR7per	–145	145	–124	124	–109	109	–97	97	ps	
	8 cycles	^{t}ERR8per	–151	151	–129	129	–113	113	–101	101	ps	
	9 cycles	^{t}ERR9per	–156	156	–134	134	–120	120	–104	104	ps	
	10 cycles	^{t}ERR10per	–160	160	–137	137	–123	123	–107	107	ps	
	11 cycles	^{t}ERR11per	–164	164	–141	141	–126	126	–110	110	ps	
	12 cycles	^{t}ERR12per	–168	168	–144	144	–129	129	–112	112	ps	
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper MAX								ps	
DQ Input Timing												
Data setup time to DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DS	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Noncalibrated V_{REF}	^{t}PDA_S	minimum of 0.5IU								IU	
Data hold time from DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DH	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)								–	
	Noncalibrated V_{REF}	^{t}PDA_H	minimum of 0.5IU								IU	
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	–	0.58	–	0.58	–	0.58	–	IU	
DQ Output Timing (DLL enabled)												
DQS_t, DQS_c to DQ skew, per group, per access		^{t}DQSQ	–	0.16	–	0.16	–	0.16	–	0.17	IU	
DQ output hold time from DQS_t, DQS_c		^{t}QH	0.76	–	0.76	–	0.76	–	0.76	–	IU	
Data Valid Window per device: ^{t}QH - ^{t}DQSQ each device's output per UI		^{t}DVW$_d$	0.63		0.63		0.64		0.64		IU	
Data Valid Window per device, per pin: ^{t}QH - ^{t}DQSQ each device's output per UI		^{t}DVW$_p$	0.66	–	0.66	–	0.69	–	0.72	–	IU	

Table 81: Electrical Characteristics and AC Timing Parameters: DDR4-1600 through DDR4-2400 (Continued)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQ Low-Z time from CK_t, CK_c	tLZDQ	–450	225	–390	195	–360	180	–360	150	ps	
DQ High-Z time from CK_t, CK_c	tHZDQ	–	225	–	195	–	180	–	150	ps	
DQ Strobe Input Timing											
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge	tDQSS	–0.27	0.27	–0.27	0.27	–0.27	0.27	–0.27	0.27	CK	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge	tDSS	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge	tDSH	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c differential WRITE preamble	tWPRE	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential WRITE postamble	tWPST	0.33	–	0.33	–	0.33	–	0.33	–	CK	
DQS Strobe Output Timing (DLL enabled)											
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	tDQSCK	–225	225	–195	195	–180	180	–175	175	ps	
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKi	–	370	–	330	–	310	–	290	ps	
DQS_t, DQS_c differential output high time	tQSH	0.38	–	0.38	–	0.38	–	0.38	–	CK	
DQS_t, DQS_c differential output low time	tQSL	0.38	–	0.38	–	0.38	–	0.38	–	CK	
DQS_t, DQS_c Low-Z time (RL - 1)	tLZDQS	–450	225	–390	195	–360	180	–300	150	ps	
DQS_t, DQS_c High-Z time (RL + BL/2)	tHZDQS	–	225	–	195	–	180	180	150	ps	
DQS_t, DQS_c differential READ preamble	tRPRE	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential READ postamble	tRPST	0.33	–	0.33	–	0.33	–	0.33	–	CK	
Command and Address Timing											

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
DLL locking time		^{t}DLLK	597	–	597	–	768	–	768	–	CK	2, 4
CMD, ADDR setup time to CK_t, CK_c Base referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^{t}IS	115	–	100	–	80	–	62	–	ps	
	V_{REFCA}	$^{t}IS_{VREF}$	215	–	200	–	180	–	162	–	ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^{t}IH	140	–	125	–	105	–	87	–	ps	
	V_{REFCA}	$^{t}IH_{VREF}$	215	–	200	–	180	–	162	–	ps	
CTRL, ADDR pulse width for each input		^{t}IPW	600	–	525	–	460	–	410	–	ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD								ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP								ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS								ns	13
ACTIVATE-to-ACTIVATE or REF command period		^{t}RC	See Speed Bin Tables for ^{t}RC								ns	13
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size		^{t}RRD_S (1/2KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size		^{t}RRD_S (1KB)	MIN = greater of 4CK or 5ns		MIN = greater of 4CK or 4.2ns		MIN = greater of 4CK or 3.7ns		MIN = greater of 4CK or 3.3ns		CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size		^{t}RRD_S (2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size		^{t}RRD_L (1/2KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size		^{t}RRD_L (1KB)	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 4.9ns		CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size		^{t}RRD_L (2KB)	MIN = greater of 4CK or 7.5ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		CK	1
Four ACTIVATE windows for 1/2KB page size		^{t}FAW (1/2KB)	MIN = greater of 16CK or 20ns		MIN = greater of 16CK or 17ns		MIN = greater of 16CK or 15ns		MIN = greater of 16CK or 13ns		ns	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter	Symbol	DDR4 -1600		DDR4 - 1866		DDR4 - 2133		DDR4 - 2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN = greater of 20CK or 25ns		MIN = greater of 20CK or 23ns		MIN = greater of 20CK or 21ns		MIN = greater of 20CK or 21ns		ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN = greater of 28CK or 35ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		ns	
WRITE recovery time	^{t}WR	MIN = 15ns								ns	6, 10, 1
	^{t}WR$_2$	MIN = 1CK + ^{t}WR								CK	6, 11, 1
WRITE recovery time when CRC and DM are both enabled	^{t}WR_CRC_DM	MIN = ^{t}WR_L + greater of (4CK or 3.75ns)		MIN = ^{t}WR_L + greater of (5CK or 3.75ns)						CK	7, 10, 1
	^{t}WR_CRC_DM$_2$	MIN = 1CK + ^{t}WR_CRC_DM								CK	7, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group	^{t}WTR_L	MIN = greater of 4CK or 7.5ns								CK	6, 10, 1
	^{t}WTR_L$_2$	MIN = 1CK + ^{t}WTR_L								CK	6, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	^{t}WTR_L_CRC_DM	MIN = ^{t}WR_S + greater of (4CK or 3.75ns)		MIN = ^{t}WR_S + greater of (5CK or 3.75ns)						CK	7, 10, 1
	^{t}WTR_L_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_L_CRC_DM								CK	7, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group	^{t}WTR_S	MIN = greater of (2CK or 2.5ns)								CK	6, 8, 9, 10, 1
	^{t}WTR_S$_2$	MIN = 1CK + ^{t}WTR_S								CK	6, 8, 9, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	^{t}WTR_S_CRC_DM	MIN = ^{t}WR + greater of (4CK or 3.75ns)		MIN = ^{t}WR + greater of (5CK or 3.75ns)						CK	7, 8, 9, 10, 1
	^{t}WTR_S_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_S_CRC_DM								CK	7, 8, 9, 11, 1
READ-to-PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns								CK	1
CAS_n-to-CAS_n command delay to different bank group	^{t}CCD_S	4	–	4	–	4	–	4	–	CK	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter	Symbol	DDR4 -1600		DDR4 -1866		DDR4 -2133		DDR4 -2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS_n-to-CAS_n command delay to same bank group	tCCD_L	MIN = greater of 4CK or 6.25ns	–	MIN = greater of 4CK or 5.355ns	–	MIN = greater of 4CK or 5.355ns	–	MIN = greater of 4CK or 5ns	–	CK	15
Auto precharge write recovery + precharge time	tDAL (MIN)	MIN = WR + ROUNDUP tRP/tCK (AVG); MAX = N/A								CK	
MRS Command Timing											
MRS command cycle time	tMRD	8	–	8	–	8	–	8	–	CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16CK, 10ns)								CK	1
MRS command cycle time in CAL mode	tMOD	MIN = tMOD + tCAL								CK	
MRS command update delay in PDA mode	tMOD	MIN = greater of (24nCK, 15ns)								CK	1
MRS command update delay	tMOD_PDA	MIN = tMOD								CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL								CK	
MRS commandto DQS drive in preamble training	tSDO	MIN = tMOD + 9ns									
MPR Command Timing											
Multipurpose register recovery time	tMPRR	MIN = 1CK								CK	
Multipurpose register write recovery time	tWR_MPRR	MIN = tMOD + AL + PL									
CRC Error Reporting Timing											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10	6	10	CK	
CA Parity Timing											
Parity latency	PL	4	–	4	–	4	–	5	–	CK	
Commands uncertain to be executed during this time	tPAR_UNKNOWN	–	PL	–	PL	–	PL	–	PL	CK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	–	PL + 6ns	–	PL + 6ns	–	PL + 6ns	–	PL + 6ns	CK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	128	CK	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter		Symbol	DDR4 -1600		DDR4 -1866		DDR4 - 2133		DDR4 - 2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Time from alert asserted until DES commands required in persistent CA parity mode		tPAR_ALERT_RSP	–	43	–	50	–	57	–	64	CK	
CAL Timing												
CS_n to command address latency		tCAL	3	–	4	–	4	–	5	–	CK	
CS_n to command address latency in gear-down mode		tCALg	N/A	–	N/A	–	N/A	–	N/A	–	CK	
MPSM Timing												
Command path disable delay upopn MPSM entry		tMPED	MIN = tMOD (MIN) + tCPDED (MIN)								CK	1
Valid clock requirement after MPSM entry		tCKMPE	MIN = tMOD (MIN) + tCPDED (MIN)								CK	1
Valid clock requirement before MPSM exit		tCKMPX	MIN = tCKSRX (MIN)								CK	1
Exit MPSM to commands not requiring a locked DLL		tXMP	tXS (MIN)								CK	
Exit MPSM to commands requiring a locked DLL		tXMPDLL	MIN = tXMP (MIN) + tXSDLL (MIN) CK 1								CK	1
CS setup time to CKE		tMPX_S	MIN = tIS (MIN) + tIH (MIN)								ns	
CS_n HIGH hold time to CKE rising edge		tMPX_HH	MIN = tXP								ns	
CS_n LOW hold time to CKE rising edge		tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	ns	
Connectivity Test Timing												
TEN pin HIGH to CS_n LOW – Enter CT mode		tCT_Enable	200	–	200	–	200	–	200	–	ns	
CS_n LOW and valid input to valid output		tCT_Valid	–	200	–	200	–	200	–	200	ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		tCKECT_Valid	10	–	10	–	10	–	10	–	ns	
Calibration and V_{REFDQ} Train Timing												
ZQCL command: Long calibration time	POWER-UP and RESET operation	tZQinit	1024	–	1024	–	1024	–	1024	–	CK	
	Normal operation	tZQoper	512	–	512	–	512	–	512	–	CK	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter		Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
ZQCS command: Short calibration time		tZQCS	128	–	128	–	128	–	128	–	CK	
The V_{REF} increment/decrement step time		V_{REF_time}	MIN = 150ns									
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		tVREFDQE	MIN = 150ns								ns	1
Exit V_{REFDQ} training mode to the first WRITE command delay		tVREFDQX	MIN = 150ns								ns	1
Initialization and Reset Timing												
Exit reset from CKE HIGH to a valid command		tXPR	MIN = greater of 5CK or tRFC (MIN) + 10ns								CK	1
RESET_L pulse low after power stable		tPW_REST_S	0.1	–	0.1	–	0.1	–	0.1	–	µs	
RESET_L pulse low at power-up		tPW_REST_L	200	–	200	–	200	–	200	–	µs	
Begin power supply ramp to power supplies stable		tVDDPR	MIN = N/A; MAX = 200								ms	
RESET_n LOW to power supplies stable		tRPS	MIN = 0; MAX = 0								ns	
RESET_n LOW to I/O and R_{TT} High-Z		tIOZ	MIN = N/A; MAX = undefined								ns	
Refresh Timing												
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	tRFC1	MIN = 260								ns	1, 12
		tRFC2	MIN = 160								ns	1, 12
		tRFC4	MIN = 110								ns	1, 12
	8Gb	tRFC1	MIN = 350								ns	1, 12
		tRFC2	MIN = 260								ns	1, 12
		tRFC4	MIN = 160								ns	1, 12
	16Gb	tRFC1	MIN = 550								ns	1, 12
		tRFC2	MIN = 405								ns	1, 12
		tRFC4	MIN = 250								ns	1, 12
Average periodic refresh interval	0°C ≤ T_C ≤ 85°C	tREFI	MIN = N/A; MAX = 7.8								µs	12
	85°C < T_C ≤ 95°C	tREFI	MIN = N/A; MAX = 3.9								µs	12
Self Refresh Timing												
Exit self refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self refresh abort		tXS	MIN = tRFC + 10ns								ns	1
		tXS_ABORT	MIN = tRFC4 + 10ns								ns	1

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)	tXS_FAST	MIN = tRFC4 + 10ns								ns	1
Exit self refresh to commands requiring a locked DLL	tXSDLL	MIN = tDLLK (MIN)								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing	tCKESR	MIN = tCKE (MIN) + 1*n*CK								CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled	tCKESR_PAR	MIN = tCKE (MIN) + 1*n*CK + PL								CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)	tCKSRE	MIN = greater of (5CK, 10ns)								CK	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled	tCKSRE_PAR	MIN = greater of (5CK, 10ns) + PL								CK	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	tCKSRX	MIN = greater of (5CK, 10ns)								CK	1
Power-Down Timing											
Exit power-down with DLL on to any valid command	tXP	MIN = greater of 4CK or 6ns								CK	1
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled.	tXP_PAR	MIN = (greater of 4CK or 6ns) + PL								CK	1
CKE MIN pulse width	tCKE (MIN)	MIN = greater of 3CK or 5ns								CK	1
Command pass disable delay	tCPDED	1	–	4	–	4	–	4	–	CK	
Power-down entry to power-down exit timing	tPD	MIN = tCKE (MIN); MAX = 9 × tREFI								CK	
Begin power-down period prior to CKE registered HIGH	tANPD	WL - 1CK								CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of tANPD or tRFC - REFRESH command to CKE LOW time								CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	tANPD + tXSDLL								CK	
Power-Down Entry Minimum Timing											

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
ACTIVATE command to power-down entry	tACTPDEN	1	–	1	–	2	–	2	–	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	1	–	1	–	2	–	2	–	CK	
REFRESH command to power-down entry	tREFPDEN	1	–	1	–	2	–	2	–	CK	
MRS command to power-down entry	tMRSPDEN	MIN = tMOD (MIN)								CK	1
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1								CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	MIN = WL + 4 + tWR/tCK(AVG)								CK	1
WRITE command to power-down entry (BC4MRS)	tWRPBC4DEN	MIN = WL + 2 + tWR/tCK(AVG) CK								CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1								CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1 CK 1								CK	1
ODT Timing											
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2								CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2								CK	
R_{TT} dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	tAONAS	1	9	1	9	1	9	1	9	ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	tAOFAS	1	9	1	9	1	9	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1tCK	6	–	6	–	6	–	6	–	CK	
	ODTH8 2tCK	7	–	7	–	7	–	7	–		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1tCK	4	–	4	–	4	–	4	–	CK	
	ODTH4 2tCK	5	–	5	–	5	–	5	–		
Write Leveling Timing											
First DQS_t, DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	–	40	–	40	–	40	–	CK	

TABLE 81: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS: DDR4-1600 THROUGH DDR4-2400 (CONTINUED)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
DQS_t, DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	–	25	–	25	–	25	–	CK	
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	tWLS	0.13	–	0.13	–	0.13	–	0.13	–	CK	
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	–	0.13	–	0.13	–	0.13	–	CK	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	
Gear-Down Timing (Not Supported Below DDR4-2666)											
Exit reset from CKE HIGH to a valid MRS gear-down	tXPR_GEAR	N/A		N/A		N/A		N/A		CK	
CKE HIGH assert to gear-down enable time)	tXS_GEAR	N/A		N/A		N/A		N/A		CK	
MRS command to sync pulse time	tSYNC_GEAR	N/A		N/A		N/A		N/A		CK	
Sync pulse to first valid command	tCMD_GEAR	N/A		N/A		N/A		N/A		CK	
Gear-down setup time	tGEAR_setup	N/A	–	N/A	–	N/A	–	N/A	–	CK	
Gear-down hold time	tGEAR_hold	N/A		N/A	–	N/A	–	N/A	–	CK	

Notes:
1. Maximum limit not applicable.
2. ^{t}CCD_L and ^{t}DLLK should be programmed according to the value defined per operating frequency.
3. Although unlimited row accesses to the same row is allowed within the refresh period, excessive row accesses to the same row over a long term can result in degraded operation.
4. Data rate is less than or equal to 1333 Mb/s.
5. Data rate is less than or equal to TBD.
6. WRITE-to-READ when CRC and DM are both not enabled.
7. WRITE-to-READ delay when CRC and DM are both enabled.
8. The start of internal write transactions is defined as follows:
   - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
9. For these parameters, the device supports ^{t}*n*PARAM [nCK] = RU{^{t}PARAM [ns]/^{t}CK(AVG) [ns]}, in clock cycles, assuming all input clock jitter specifications are satisfied.
10. When operating in 1^{t}CK WRITE preamble mode.
11. When operating in 2^{t}CK WRITE preamble mode.
12. When CA parity mode is selected and the DLL-off mode is used, each REF command requires an additional "PL" added to ^{t}RFC refresh time.
13. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
14. Applicable from ^{t}CK (AVG) MIN to ^{t}CK (AVG) MAX as stated in the Speed Bin tables.
15. JEDEC specfies a minimum of five clocks.

Electrical Characteristics and AC Timing Parameters: 2666 Through 3200 Mbs

Table 82: Electrical Characteristics and AC Timing Parameters: DDR4 - 2666 through DDR4 - 3200

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200				Unit	Notes
			Min	Max	Min	Max	Min	Max				
Clock Timing												
Clock period average (DLL off mode)		tCK (DLL_OFF)	8	20	8	20	8	20			ns	
Clock period average		tCK (AVG, DLL_ON)	0.75	1.6	0.682	1.6	0.625	1.6			ns	14
High pulse width average		tCH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			CK	
Low pulse width average		tCL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52			Ck	
Clock period jitter	Total	tJITper_tot	–38	38	–34	34	–31	31			ps	
	Deterministic	tJITper_dj	–19	19	–17	17	–16	16			ps	
	DLL locking	tJITper,lck	–30	30	–27	27	–25	25			ps	
Clock absolute period		tCK (ABS)	MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK (AVG) MAX + tJITper_tot MAX								ps	
Clock absolute high pulse width (includes duty cycle jitter)		tCH (ABS)	0.45	–	0.45	–	0.45	–			tCK (AVG)	
Clock absolute low pulse width (includes duty cycle jitter)		tCL (ABS)	0.45	–	0.45	–	0.45	–			tCK (AVG)	
Cycle-to-cycle jitter	Total	tJITcc _tot	75		–68		63				ps	
	Deterministic	tJITcc _dj	38		–34		31				ps	
	DLL locking	tJITcc,lck	6		–68		50				ps	

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter		Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	DDR4-3200 Min	DDR4-3200 Max		Unit
Cumulative error across	2 cycles	^{t}ERR2per	–55	55	–50	50	–46	46		ps
	3 cycles	^{t}ERR3per	–66	66	–59	59	–55	55		ps
	4 cycles	^{t}ERR4per	–73	73	–66	66	–61	61		ps
	5 cycles	^{t}ERR5per	–79	79	–71	71	–65	65		ps
	6 cycles	^{t}ERR6per	–83	83	–75	75	–69	69		ps
	7 cycles	^{t}ERR7per	–87	87	–79	79	–73	73		ps
	8 cycles	^{t}ERR8per	–91	91	–82	82	–75	75		ps
	9 cycles	^{t}ERR9per	–94	94	–85	85	–78	78		ps
	10 cycles	^{t}ERR10per	–96	96	–87	87	–80	80		ps
	11 cycles	^{t}ERR11per	–99	99	–89	89	–82	82		ps
	12 cycles	^{t}ERR12per	–101	101	–91	91	–84	84		ps
	n = 13, 14 . . . 49, 50 cycles	^{t}ERR*n*per	^{t}ERR*n*per MIN = (1 + 0.68ln[*n*]) × ^{t}JITper MIN ^{t}ERR*n*per MAX = (1 + 0.68ln[*n*]) × ^{t}JITper MAX							ps
DQ Input Timing										
Data setup time to DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DS	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)							–
	Noncalibrated V_{REF}	^{t}PDA_S	minimum of 0.5IU							IU
Data hold time from DQS_t, DQS_c	Base (calibrated V_{REF})	^{t}DH	Refer to DQ Input Receiver Specification section (approximately 0.15^{t}CK to 0.28^{t}CK)							–
	Noncalibrated V_{REF}	^{t}PDA_H	minimum of 0.5IU							IU
DQ and DM minimum data pulse width for each input		^{t}DIPW	0.58	–	0.58	–	0.58	–		IU_d
DQ Output Timing (DLL enabled)										
DQS_t, DQS_c to DQ skew, per group, per access		^{t}DQSQ	–	0.18	–	0.18	–	0.18		IU_d
DQ output hold time from DQS_t, DQS_c		^{t}QH	0.74	–	0.74	–	0.74	–		IU_d
Data Valid Window per device: ^{t}QH - ^{t}DQSQ each device's output per UI		^{t}DVW$_d$	0.64		0.64		0.64			IU_d
Data Valid Window per device, per pin: ^{t}QH - ^{t}DQSQ each device's output per UI		^{t}DVW$_p$	0.72	–	0.72	–	0.72	–		IU_d
DQ Low-Z time from CK_t, CK_c		^{t}LZDQ	–340	140	–330	135	–320	130		ps

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200			Unit
		Min	Max	Min	Max	Min	Max		
DQ High-Z time from CK_t, CK_c	tHZDQ	–	140	–	135	–	130		ps
DQ Strobe Input Timing									
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1 tCKpreamble	$^{t}DQSS_{1ck}$	–0.27	0.27	–0.27	0.27	–0.27	0.27		CK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2 tCKpreamble	$^{t}DQSS_{2ck}$	–0.5	0.5	–0.5	0.5	–0.5	0.5		CK
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54		CK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54		CK
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge	tDSS	0.18	–	0.18	–	0.18	–		CK
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge	tDSH	0.18	–	0.18	–	0.18	–		CK
DQS_t, DQS_c differential WRITE preamble	tWPRE	0.9	–	0.9	–	0.9	–		CK
DQS_t, DQS_c differential WRITE postamble	tWPST	0.33	–	0.33	–	0.33	–		CK
DQS Strobe Output Timing (DLL enabled)									
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	tDQSCK	–170	170	–165	165	–160	160		ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKi	–	270	–	265	–	260		ps
DQS_t, DQS_c differential output high time	tQSH	0.40	–	0.40	–	0.40	–		CK
DQS_t, DQS_c differential output low time	tQSL	0.40	–	0.40	–	0.40	–		CK
DQS_t, DQS_c Low-Z time (RL - 1)	tLZDQS	–340	140	–330	130	–320	130		ps
DQS_t, DQS_c High-Z time (RL + BL/2)	tHZDQS	–	140	–	135	–	130		ps
DQS_t, DQS_c differential READ preamble	tRPRE	0.9	–	0.9	–	0.9	–		CK

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter		Symbol	DDR4-2666		DDR4-2933		DDR4-3200			Unit	Notes
			Min	Max	Min	Max	Min	Max			
Command and Address Timing											
DLL locking time		^{t}DLLK	854	–	940	–	1024	–		CK	2, 4
CMD, ADDR setup time to CK_t, CK_c Base referenced to $V_{IH(AC)}$ and $V_{IL(AC)}$ levels	Base	^{t}IS	55	–	48	–	40	–		ps	
	V_{REFCA}	^{t}IS$_{VREF}$	145	–	138	–	130	–		ps	
CMD, ADDR hold time to CK_t, CK_c Base referenced to $V_{IH(DC)}$ and $V_{IL(DC)}$ levels	Base	^{t}IH	80	–	73	–	65	–		ps	
	V_{REFCA}	^{t}IH$_{VREF}$	145	–	138	–	130	–		ps	
CTRL, ADDR pulse width for each input		^{t}IPW	385	–	365	–	320	–		ps	
ACTIVATE to internal READ or WRITE delay		^{t}RCD	See Speed Bin Tables for ^{t}RCD							ns	
PRECHARGE command period		^{t}RP	See Speed Bin Tables for ^{t}RP							ns	
ACTIVATE-to-PRECHARGE command period		^{t}RAS	See Speed Bin Tables for ^{t}RAS							ns	13
ACTIVATE-to-ACTIVATE or REF command period		^{t}RC	See Speed Bin Tables for ^{t}RC							ns	13
ACTIVATE-to-ACTIVATE command period to different bank groups for 1/2KB page size		^{t}RRD_S (1/2KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns			CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 1KB page size		^{t}RRD_S (1KB)	MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns		MIN = greater of 4CK or 3.0ns			CK	1
ACTIVATE-to-ACTIVATE command period to different bank groups for 2KB page size		^{t}RRD_S (2KB)	MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns		MIN = greater of 4CK or 5.3ns			CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1/2KB page size		^{t}RRD_L (1/2KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns			CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 1KB page size		^{t}RRD_L (1KB)	MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns		MIN = greater of 4CK or 4.9ns			CK	1
ACTIVATE-to-ACTIVATE command period to same bank groups for 2KB page size		^{t}RRD_L (2KB)	MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns		MIN = greater of 4CK or 6.4ns			CK	1

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Four ACTIVATE windows for 1/2KB page size	^{t}FAW (1/2KB)	MIN = greater of 16CK or 12ns		MIN = greater of 16CK or 12ns		MIN = greater of 16CK or 11.9ns		ns	
Four ACTIVATE windows for 1KB page size	^{t}FAW (1KB)	MIN = greater of 20CK or 25ns		MIN = greater of 20CK or 23ns		MIN = greater of 20CK or 21ns		ns	
Four ACTIVATE windows for 2KB page size	^{t}FAW (2KB)	MIN = greater of 28CK or 35ns		MIN = greater of 28CK or 30ns		MIN = greater of 28CK or 30ns		ns	
WRITE recovery time	^{t}WR	MIN = 15ns						ns	5, 10, 1
	^{t}WR$_2$	MIN = 1CK + ^{t}WR						CK	5, 11, 1
WRITE recovery time when CRC and DM are both enabled	^{t}WR_CRC_DM	MIN = ^{t}WR + greater of (5CK or 3.75ns)						CK	6, 10, 1
WRITE recovery time when CRC and DM are both enabled	^{t}WR_CRC_DM$_2$	MIN = 1CK + ^{t}WR_CRC_DM						CK	6, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group	^{t}WTR_L	MIN = greater of 4CK or 7.5ns						CK	5, 10, 1
	^{t}WTR_L$_2$	MIN = 1CK + ^{t}WTR_L						CK	5, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Same bank group when CRC and DM are both enabled	^{t}WTR_L_CRC_DM	MIN = ^{t}WTR_L + greater of (5CK or 3.75ns)						CK	6, 10, 1
	^{t}WTR_L_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_L_CRC_DM						CK	6, 10, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group	WTR_S	MIN = greater of (2CK or 2.5ns)						CK	5, 7, 8, 10, 1
	^{t}WTR_S$_2$	MIN = 1CK + ^{t}WTR_S						CK	5, 7, 8, 11, 1
Delay from start of internal WRITE transaction to internal READ command – Different bank group when CRC and DM are both enabled	^{t}WTR_S_CRC_DM	MIN = ^{t}WTR_S + greater of (5CK or 3.75ns)						CK	6, 7, 8, 10, 1
	^{t}WTR_S_CRC_DM$_2$	MIN = 1CK + ^{t}WTR_S_CRC_DM						CK	6, 7, 8, 11, 1
READ-to-PRECHARGE time	^{t}RTP	MIN = greater of 4CK or 7.5ns						CK	1
CAS_n-to-CAS_n command delay to different bank group	^{t}CCD_S	4	–	4	–	4	–	CK	

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS_n-to-CAS_n command delay to same bank group	tCCD_L	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–	MIN = greater of 4CK or 5ns	–			CK	
Auto precharge write recovery + precharge time	tDAL (MIN)	MIN = WR + ROUNDUP tRP/tCK (AVG); MAX = N/A								CK	
MRS Command Timing											
MRS command cycle time	tMRD	9	–	10	–	10	–			CK	
MRS command cycle time in PDA mode	tMRD_PDA	MIN = greater of (16nCK, 10ns)									1
MRS command cycle time in CAL mode	tMRD_CAL	MIN = tMOD + tCAL								CK	
MRS command update delay in PDA mode	tMOD	MIN = greater of (24nCK, 15ns)								CK	1
MRS command update delay	tMOD_PDA	MIN = tMOD								CK	
MRS command update delay in CAL mode	tMOD_CAL	MIN = tMOD + tCAL								CK	
MRS commandto DQS drive in preamble training	tSDO	MIN = tMOD + 9ns									
MPR Command Timing											
Multipurpose register recovery time	tMPRR	MIN = 1nCK								CK	
Multipurpose register write recovery time	tWR_MPRR	MIN = tMOD + AL + PL									
CRC Error Reporting Timing											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13			ns	
CRC ALERT_n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10			CK	
CA Parity Timing											
Parity latency	PL	6	–	8	–	8	–			CK	
Commands uncertain to be executed during this time	PAR_UNKNOWN	–	PL	–	PL	–	PL			CK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	–	PL + 6ns	–	PL + 6ns	–	PL + 6ns			CK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	80	160	88	176	96	192			CK	

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter		Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	DDR4-3200 Min	DDR4-3200 Max		Unit	Notes
Time from alert asserted until DES commands required in persistent CA parity mode		^{t}PAR_ALERT_RSP	–	71	–	78	–	85		CK	
CAL Timing											
CS_n to command address latency		^{t}CAL	5	–	6	–	6	–		CK	
CS_n to command address latency in gear-down mode		^{t}CALg	6	–	8	–	8	–		CK	
MPSM Timing											
Command path disable delay upopn MPSM entry		^{t}MPED	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)							CK	1
Valid clock requirement after MPSM entry		^{t}CKMPE	MIN = ^{t}MOD (MIN) + ^{t}CPDED (MIN)							CK	1
Valid clock requirement before MPSM exit		^{t}CKMPX	MIN = CK - ^{t}SRX (MIN)							CK	1
Exit MPSM to commands not requiring a locked DLL		^{t}XMP	^{t}XS (MIN)							CK	
Exit MPSM to commands requiring a locked DLL		^{t}XMPDLL	MIN = ^{t}XMP (MIN) + ^{t}XSDLL (MIN) CK 1							CK	1
CS setup time to CKE		^{t}MPX_S	MIN = ^{t}IS (MIN) + ^{t}IH (MIN)							ns	
CS_n HIGH hold time to CKE rising edge		^{t}MPX_HH	MIN = ^{t}XP							ns	
CS_n LOW hold time to CKE rising edge		^{t}MPX_LH	12	^{t}XMP-10ns	12	^{t}XMP-10ns	12	^{t}XMP-10ns		ns	
Connectivity Test Timing											
TEN pin HIGH to CS_n LOW – Enter CT mode		^{t}CT_Enable	200	–	200	–	200	–		ns	
CS_n LOW and valid input to valid output		^{t}CT_Valid	–	200	–	200	–	200		ns	
CK_t, CK_c valid and CKE HIGH after TEN goes HIGH		^{t}CPECT_Valid	10	–	10	–	10	–		ns	
Calibration and V_{REFDQ} Train Timing											
ZQCL command: Long calibration time	POWER-UP and RESET operation	^{t}ZQinit	1024	–	1024	–	1024	–		CK	
	Normal operation	^{t}ZQoper	512	–	512	–	512	–		CK	

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter		Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	DDR4-3200 Min	DDR4-3200 Max	Unit	Notes
ZQCS command: Short calibration time		^{t}ZQCS	128	–	128	–	128	–	CK	
The V_{REF} increment/decrement step time		V_{REF_time}	MIN = 150ns							
Enter V_{REFDQ} training mode to the first write or V_{REFDQ} MRS command delay		^{t}VREFDQE	MIN = 150ns						ns	1
Exit V_{REFDQ} training mode to the first WRITE command delay		^{t}VREFDQX	MIN = 150ns						ns	1
Initialization and Reset Timing										
Exit reset from CKE HIGH to a valid command		^{t}XPR	MIN = greater of 5CK or ^{t}RFC (MIN) + 10ns						CK	1
RESET_L pulse low after power stable		^{t}PW_REST_S	0.1	–	0.1	–	0.1	–	µs	
RESET_L pulse low at power-up		^{t}PW_REST_L	200	–	200	–	200	–	µs	
Begin power supply ramp to power supplies stable		^{t}VDDPR	MIN = N/A; MAX = 200						ms	
RESET_n LOW to power supplies stable		^{t}RPS	MIN = 0; MAX = 0						ns	
RESET_n LOW to I/O and R_{TT} High-Z		^{t}IOZ	MIN = N/A; MAX = undefined						ns	
Refresh Timing										
REFRESH-to-ACTIVATE or REFRESH command period (all bank groups)	4Gb	^{t}RFC1	MIN = 260						ns	1, 12
		^{t}RFC2	MIN = 160						ns	1, 12
		^{t}RFC4	MIN = 110						ns	1, 12
	8Gb	^{t}RFC1	MIN = 350						ns	1, 12
		^{t}RFC2	MIN = 260						ns	1, 12
		^{t}RFC4	MIN = 160						ns	1, 12
	16Gb	^{t}RFC1	MIN = 550						ns	1, 12
		^{t}RFC2	MIN = 405						ns	1, 12
		^{t}RFC4	MIN = 250						ns	1, 12
Average periodic refresh interval	0°C ≤ T_C ≤ 85°C	^{t}REFI	MIN = N/A; MAX = 7.8						µs	12
	85°C < T_C ≤ 95°C	^{t}REFI	MIN = N/A; MAX = 3.9						µs	12
Self Refresh Timing										
Exit self refresh to commands not requiring a locked DLL SRX to commands not requiring a locked DLL in self refresh abort		^{t}XS	MIN = ^{t}RFC + 10ns						ns	1
		^{t}XS_ABORT	MIN = ^{t}RFC4 + 10ns						ns	1

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter	Symbol	DDR4-2666 Min	DDR4-2666 Max	DDR4-2933 Min	DDR4-2933 Max	DDR4-3200 Min	DDR4-3200 Max	Unit	Notes
Exit self refresh to ZQCL, ZQCS and MRS (CL, CWL, WR, RTP and gear-down)	^{t}XS_FAST	MIN = ^{t}RFC4 + 10ns						ns	1
Exit self refresh to commands requiring a locked DLL	^{t}XSDLL	MIN = ^{t}DLLK (MIN)						CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing	^{t}CKESR	MIN = ^{t}CKE (MIN) + 1*n*CK						CK	1
Minimum CKE low pulse width for self refresh entry to self refresh exit timing when CA parity is enabled	^{t}CKESR_par	MIN = ^{t}CKE (MIN) + 1*n*CK + PL						CK	1
Valid clocks after self refresh entry (SRE) or power-down entry (PDE)	^{t}CKSRE	MIN = greater of (5CK, 10ns)						CK	1
Valid clock requirement after self refresh entry or power-down when CA parity is enabled	^{t}CKSRE_par	MIN = greater of (5CK, 10ns) + PL						CK	1
Valid clocks before self refresh exit (SRX) or power-down exit (PDX), or reset exit	^{t}CKSRX	MIN = greater of (5CK, 10ns)						CK	1
Power-Down Timing									
Exit power-down with DLL on to any valid command	^{t}XP	MIN = greater of 4CK or 6ns						CK	1
Exit precharge power-down with DLL frozen to commands not requiring a locked DLL when CA Parity is enabled.	^{t}XP_PAR	MIN = (greater of 4CK or 6ns) + PL						CK	1
CKE MIN pulse width	^{t}CKE (MIN)	MIN = greater of 3CK or 5ns						CK	1
Command pass disable delay	^{t}CPDED	5	–	5	–	6	–	CK	
Power-down entry to power-down exit timing	^{t}PD	MIN = ^{t}CKE (MIN); MAX = 9 × ^{t}REFI						CK	
Begin power-down period prior to CKE registered HIGH	^{t}ANPD	WL - 1CK						CK	
Power-down entry period: ODT either synchronous or asynchronous	PDE	Greater of ^{t}ANPD or ^{t}RFC - REFRESH command to CKE LOW time						CK	
Power-down exit period: ODT either synchronous or asynchronous	PDX	^{t}ANPD + ^{t}XSDLL						CK	
Power-Down Entry Minimum Timing									

TABLE 82: ELECTRICAL CHARACTERISTICS AND AC TIMING PARAMETERS (CONTINUED)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
ACTIVATE command to power-down entry	tACTPDEN	2	–	2	–	2	–	CK	
PRECHARGE/PRECHARGE ALL command to power-down entry	tPRPDEN	2	–	2	–	2	–	CK	
REFRESH command to power-down entry	tREFPDEN	2	–	2	–	2	–	CK	
MRS command to power-down entry	tMRSPDEN	MIN = tMOD (MIN)						CK	1
READ/READ with auto precharge command to power-down entry	tRDPDEN	MIN = RL + 4 + 1						CK	1
WRITE command to power-down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	MIN = WL + 4 + tWR/tCK(AVG)						CK	1
WRITE command to power-down entry (BC4MRS)	tWRPBC4DEN	MIN = WL + 2 + tWR/tCK(AVG) CK						CK	1
WRITE with auto precharge command to power-down entry (BL8OTF, BL8MRS,BC4OTF)	tWRAPDEN	MIN = WL + 4 + WR + 1						CK	1
WRITE with auto precharge command to power-down entry (BC4MRS)	tWRAPBC4DEN	MIN = WL + 2 + WR + 1 CK 1						CK	1
ODT Timing									
Direct ODT turn-on latency	DODTLon	WL - 2 = CWL + AL + PL - 2						CK	
Direct ODT turn-off latency	DODTLoff	WL - 2 = CWL + AL + PL - 2						CK	
R_{TT} dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	CK	
Asynchronous $R_{TT(NOM)}$ turn-on delay (DLL off)	tAONAS	1	9	1	9	1	9	ns	
Asynchronous $R_{TT(NOM)}$ turn-off delay (DLL off)	tAOFAS	1	9	1	9	1	9	ns	
ODT HIGH time with WRITE command and BL8	ODTH8 1tCK	6	–	6	–	6	–	CK	
	ODTH8 2tCK	7	–	7	–	7	–		
ODT HIGH time without WRITE command or with WRITE command and BC4	ODTH4 1tCK	4	–	4	–	4	–	CK	
	ODTH4 2tCK	5	–	5	–	5	–		
Write Leveling Timing									
First DQS_t, DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	–	40	–	40	–	CK	

Table 82: Electrical Characteristics and AC Timing Parameters (Continued)

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit
		Min	Max	Min	Max	Min	Max	
DQS_t, DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	–	25	–	25	–	CK
Write leveling setup from rising CK_t, CK_c crossing to rising DQS_t, DQS_c crossing	tWLS	0.13	–	0.13	–	0.13	–	CK
Write leveling hold from rising DQS_t, DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	–	0.13	–	0.13	–	CK
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns
Gear-Down Timing								
Exit reset from CKE HIGH to a valid MRS gear-down	tXPR_GEAR	tXPR		tXPR		tXPR		CK
CKE HIGH assert to gear-down enable time)	tXS_GEAR	tXS		tXS		tXS		CK
MRS command to sync pulse time	tSYNC_GEAR	tMOD + 4CK		tMOD + 4CK		tMOD + 4CK		CK
Sync pulse to first valid command	tCMD_GEAR	tMOD		tMOD		tMOD		CK
Gear-down setup time	tGEAR_setup	2CK	–	2CK	–	2CK	–	CK
Gear-down hold time	tGEAR_hold	2CK	–	2CK	–	2CK	–	CK

Notes:
1. Maximum limit not applicable.
2. tCCD_L and tDLLK should be programmed according to the value defined per operating frequency.
3. Data rate is less than or equal to 1333 MT/s.
4. Data rate is less than or equal to TBD.
5. WRITE-to-READ when CRC and DM are both not enabled.
6. WRITE-to-READ delay when CRC and DM are both enabled.
7. The start of internal write transactions is defined as follows:
   - For BL8 (fixed by MRS and on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (on-the-fly): rising clock edge four clock cycles after WL
   - For BC4 (fixed by MRS): rising clock edge two clock cycles after WL
8. For these parameters, the device supports tnPARAM [nCK] = RU{tPARAM [ns]/tCK(AVG) [ns]}, in clock cycles, assuming all input clock jitter specifications are satisfied.
9. Although unlimited row accesses to the same row is allowed within the refresh period, excessive row accesses to the same row over a long term can result in degraded operation.
10. When operating in 1tCK WRITE preamble mode.
11. When operating in 2tCK WRITE preamble mode.
12. When CA parity mode is selected and the DLLoff mode is used, each REF command requires an additional "PL" added to tRFC refresh time.
13. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime and/or reduction in data retention ability.
14. Applicable from tCK (AVG) MIN to tCK (AVG) MAX as stated in the Speed Bin tables.
15. JEDEC specfies a minimum of five clocks.
16. The maximum read postamble is bound by tDQSCK(MIN) plus tQSH(MIN) on the left side and tHZ(DQS)MAX on the right side.
17. The reference level of DQ output signal is specified with a midpoint as a widest part of output signal eye, which should be approximately 0.7 × VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $V_{TT} = V_{DDQ}$.

RESET and Initialization Procedure

Power-Up and Initialization Sequence

The following sequence is required for power-up and initialization:

1. Apply power (RESET_n and TEN must be maintained below $0.2 \times V_{DD}$ while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, RESET_n must be maintainedbelow $0.2 \times V_{DD}$ for a minimum of ^{t}PW_RESET_L and TEN must be maintained below $0.2 \times V_{DD}$ for a minimum of 700µs. CKE is pulled LOW anytime before RESET_n is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and (V_{DD} - V_{DDQ} < 0.3V). V_{PP} must ramp at the same time or before V_{DD}, and V_{PP} must be equal to or higher than V_{DD} at all times. After V_{DD} has ramped and reached the stable level, the initialization sequence must be started within 64ms.
   During power-up, either of the following conditions may exist and must be met:
   - Condition A:
     - Apply V_{PP} without any slope reversal before or at the same time as V_{DD} and V_{DDQ}.
     - V_{DD} and V_{DDQ} are driven from a single-power converter output and apply V_{DD}/V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
     - The voltage levels on all balls other than V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be greater than or equal to V_{SSQ} and V_{SS} on the other side.
     - V_{TT} is limited to 0.76V MAX when the power ramp is complete.
     - V_{REFCA} tracks V_{DD}/2.
   - Condition B:
     - Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
     - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
     - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
     - The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET_n is de-asserted, wait for another 500µs until CKE becomes active. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^{t}CK (whichever is larger) before CKE goes active. Because CKE is a synchronous signal, the corresponding setup time to clock (^{t}IS) must be met. Also, a DESELECT command must be registered (with ^{t}IS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^{t}DLLK and ^{t}ZQINIT.
4. The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^{t}DLLK and ^{t}ZQ_{INIT}.

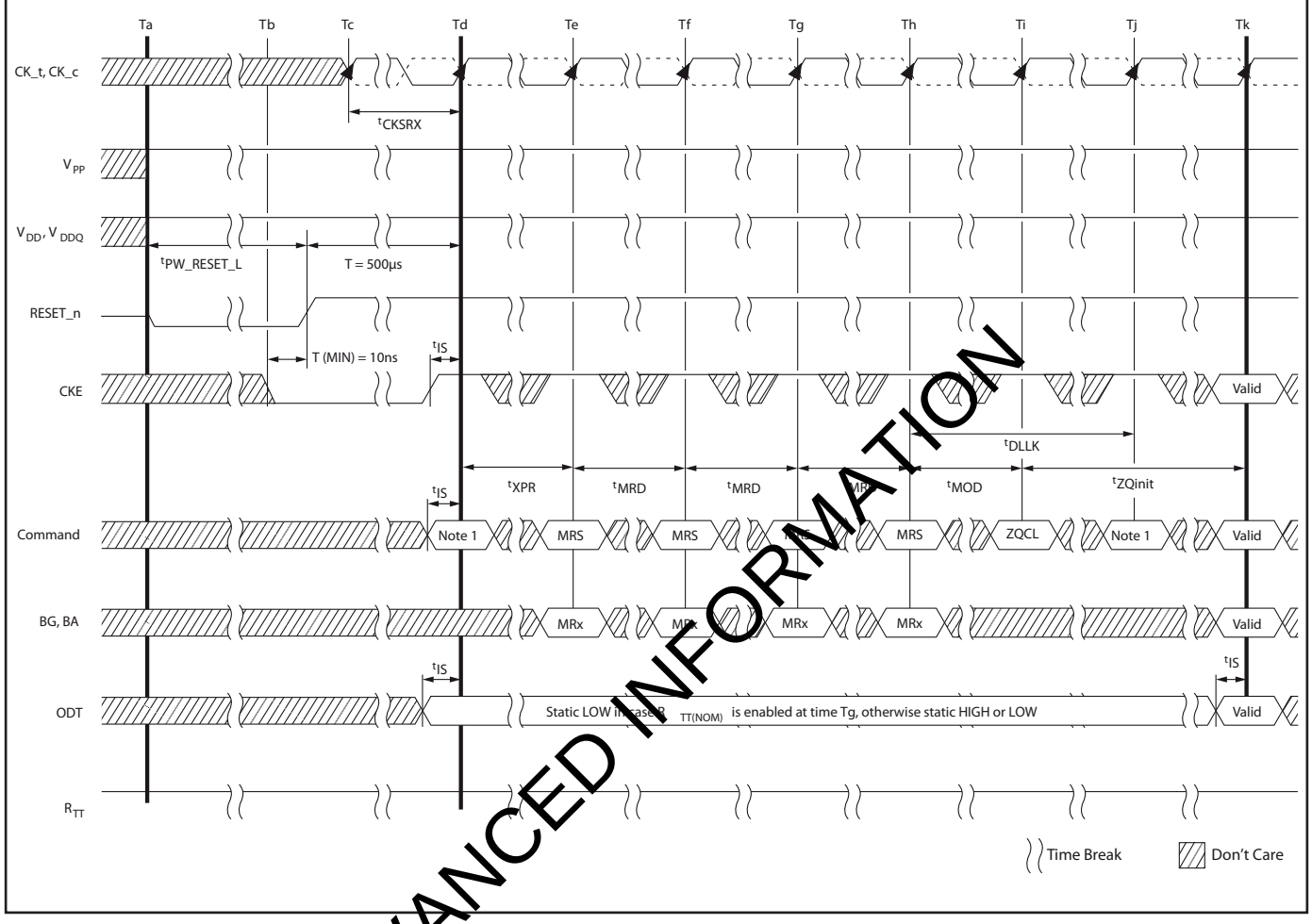
5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ^{t}XPR, before issuing the first MRS command to load mode register (^{t}XPR = MAX (^{t}XS; 5 × ^{t}CK).
6. Issue MRS command to load MR3 with all application settings, wait ^{t}MRD.
7. Issue MRS command to load MR6 with all application settings, wait ^{t}MRD.
8. Issue MRS command to load MR5 with all application settings, wait ^{t}MRD.
9. Issue MRS command to load MR4 with all application settings, wait ^{t}MRD.
10. Issue MRS command to load MR2 with all application settings, wait ^{t}MRD.
11. Issue MRS command to load MR1 with all application settings, wait ^{t}MRD.
12. Issue MRS command to load MR0 with all application settings, wait ^{t}MOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for ^{t}DLLK and ^{t}ZQINIT to complete.
15. The device will be ready for normal operation.

A stable valid V_{DD} level is a set DC level (0 Hz to 20 MHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 20 MHz) is allowed on VDD provided the noise doesn't alter V_{DD} to less than $V_{DD,min}$ or greater than $V_{DD,max}$.

A stable valid V_{DDQ} level is a set DC level (0 Hz to 20 MHz) and must be no less than $V_{DDQ,min}$ and no greater than $V_{DDQ,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 20 MHz) is allowed on V_{DDQ} provided the noise doesn't alter V_{DDQ} to less than $V_{DDQ,min}$ or greater than $V_{DDQ,max}$.

A stable valid V_{PP} level is a set DC level (0 Hz to 20 MHz) and must be no less than $V_{PP,min}$ and no greater than $V_{PP,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±120mV (greater than 20 MHz) is allowed on V_{PP} provided the noise doesn't alter V_{PP} to less than $V_{PP,min}$ or greater than $V_{PP,max}$.

Figure 50: RESET and Initialization Sequence at Power-On Ramping



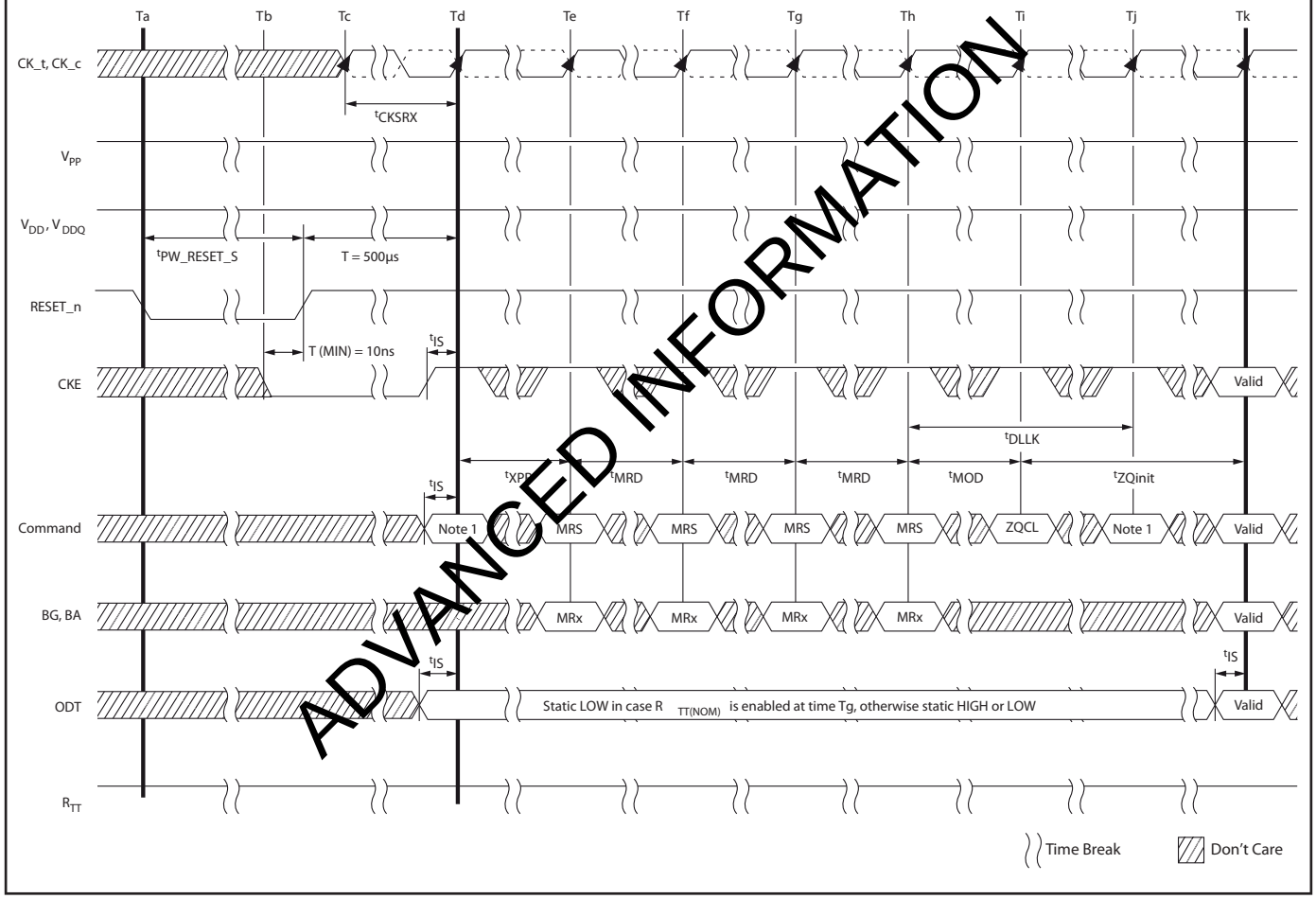
Notes:
1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.

The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET_n below 0.2 × V_{DD} any time reset is needed (all other inputs may be undefined). RESET must be maintained for a minimum of 100ns. CKE is pulled LOW before RESET_n is de-asserted (minimum time 10ns).
2. Follow Steps 2 to 7 in the Reset and Initialization Sequence at Power-on Ramping procedure.

When the reset sequence is complete, all counters except the refresh counters have been reset and the device is ready for normal operation.

FIGURE 51: RESET PROCEDURE AT POWER STABLE CONDITION



Notes:
1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.

Programming Mode Registers

Uncontrolled Power-Down Sequence

In the event of an uncontrolled ramping down of V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- Condition B: The amount that V_{PP} may be less than V_{DD}/V_{DDQ} is less than or equal to 500mV.
- Condition C: The time V_{PP} may be less than V_{DD} is ≤10ms per occurrence with a total accumulated time in this state ≤100ms.
- Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is ≤15ms per occurrence with a total accumulated time in this state ≤150ms.

Programming Mode Registers

For application flexibility, certain functions, features, and modes are programmable in seven mode registers (MR*n*) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because the default values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

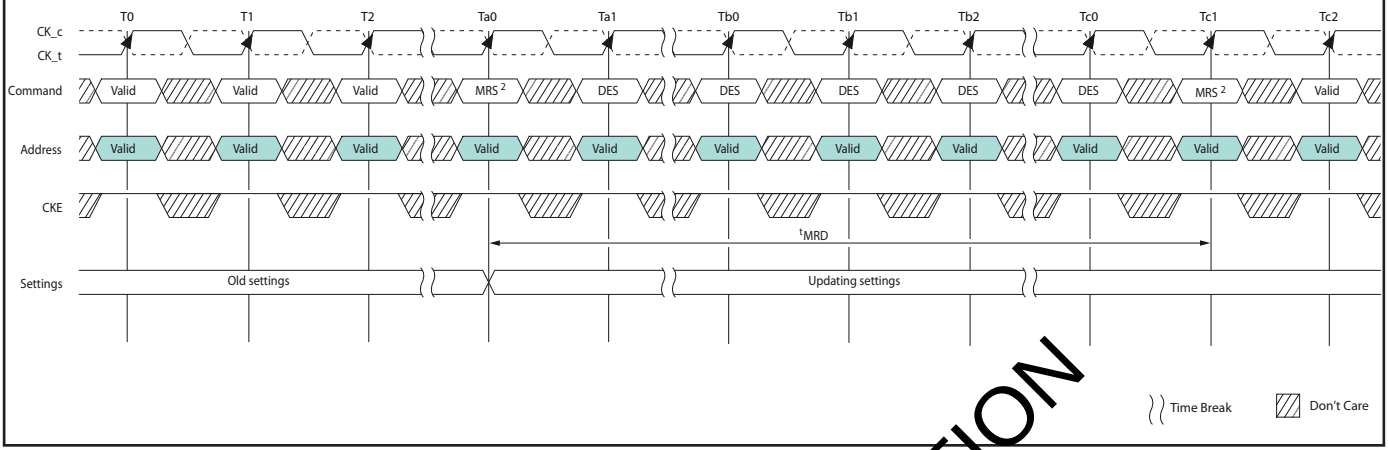
The MRS command cycle time, ^{t}MRD, is required to complete the WRITE operation to the mode register and is the minimum time required between the two MRS commands shown in the ^{t}MRD Timing figure.

Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply ^{t}MRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions:

- Gear-down mode
- Per-DRAM addressability
- Maximum power saving mode
- CS to command/address latency
- CA parity latency mode
- V_{REFDQ} training value
- V_{REFDQ} training mode
- V_{REFDQ} training range

Some mode register settings may not be supported because they are not required by certain speed bins.

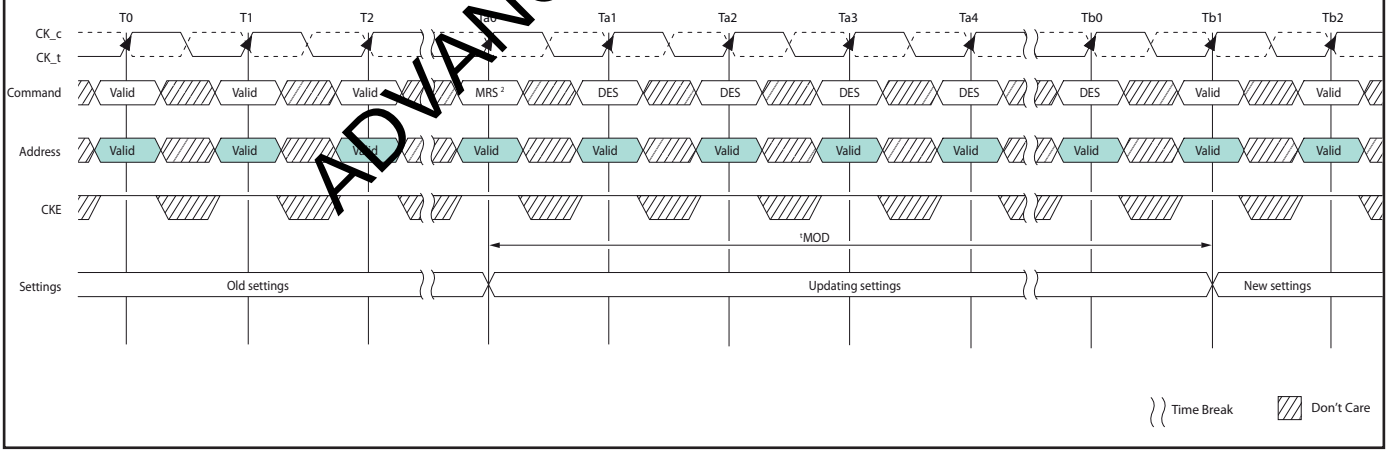
FIGURE 52: TMRD TIMING



Notes:
1. This timing diagram depicts CA parity mode "disabled" case.
2. tMRD applies to all MRS commands with the following exceptions:
   Gear-down mode
   CA parity mode
   CAL mode
   Per-DRAM addressability mode
   V_{REFDQ} training value, V_{REFDQ} training mode, and V_{REFDQ} training range

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET. tMOD is the minimum time required from an MRS command to a nonMRS command, excluding DES, as shown in the tMOD Timing figure.

FIGURE 53: TMOD TIMING



Notes:
1. This timing diagram depicts CA parity mode "disabled" case.
2. tMOD applies to all MRS commands with the following exceptions:
   DLL enable, Gear-down mode
   V_{REFDQ} training value, internal V_{REF} training monitor, V_{REFDQ} training mode, and V_{REFDQ} training range
   Maximum power savings mode , Per-DRAM addressability mode, and CA parity mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the $R_{TT(NOM)}$ feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring R_{TT} is in an off state prior to the MRS command. The ODT signal may be registered HIGH after ^{t}MOD has expired. If the $R_{TT(NOM)}$ feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes.

In some mode register setting cases, function updating takes longer than ^{t}MOD. This type of MRS does not apply ^{t}MOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

Mode register 0 (MR0) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR0 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR0 Register Definition table.

Mode Register 0

Table 83: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 84: MR0 Register Definition

Mode Register	Description
21	RFU 0 = Must be programmed to 0 0 = Must be programmed to 0
20:18	**MR select** **000 = MR0** 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13,11:9	WR (WRITE recovery)/RTP (READ-to-PRECHARGE) 0000 = 10 / 5 clocks[1] 0001 = 12 / 6 clocks 0010 = 14 / 7 clocks[1] 0011 = 16 / 8 / clocks 0100 = 18 / 9 clocks[1] 0101 = 20 /10 clocks 0110 = 24 / 12 clocks 0111 = 22 / 11 clocks[1] 1000 = 26 / 13 clocks[1] 1001 through 1111 = Reserved

TABLE 84: MR0 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
8	**DLL reset** 0 = No 1 = Yes
7	**Test mode (TM) – Manufacturer use only** 0 = Normal operating mode, must be programmed to 0
12, 6:4, 2	**CAS latency (CL) – Delay in clock cycles from the internal READ command to first data-out** 00000 = 9 clocks[1] 00001 = 10 clocks 00010 = 11 clocks[1] 00011 = 12 clocks 00100 = 13 clocks[1] 00101 = 14 clocks 00110 = 15 clocks[1] 00111 = 16 clocks 01000 = 18 clocks 01001 = 20 clocks 01010 = 22 clocks 01011 = 24 clocks 01100 = 23 clocks[1] 01101 = 17 clocks[1] 01110 = 19 clocks[1] 01111 = 21 clocks [1] 10000 = 25 clocks (3DS use only) 10001 = 26 clocks 10010 = 27 clocks (3DS use only) 10011 = 28 clocks 10100 = 29 clocks[1] 10101 = 30 clocks 10110 = 31 clocks[1] 10111 = 32 clocks
3	**Burst type (BT) – Data burst ordering within a READ or WRITE burst access** 0 = Nibble sequential 1 = Interleave
1:0	**Burst length (BL) – Data burst size associated with each read or write access** 00 = BL8 (fixed) 01 = BC4 or BL8 (on-the-fly) 10 = BC4 (fixed) 11 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following table. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selec-ted coincidentally with the registration of a READ or WRITE command via A12/BC_n.

Table 85: Burst Type and Burst Order

Note 1 applies to the entire table

Burst Length	READ/ WRITE	Starting Column Address (A[2, 1, 0])	Burst Type = Sequential (Decimal)	Burst Type = Interleaved (Decimal)	Notes
BC4	READ	0 0 0	1, 2, 3, 0, T, T, T, T	0, 1, 2, 3, T, T, T, T	2, 3
		0 0 1	1, 2, 3, 0, T, T, T, T	1, 0, 3, 2, T, T, T, T	2, 3
		0 1 0	2, 3, 0, 1, T, T, T, T	2, 3, 0, 1, T, T, T, T	2, 3
		0 1 1	3, 0, 1, 2, T, T, T, T	3, 2, 1, 0, T, T, T, T	2, 3
		1 0 0	4, 5, 6, 7, T, T, T, T	4, 5, 6, 7, T, T, T, T	2, 3
		1 0 1	5, 6, 7, 4, T, T, T, T	5, 4, 7, 6, T, T, T, T	2, 3
		1 1 0	6, 7, 4, 5, T, T, T, T	6, 7, 4, 5, T, T, T, T	2, 3
		1 1 1	7, 4, 5, 6, T, T, T, T	7, 6, 5, 4, T, T, T, T	2, 3
	WRITE	0, V, V	0, 1, 2, 3, X, X, X, X	0, 1, 2, 3, X, X, X, X	2, 3
		1, V, V,	4, 5, 6, 7, X, X, X, X	4, 5, 6, 7, X, X, X, X	2, 3
BL8	READ	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	
		0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6	
		0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5	
		0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4	
		1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3	
		1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2	
		1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1	
		1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0	
	WRITE	V, V, V	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7	3

Notes:
1. 0...7 bit number is the value of CA[2:0] that causes this bit to be the first read during a burst.
2. When setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode, meaning the starting point for ^{t}WR and ^{t}WTR will be pulled in by two clocks. When setting burst length to OTF in MR0, the internal WRITE operation starts at the same time as a BL8 (even if BC4 was selected during column time using A12/BC4_n) meaning that if the OTF MR0 setting is used, the starting point for ^{t}WR and ^{t}WTR will not be pulled in by two clocks as described in the BC4 (fixed) case.
3. T = Output driver for data and strobes are in High-Z.
   V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.
   X = "Don't Care."

CAS Latency

The CAS latency (CL) setting is defined in the MR0 Register Definition table. CAS laten-cy is the delay, in clock cycles, between the internal READ command and the availability of the first bit of output data. The device does not support half-clock latencies. The overall read latency (RL) is defined as additive latency (AL) + CAS latency (CL): RL = AL + CL.

Test Mode

The normal operating mode is selected by MR0[7] and all other bits set to the desired values shown in the MR0 Register Definition table. Programming MR0[7] to a value of 1 places the device into a DRAM manufacturer-defined test mode to be used only by the manufacturer, not by the end user. No operations or functionality is specified if MR0[7]
= 1.

Write Recovery (WR) / READ-to-PRECHARGE

The programmed write recovery (WR) value is used for the auto precharge feature along with tRP to determine ^{t}DAL. WR for auto precharge (MIN) in clock cycles is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up to the next integer: WR (MIN) cycles = roundup (tWR[ns]/^{t}CK[ns]). The WR value must be programmed to be equal to or larger than ^{t}WR (MIN). When both DM and write CRC are enabled in the mode register, the device calculates CRC before sending the write data into the array; ^{t}WR values will change when enabled. If there is a CRC error, the device blocks the WRITE operation and discards the data.

Internal READ-to-PRECHARGE (RTP) command delay for auto precharge (MIN) in clock cycles is calculated by dividing tRTP (in ns) by ^{t}CK (in ns) and rounding up to the next integer: RTP (MIN) cycles = roundup (tRTP[ns]/^{t}CK[ns]). The RTP value in the mode register must be programmed to be equal to or larger than RTP (MIN). The programmed RTP value is used with ^{t}RP to determine the ACT timing to the same bank.

DLL RESET

The DLL reset bit is self-clearing, meaning that it returns to the value of 0 after the DLL RESET function has been issued. After the DLL is enabled, a subsequent DLL RESET should be applied. Any time the DLL RESET function is used, ^{t}DLLK must be met before functions requiring the DLL can be used, such as READ commands or synchronous ODT operations, for example.)

Mode register 1 (MR1) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR1 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR1 Register Definition table.

Mode Register 1

Table 86: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 87: MR1 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 **001 = MR1** 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data output disable (Qoff) – Output buffer disable** 0 = Enabled (normal operation) 1 = Disabled (both ODI and RTT_{TT})
11	**Termination data strobe (TDQS) – Additional termination pins (x8 configuration only)** 0 = TDQS disabled 1 = TDQS enabled

TABLE 87: MR1 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
10, 9, 8	**Nominal ODT ($R_{TT(NOM)}$) – Data bus termination setting** 000 = $R_{TT(NOM)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
7	**Write leveling (WL) – Write leveling mode** 0 = Disabled (normal operation) 1 = Enabled (enter WL mode)
6, 5	**RFU** 0 = Must be programmed to 0 1 = Reserved
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 1[1] 10 = CL - 2 11 = Reserved
2, 1	**Output driver impedance (ODI) – Output driver impedance setting** 00 = RZQ/7 (34 ohm) 01 = RZQ/5 (48 ohm) 10 = Reserved (Although not JEDEC-defined and not tested, this setting will provide RZQ/6 or 40 ohm) 11 = Reserved
0	**DLL enable – DLL enable feature** 0 = DLL disabled 1 = DLL enabled (normal operation)

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

DLL Enable/DLL Disable

The DLL must be enabled for normal operation and is required during power-up initialization and upon returning to normal operation after having the DLL disabled. During normal operation (DLL enabled with MR1[0]) the DLL is automatically disabled when entering the SELF REFRESH operation and is automatically re-enabled upon exit of the SELF REFRESH operation. Any time the DLL is enabled and subsequently reset, ^{t}DLLK clock cycles must occur before a READ or SYNCHRONOUS ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}DQSCK, ^{t}AON, or ^{t}AOF parameters.

During ^{t}DLLK, CKE must continuously be registered HIGH. The device does not require DLL for any WRITE operation, except when $R_{TT(WR)}$ is enabled and the DLL is required for proper ODT operation.

The direct ODT feature is not supported during DLL off mode. The ODT resistors must be disabled by continuously registering the ODT pin LOW and/or by programming the RTT(NOM) bits MR1[9,6,2] = 000 via an MRS command during DLL off mode.

The dynamic ODT feature is not supported in DLL off mode; to disable dynamic ODT externally, use the MRS command to set RTT(WR), MR2[10:9] = 00

Output Driver Impedance Control

The output driver impedance of the device is selected by MR1[2,1], as shown in the MR1 Register Definition table.

ODT $R_{TT(NOM)}$ Values

The device is capable of providing three different termination values: $R_{TT(Static)}$, $R_{TT(NOM)}$, and $R_{TT(WR)}$. The nominal termination value, $R_{TT(NOM)}$, is programmed in MR1. A separate value, $R_{TT(WR)}$, may be programmed in MR2 to enable a unique R_{TT} value when ODT is enabled during WRITE operations. The $R_{TT(WR)}$ value can be applied during WRITE commands even when $R_{TT(NOM)}$ is disabled. A third R_{TT} value, $R_{TT(Static)}$, is programed in MR5. $R_{TT(Static)}$ provides a termination value when the ODT signal is LOW.

Additive Latency

The ADDITIVE LATENCY (AL) operation is supported to make command and data buses efficient for sustainable bandwidths in the device. In this operation, the device allows a READ or WRITE command (either with or without auto precharge) to be issued immediately after the ACTIVATE command. The command is held for the time of AL before it is issued inside the device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL) register settings. WRITE latency (WL) is controlled by the sum of the AL and CAS WRITE latency (CWL) register settings.

Table 88: Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note: 1. AL has a value of CL - 1 or CL - 2 based on the CL values programmed in the MR0 register.

Write Leveling

For better signal integrity, fly-by topology is frequently used for the commands, addresses, control signals, and clocks. Fly-by topology benefits from a reduced number of stubs and their lengths, but it causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write leveling feature that allows the controller to compensate for skew.

Output Disable

The device outputs may be enabled/disabled by MR1[12] as shown in the MR1 Register Definition table. When MR1[12] is enabled (MR1[12] = 1) all output pins (such as DQ and DQS) are disconnected from the device, which removes any loading of the output drivers. For example, this feature may be useful when measuring module power. For normal operation, set MR1[12] to 0.

Mode Register 2

Mode register 2 (MR2) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR2 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR2 Register Definition table.

TABLE 89: ADDRESS PIN MAPPING

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

TABLE 90: MR2 REGISTER DEFINITION

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 **010 = MR2** 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**TRR mode** 0 = Disabled 1 = Enabled
12	**WRITE data bus CRC** 0 = Disabled 1 = Enabled

TABLE 90: MR2 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
11:9	**Dynamic ODT ($R_{TT(WR)}$) – Data bus termination setting during WRITEs** 000 = $R_{TT(WR)}$ disabled (WRITE does not affect R_{TT} value) 001 = RZQ/2 (120 ohm) 010 = RZQ/1 (240 ohm) 011 = High-Z 100 = RZQ/3 (80 ohm) 101 = Reserved 110 = Reserved 111 = Reserved
7:6	**Low-power auto self refresh (LPASR) – Mode summary** 00 = Manual mode - Normal operating temperature range (T_C: 0°C–85°C) 01 = Manual mode - Reduced operating temperature range (T_C: 0°C–45°C) 10 = Manual mode - Extended operating temperature range (T_C: 0°C–95°C) 11 = ASR mode - Automatically switching among all modes
5:3	**CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 1^t CK WRITE preamble** 000 = 9 (DDR4-1600)[1] 001 = 10 (DDR4-1866) 010 = 11 (DDR4-2133/1600)[1] 011 = 12 (DDR4-2400/1866) 100 = 14 (DDR4-2666/2133) 101 = 16 (DDR4-2933,3200/2400) 110 = 18 (DDR4-2666) 111 = 20 (DDR4-2933, 3200)
	CAS WRITE latency (CWL) – Delay in clock cycles from the internal WRITE command to first data-in 2^{t}CK WRITE preamble 000 = N/A 001 = N/A 010 = N/A 011 = N/A 100 = 14 (DDR4-2400) 101 = 16 (DDR4-2666/2400) 110 = 18 (DDR4-2933, 3200/2666) 111 = 20 (DDR4-2933, 3200)
8, 2	**TRR mode - BG*n* control** 00 = BG0 01 = BG1 10 = BG2 11 = BG3
1:0	**TRR mode - BA*n* control** 00 = BA0 01 = BA1 10 = BA2 11 = BA3

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

CAS WRITE Latency

CAS WRITE latency (CWL) is defined by MR2[5:3] as shown in the MR2 Register Definition table. CWL is the delay, in clock cycles, between the internal WRITE command and the availability of the first bit of input data. The device does not support any half-clock latencies. The overall WRITE latency (WL) is defined as additive latency (AL) + parity latency (PL) + CAS WRITE latency (CWL): WL = AL +PL + CWL.

Low-Power Auto Self Refresh

Low-power auto self refresh (LPASR) is supported in the device. Applications requiring SELF REFRESH operation over different temperature ranges can use this feature to optimize the IDD6 current for a given temperature range as specified in the MR2 Register Definition table.

Dynamic ODT

In certain applications and to further enhance signal integrity on the data bus, it is desirable to change the termination strength of the device without issuing an MRS command. This may be done by configuring the dynamic ODT ($R_{TT(WR)}$) settings in MR2[11:9]. In write leveling mode, only $R_{TT(NOM)}$ is available.

Write Cyclic Redundancy Check Data Bus

The write cyclic redundancy check (CRC) data bus feature during writes has been added to the device. When enabled via the mode register, the data transfer size goes from the normal 8-bit (BL8) frame to a larger 10-bit UI frame, and the extra two UIs are used for the CRC information.

Target Row Refresh Mode

For the device, rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (^{t}MAW) before the adjacent rows need to be refreshed, regardless of how the activates are distributed over ^{t}MAW. The row receiving the excessive activates is the target row (TR*n*); the two adjacent rows to be refreshed are the victim rows.

When the MAC limit is reached on TRn, either the device must receive (roundup of ^{t}MAW / ^{t}REFI) REFRESH commands (REF) before another row activate is issued, or it needs to be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered the MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the activates from two target rows on a victim row should not exceed the MAC value as well. When the temperature controlled refresh (TCR) mode is enabled, ^{t}MAW should be adjusted depending on the TCR range as shown in the following table.

Using TRR mode is not required, and in some cases has been rendered inoperable, as the device automatically performs TRR Mode in the background.

Mode Register 3

Mode register 3 (MR3) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR3 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR3 Register Definition table.

Table 91: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 92: MR3 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 **011 = MR3** 100 = MR4 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:11	**Multipurpose register (MPR) – Read format** 00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
10:9	**WRITE CMD latency when CRC/DM enabled** 00 = 4CK (DDR4-1600) 01 = 5CK (DDR4-1866/2133/2400) 10 = 6CK (DDR4-2666/2933/3200) 11 = Reserved

TABLE 92: MR3 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
8:6	**Fine granularity refresh mode** 000 = Normal mode (fixed 1x) 001 = Fixed 2x 010 = Fixed 4x 011 = Reserved 100 = Reserved 101 = On-the-fly 1x/2x 110 = On-the-fly 1x/4x 111 = Reserved
5	**Temperature sensor status** 0 = Disabled 1 = Enabled
4	**Per-DRAM addressability** 0 = Normal operation (disabled) 1 = Enable
3	**Gear-down mode – Ratio of internal clock to external data rate** 0 = [1:1]; (1/2 rate data) 1 = [2:1]; (1/4 rate data)
2	**Multipurpose register (MPR) access** 0 = Normal operation 1 = Data flow from MPR
1:0	**MPR page select** 00 = Page 0 01 = Page 1 10 = Page 2 11 = Page 3 (restricted for DRAM manufacturer use only)

Multipurpose Register

The multipurpose register (MPR) is used for several features:

- Readout of the contents of the MR*n* registers
- WRITE and READ system patterns used for data bus calibration
- Readout of the error frame when the command address parity feature is enabled

To enable MPR, issue an MRS command to MR3[2] = 1. MR3[12:11] define the format of read data from the MPR. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and ^{t}RP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power-down mode, SELF REFRESH, and any other nonRD/RDA or nonWR/WRA commands are not allowed during MPR mode. The RESET function is supported during MPR mode, which requires device re-initialization.

WRITE Command Latency When CRC/DM is Enabled

The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode. This provides the extra time required when completing a WRITE burst when write CRC and DM are enabled.

Fine Granularity Refresh Mode

This mode had been added to DDR4 to help combat the performance penalty due to refresh lockout at high densities. Shortening ^{t}RFC and increasing cycle time allows more accesses to the chip and can produce higher bandwidth.

Temperature Sensor Status

This mode directs the DRAM to update the temperature sensor status at MPR Page 2, MPR0 [4,3]. The temperature sensor setting should be updated within 32ms; when an MPR read of the temperature sensor status bits occurs, the temperature sensor status should be no older than 32ms.

Per-DRAM Addressability

This mode allows commands to be masked on a per device basis providing any device in a rank (devices sharing the same command and address signals) to be programmed individually. As an example, this feature can be used to program different ODT or VREF values on DRAM devices within a given rank.

Gear-Down Mode

The device defaults in 1/2 rate (1N) clock mode and uses a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. For operation in 1/2 rate mode, no MRS command or sync pulse is required.

Mode Register 4

Mode register 4 (MR4) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR4 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR4 Register Definition table.

TABLE 93: ADDRESS PIN MAPPING

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET (MRS) command.

TABLE 94: MR4 REGISTER DEFINITION

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 **100 = MR4** 101 = MR5 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**Post Package Repair (PPR mode)** 0 = Disabled 1 = Enabled
12	**WRITE preamble setting** 0 = 1^{t}CK toggle[1] 1 = 2^{t}CK toggle
11	**READ preamble setting** 0 = 1^{t}CK toggle[1] 1 = 2^{t}CK toggle (When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.)
10	**READ preamble training** 0 = Disabled 1 = Enabled

TABLE 94: MR4 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
9	**Self refresh abort mode** 0 = Disabled 1 = Enabled
8:6	**CMD (CAL) address latency** 000 = 0 clocks (disabled) 001 =3 clocks[1] 010 = 4 clocks 011 = 5 clocks[1] 100 = 6 clocks 101 = 8 clocks 110 = Reserved 111 = Reserved
5	**soft Post Package Repair (sPPR mode)** 0 = Disabled 1 = Enabled
4	**Internal V_{REF} monitor** 0 = Disabled 1 = Enabled
3	**Temperature controlled refresh mode** 0 = Disabled 1 = Enabled
2	**Temperature controlled refresh range** 0 = Normal temperature mode 1 = Extended temperature mode
1	**Maximum power savings mode** 0 = Normal operation 1 = Enabled
0	**RFU** 0 = Must be programmed to 0 1 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

WRITE Preamble

Programmable WRITE preamble, ^{t}WPRE, can be set to 1^{t}CK or 2^{t}CK via the MR4 register. The 1^{t}CK setting is similar to DDR3. However, when operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

READ Preamble

Programmable READ preamble ^{t}RPRE can be set to 1^{t}CK or 2^{t}CK via the MR4 register. Both the 1^{t}CK and 2^{t}CK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range. Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble Training

Programmable READ preamble training can be set to 1^{t}CK or 2^{t}CK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature- Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of 0°C to 85°C, while the extended temperature range covers 0°C to 95°C.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register and is based on the roundup (in clocks) of [^{t}CK(ns)/^{t}CAL(ns)].

Internal VREF Monitor

The device generates its own internal V_{REFDQ}. This mode may be enabled during V_{REFDQ} training, and when enabled, $V_{REF,time\text{-}short}$ and $V_{REF,time\text{-}long}$ need to be increased by 10ns if DQ0, DQ1, DQ2, or DQ3 have 0pF loading. An additional 15ns per pF of loading is also needed.

Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

Mode Register 5

Mode register 5 (MR5) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR5 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR5 Register Definition table.

TABLE 95: ADDRESS PIN MAPPING

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

TABLE 96: MR5 REGISTER DEFINITION

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 **101 = MR5** 110 = MR6 111 = DNU
17	**N/A on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12	**Data bus inversion (DBI) – READ DBI enable** 0 = Disabled 1 = Enabled
11	**Data bus inversion (DBI) – WRITE DBI enable** 0 = Disabled 1 = Enabled
10	**Data mask (DM)** 0 = Disabled 1 = Enabled

TABLE 96: MR5 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
9	**CA parity persistent error mode** 0 = Disabled 1 = Enabled
8:6	**Parked ODT value ($_{TT(Park)}$)** 000 = $R_{TT(Park)}$ disabled 001 = RZQ/4 (60 ohm) 010 = RZQ/2 (120 ohm) 011 = RZQ/6 (40 ohm) 100 = RZQ/1 (240 ohm) 101 = RZQ/5 (48 ohm) 110 = RZQ/3 (80 ohm) 111 = RZQ/7 (34 ohm)
5	**ODT input buffer for power-down** 0 = Buffer enabled 1 = Buffer disabled
4	**CA parity error status** 0 = Clear 1 = Error
3	**CRC error status** 0 = Clear 1 = Error
2:0	**CA parity latency mode** 000 = Disable 001 = 4 clocks (DDR4-1600/1866/2133) 010 = 5 clocks (DDR4-2400)[1] 011 = 6 clocks (DDR4-2666) 100 = 8 clocks (DDR4-2933/3200) 101 = Reserved 110 = Reserved 111 = Reserved

Note: 1. Not allowed when 1/4 rate gear-down mode is enabled.

Data Bus Inversion

The DATA BUS INVERSION (DBI) function has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DBI function shares a common pin with the DM and TDQS functions. The DBI function applies to both READ and WRITE operations; Write DBI cannot be enabled at the same time the DM function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI). DBI is not allowed during MPR READ operation; during an MPR read, the DRAM ignores the read DBI enable setting in MR5 bit A12. DBI is not allowed during MPR READ operations.

Data Mask

The DATA MASK (DM) function, also described as a partial write, has been added to the device and is supported only for x8 and x16 configurations (x4 is not supported). The DM function shares a common pin with the DBI and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the write DBI function is enabled. Refer to the TDQS Function Matrix table for valid configurations for all three functions (TDQS/DM/DBI).

CA Parity Persistent Error Mode

Normal CA parity mode (CA parity persistent mode disabled) no longer performs CA parity checking while the parity error status bit remains set at 1. However, with CA parity persistent mode enabled, CA parity checking continues to be performed when the parity error status bit is set to a 1.

ODT Input Buffer for Power-Down

This feature determines whether the ODT input buffer is on or off during power-down. If the input buffer is configured to be on (enabled during power-down), the ODT input signal must be at a valid logic level. If the input buffer is configured to be off (disabled during power-down), the ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. However, the device may provide $R_{TT(Park)}$ termination depending on the MR settings. This is primarily for additional power savings.

CA Parity Error Status

The device will set the error status bit to 1 upon detecting a parity error. The parity error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CRC Error Status

The device will set the error status bit to 1 upon detecting a CRC error. The CRC error status bit remains set at 1 until the device controller clears it explicitly using an MRS command.

CA Parity Latency Mode

CA parity is enabled when a latency value, dependent on tCK, is programmed; this accounts for parity calculation delay internal to the device. The normal state of CA parity is to be disabled. If CA parity is enabled, the device must ensure there are no parity errors before executing the command. CA parity signal (PAR) covers ACT_n, RAS_n/A16 , CAS_n/A15, WE_n/A14, and the address bus including bank address and bank group bits. The control signals CKE, ODT, and CS_n are not included in the parity calculation.

Mode Register 6

Mode register 6 (MR6) controls various device operating modes as shown in the following register definition table. Not all settings listed may be available on a die; only settings required for speed bin support are available. MR6 is written by issuing the MRS command while controlling the states of the BGx, BAx, and Ax address pins. The mapping of address pins during the MRS command is shown in the following MR6 Register Definition table.

Table 97: Address Pin Mapping

Address bus	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode register	21	20	19	18	17	–	–	–	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Note: 1. RAS_n, CAS_n, and WE_n must be LOW during MODE REGISTER SET command.

Table 98: MR6 Register Definition

Mode Register	Description
21	**RFU** 0 = Must be programmed to 0 1 = Reserved
20:18	**MR select** 000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 **110 = MR6** 111 = DNU
17	**NA on 4Gb and 8Gb, RFU** 0 = Must be programmed to 0 1 = Reserved
13	**RFU** 0 = Must be programmed to 0 1 = Reserved
12:10	**^{t}CCD_L** 000 = 4 clocks (≤1333 Mb/s) 001 = 5 clocks (>1333 Mb/s and ≤1866 Mb/s) 010 = 6 clocks (>1866 Mb/s and ≤2400 Mb/s) 011 = 7 clocks (>2400 Mb/s and ≤2666 Mb/s) 100 = 8 clocks (>2666 Mb/s and ≤3200 Mb/s) 101 = Reserved 110 = Reserved 111 = Reserved

TABLE 98: MR6 REGISTER DEFINITION (CONTINUED)

Mode Register	Description
9, 8	**RFU** 0 = Must be programmed to 0 1 = Reserved
7	**V_{REF} Calibration Enable** 0 = Disable 1 = Enable
6	**V_{REF} Calibration Range** 0 = Range 1 1 = Range 2
5:0	**V_{REF} Calibration Value** See the V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section

tCCD_L Programming

The device controller must program the correct tCCD_L value. tCCD_L will be programmed according to the value defined per operating frequency in the AC parameter table. Although JEDEC specifies the larger of 5*n*CK or Xns, Micron's DRAM supports the larger of 4*n*CK or Xns.

V_{REFDQ} Calibration Enable

V_{REFDQ} calibration is where the device internally generates its own V_{REFDQ} to be used by the DQ input receivers. The V_{REFDQ} value will be output on any DQ of DQ[3:0] for evaluation only. The device controller is responsible for setting and calibrating the internal V_{REFDQ} level using an MRS protocol (adjust up, adjust down, and so on). It is assumed that the controller will use a series of writes and reads in conduction with V_{REFDQ} adjustments to optimize and verify the data eye. Enabling V_{REFDQ} calibration must be used whenever values are being written to the MR6[6:0] register.

V_{REFDQ} Calibration Range

The device defines two V_{REFDQ} calibration ranges: Range 1 and Range 2. Range 1 supports V_{REFDQ} between 60% and 92% of V_{DDQ} while Range 2 supports V_{REFDQ} between 45% and 77% of V_{DDQ}, as seen in V_{REFDQ} Specification table. Although not a restriction, Range 1 was targeted for module-based designs and Range 2 was added to target pointto-point designs.

V_{REFDQ} Calibration Value

Fifty settings provide approximately 0.65% of granularity steps sizes for both Range 1 and Range 2 of V_{REFDQ}, as seen in V_{REFDQ} Range and Levels table in the V_{REFDQ} Calibration section.

Table 99: Command Truth Table

Notes 1–5 apply to the entire table; Note 6 applies to all READ/WRITE commands

Function		Symbol	Prev. CKE	Pres. CKE	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	BG[1:0]	BA [1:0]	C[2:0]	A12/BC_n	A[13,11]	A10/AP	A[9:0]	Notes
MODE REGISTER SET		MRS	H	H	L	H	L	L	L	BG	BA	V	OP code				7
REFRESH		REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self refresh entry		SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	8, 9, 10
Self refresh exit		SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	8, 9, 10
					L	H	H	H	H	V	V	V	V	V	V	V	11
Single-bank PRECHARGE		PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
PRECHARGE all banks		PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
Reserved for future use		RFU	H	H	L	H	L	H	H	RFU							
Bank ACTIVATE		ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
WRITE	BL8 fixed, BC4 fixed	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
	BC4OTF	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
	BL8OTF	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
WRITE with auto precharge	BL8 fixed, BC4 fixed	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
	BC4OTF	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
	BL8OTF	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
READ	BL8 fixed, BC4 fixed	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
	BC4OTF	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
	BL8OTF	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
READ with auto precharge	BL8 fixed, BC4 fixed	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
	BC4OTF	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
	BL8OTF	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
NO OPERATION		NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	12
Device DESELECTED		DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	13
Power-down entry		PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
Power-down exit		PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	10, 14
ZQ CALIBRATION LONG		ZQCL	H	H	L	H	H	H	L	X	X	X	X	X	H	X	
ZQ CALIBRATION SHORT		ZQCS	H	H	L	H	H	H	L	X	X	X	X	X	L	X	

Truth Table Notes

Notes:

1. • BG = Bank group address
   • BA = Bank address
   • RA = Row address
   • CA = Column address
   • BC_n = Burst chop
   • X = "Don't Care"
   • V = Valid
2. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, and CKE at the rising edge of the clock. The MSB of BG, BA, RA, and CA are device density- and configuration-dependent. When ACT_n = H, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n, respectively. When ACT_n = L, pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14, respectively.
3. RESET_n is enabled LOW and is used only for asynchronous reset and must be maintained HIGH during any function.
4. Bank group addresses (BG) and bank addresses (BA) determine which bank within a bank group is being operated upon. For MRS commands, the BG and BA selects the specific mode register location.
5. V means HIGH or LOW (but a defined logic level), and X means either defined or undefined (such as floating) logic level.
6. READ or WRITE bursts cannot be terminated or interrupted, and fixed/on-the-fly (OTF) BL will be defined by MRS.
7. During an MRS command, A17 is RFU and is device density- and configuration-dependent.
8. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
9. VPP and VREF (VREFCA) must be maintained during SELF REFRESH operation.
10. Refer to the Truth Table – CKE table for more details about CKE transition.
11. Controller guarantees self refresh exit to be synchronous. DRAM implementation has the choice of either synchronous or asynchronous.
12. The NO OPERATION (NOP) command may be used only when exiting maximum power saving mode or when entering gear-down mode.
13. The NOP command may not be used in place of the DESELECT command.
14. The power-down mode does not perform any REFRESH operation.

Table 100: CKE Truth Table

Note 1 applies to the entire table

Current State	CKE		Command (n)	Action (n)	Notes
	Previous Cycle (n - 1)	Present Cycle (n)			
Power-down	L	L	X	Maintain power-down	8, 10, 11
	L	H	DES	Power-down exit	8, 10, 12
Self refresh	L	L	X	Maintain self refresh	11, 13
	L	H	DES	Self refresh exit	8, 13, 14, 15
Bank(s) active	H	L	DES	Active power-down entry	8, 10, 12, 16
Reading	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Writing	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Precharging	H	L	DES	Power-down entry	8, 10, 12, 16, 17
Refreshing	H	L	DES	Precharge power-down entry	8, 12
All banks idle	H	L	DES	Precharge power-down entry	8, 10, 12, 16, 18
	H	L	REFRESH	Self refresh	16, 18, 19

Notes:
1. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge n.
2. CKE (n) is the logic state of CKE at clock edge n; CKE (n-1) was the state of CKE at the previous clock edge.
3. COMMAND (n) is the command registered at clock edge n, and ACTION (n) is a result of COMMAND (n); ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh.
6. During any CKE transition (registration of CKE H->L or CKE H->L), the CKE level must be maintained until 1 nCK prior to ^{t}CKE (MIN) being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Truth Table – Command table.
8. For power-down entry and exit parameters, see the Power-Down Modes section.
9. CKE LOW is allowed only if ^{t}MRD and ^{t}MOD are satisfied.
10. The power-down mode does not perform any REFRESH operations.
11. X = "Don't Care" (including floating around VREF) in self refresh and power-down. X also applies to address pins.
12. The DESELECT command is the only valid command for power-down entry and exit.
13. VPP and V_{REFCA} must be maintained during SELF REFRESH operation.
14. On self refresh exit, the DESELECT command must be issued on every clock edge occurring during the ^{t}XS period. READ or ODT commands may be issued only after ^{t}XSDLL is satisfied.
15. The DESELECT command is the only valid command for self refresh exit.
16. Self refresh cannot be entered during READ or WRITE operations. For a detailed list of restrictions see the SELF REFRESH Operation and Power-Down Modes sections.
17. If all banks are closed at the conclusion of the READ, WRITE, or PRECHARGE command, then precharge power-down is entered; otherwise, active power-down is entered.

18. Idle state is defined as all banks are closed (tRP, tDAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, and so on), as well as all self refresh exit and power-down exit parameters are satisfied (tXS, tXP, tXSDLL, and so on).
19. Self refresh mode can be entered only from the all banks idle state.
20. For more details about all signals, see the Truth Table – Command table; must be a legal command as defined in the table.

NOP Command

NOP Command

The NO OPERATION (NOP) command was originally used to instruct the selected DDR4 SDRAM to perform a NOP (CS_n = LOW and ACT_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 = HIGH). This prevented unwanted commands from being registered during idle or wait states. NOP command general support has been removed and the command should not be used unless specifically allowed, which is when exiting maximum power-saving mode or when entering gear-down mode.

DESELECT Command

The deselect function (CS_n HIGH) prevents new commands from being executed; therefore, with this command, the device is effectively deselected. Operations already in progress are not affected.

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to 0, which will disable the DLL for subsequent operations until the A0 bit is set back to 1. The MR1 A0 bit for DLL control can be switched either during initialization or during self refresh mode. Refer to the Input Clock Frequency Change section for more details.

The maximum clock frequency for DLL-off mode is specified by the parameter ^{t}CKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, ^{t}REFI.

Due to latency counter and timing restrictions, only one CL value and CWL value (in MR0 and MR2 respectively) are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

DLL-off mode will affect the read data clock-to-data strobe relationship (^{t}DQSCK), but not the data strobe-to-data relationship (^{t}DQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

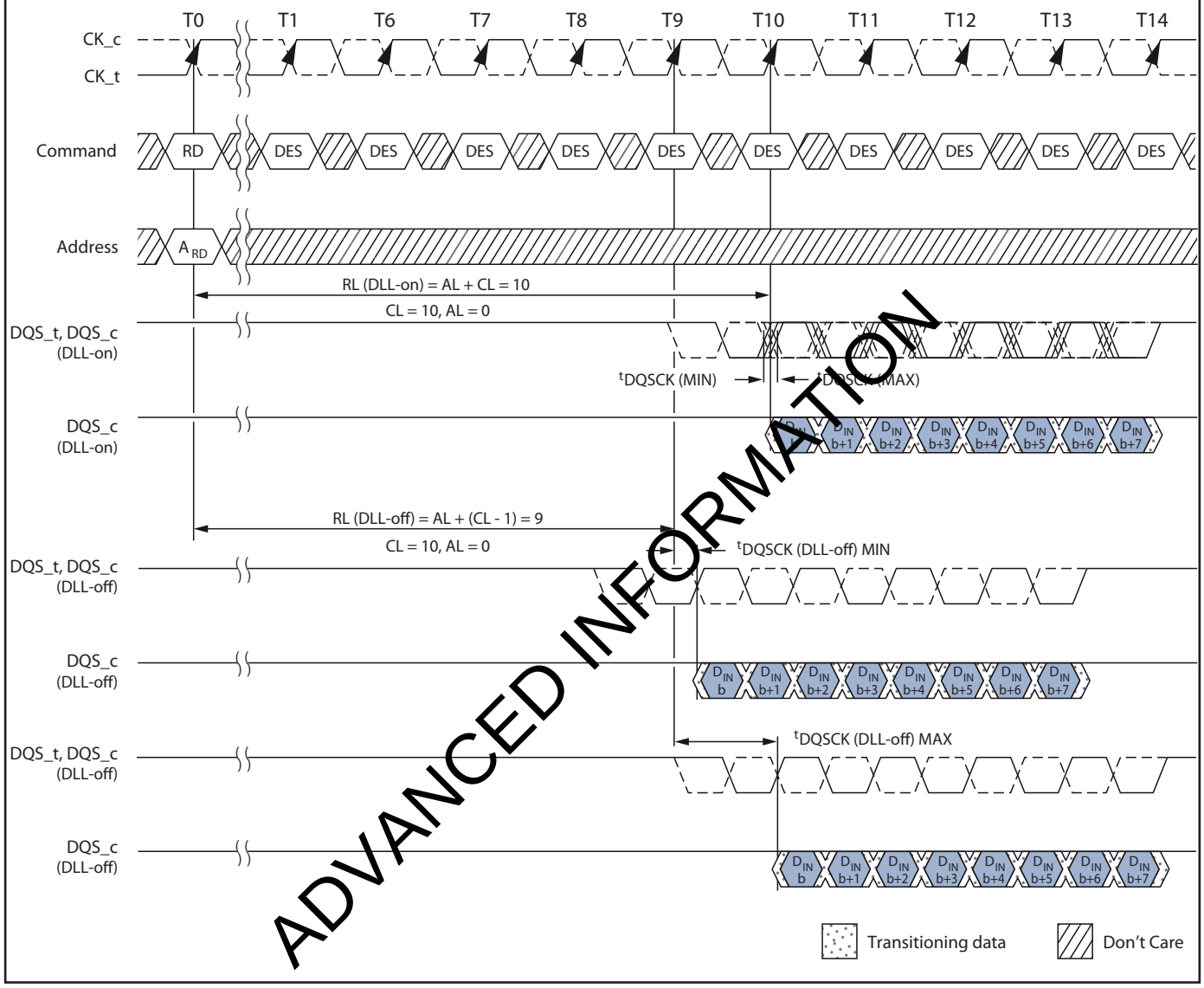
Compared with DLL-on mode, where ^{t}DQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode ^{t}DQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that ^{t}DQSCK may not be small compared to ^{t}CK (it might even be larger than ^{t}CK), and the difference between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX) is significantly larger than in DLL-on mode. The ^{t}DQSCK (DLL-off) values are vendor-specific.

The timing relations on DLL-off mode READ operation are shown in the following diagram, where CL = 10, AL = 0, and BL = 8.

The DLL-off mode is entered by setting MR1 bit A0 to 1; this will disable the DLL for subsequent operations until the A0 bit is set back to 0.

DLL-Off Mode

Figure 54: DLL-Off Mode Read Timing Operation



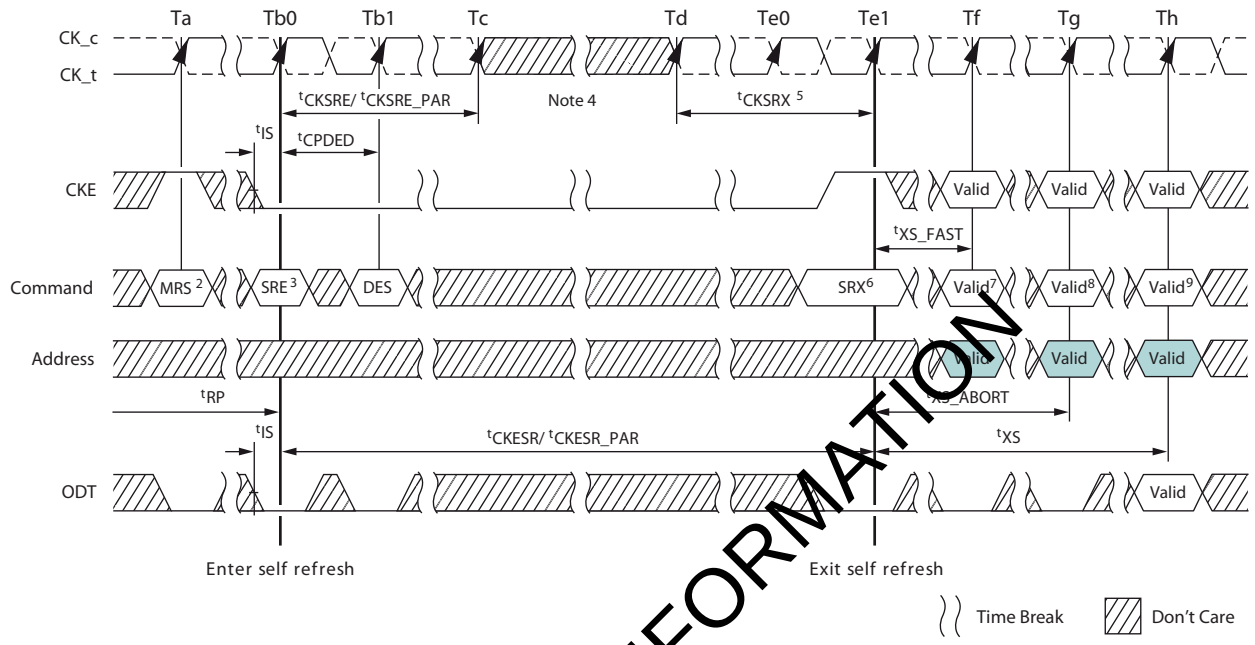
DDL Switch Sequence from DLL-On to DLL-Off

To switch from DLL-on to DLL-off requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and, to disable the DLL, the DRAM on-die termination resistors, $R_{TT(NOM)}$, must be in High-Z before MRS to MR1.)
2. Set MR1 bit A0 to 1 to disable the DLL.
3. Wait ^{t}MOD.
4. Enter self refresh mode; wait until ^{t}CKSRE/^{t}CKSRE_PAR is satisfied.
5. Change frequency, following the guidelines in the Input Clock Frequency Change section.
6. Wait until a stable clock is available for at least ^{t}CKSRX at device inputs.
7. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until all ^{t}MOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all ^{t}MOD timings from any MRS command are satisfied. If $R_{TT(NOM)}$ was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait ^{t}XS_FAST, ^{t}XS_ABORT, or ^{t}XS, and then set mode registers with appropriate values (an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after ^{t}XS_FAST).
   - ^{t}XS_FAST: ZQCL, ZQCS, and MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and gear-down mode in MR3 may be accessed provided the device is not in per-DRAM addressability mode. Access to other device mode registers must satisfy ^{t}XS timing.
   - ^{t}XS_ABORT: If the bit is enabled, then the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of ^{t}XS_ABORT. Upon exiting from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same regardless of the MRS bit setting for self refresh abort.
   - ^{t}XS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, and RDAS8.
9. Wait ^{t}MOD to complete.

The device is ready for the next command.

FIGURE 55: DLL SWITCH SEQUENCE FROM DLL-ON TO DLL- OFF



Notes:
1. Starting in the idle state: RTT in stable state.
2. Disable DLL by setting MR1 bit A0 to 0.
3. Enter SR.
4. Change frequency.
5. Clock must be stable tCKSRX.
6. Exit SR.
7. Update mode registers allowed with DLL-off settings met.

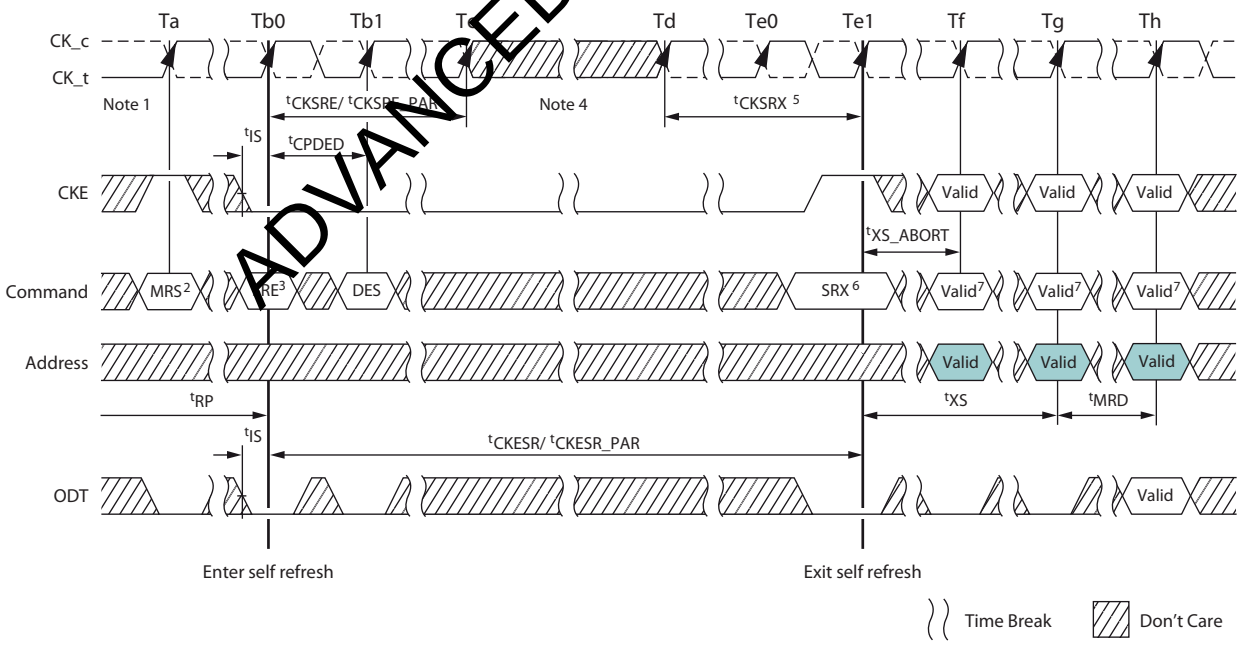
DDL-Off to DLL-On Procedure

To switch from DLL-off to DLL-on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM ODT resistors ($R_{TT(NOM)}$) must be in High-Z before self refresh mode is entered.)
2. Enter self refresh mode; wait until ^{t}CKSRE/^{t}CKSRE_PAR are satisfied.
3. Change frequency (following the guidelines in the Input Clock Frequency Change section).
4. Wait until a stable clock is available for at least ^{t}CKSRX at device inputs.
5. Starting with the SELF REFRESH EXIT command, CKE must continuously be registered HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW or HIGH until ^{t}DLLK timing from the subsequent DLL RESET command is satisfied. If $R_{TT(NOM)}$ disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait ^{t}XS or ^{t}XS_ABORT, depending on bit x in RMy, then set MR1 bit A0 to 0 to enable the DLL.
7. Wait ^{t}MRD, then set MR1 bit A8 to 1 to start DLL reset.
8. Wait ^{t}MRD, then set mode registers with appropriate values; an update of CL, CWL, and WR may be necessary. After ^{t}MOD is satisfied from any proceeding MRS command, a ZQCL command can also be issued during or after tDLLK.
9. Wait for ^{t}MOD to complete. Remember to wait ^{t}DLLK after DLL RESET before applying any command requiring a locked DLL. In addition, wait for ^{t}ZQoper in case a ZQCL command was issued.

The device is ready for the next command.

Figure 56: DLL Switch Sequence from DLL-Off to DLL-On



Notes: 1. Starting in the idle state.
2. Enter SR

3. Change frequency.
4. Clock must be stable ^{t}CKSRX.
5. Exit SR.
6. Set DLL to on by setting MR1 to A0 = 0.
7. Update mode registers.
8. Issue any valid command.

Input Clock Frequency Change

After the device is initialized, it requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed by the clock jitter and spread spectrum clocking (SSC) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequen-cy.

After the device has been successfully placed in self refresh mode and ^{t}CKSRE/^{t}CKSRE_PAR have been satisfied, the state of the clock becomes a “Don’t Care.” Following a “Don’t Care,” changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in SELF REFRESH Operation.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, and MR6 may need to be issued to program appropriate CL, CWL, gear-down mode, READ and WRITE preamble, and ^{t}CCD_L/^{t}DLLK values. If MR6 is issued prior to self refresh entry for new the ^{t}DLLK value, DLL will relock automatically at self refresh exit. However, if MR6 is issued after self refresh entry, MR0 must be issued to reset the DLL.

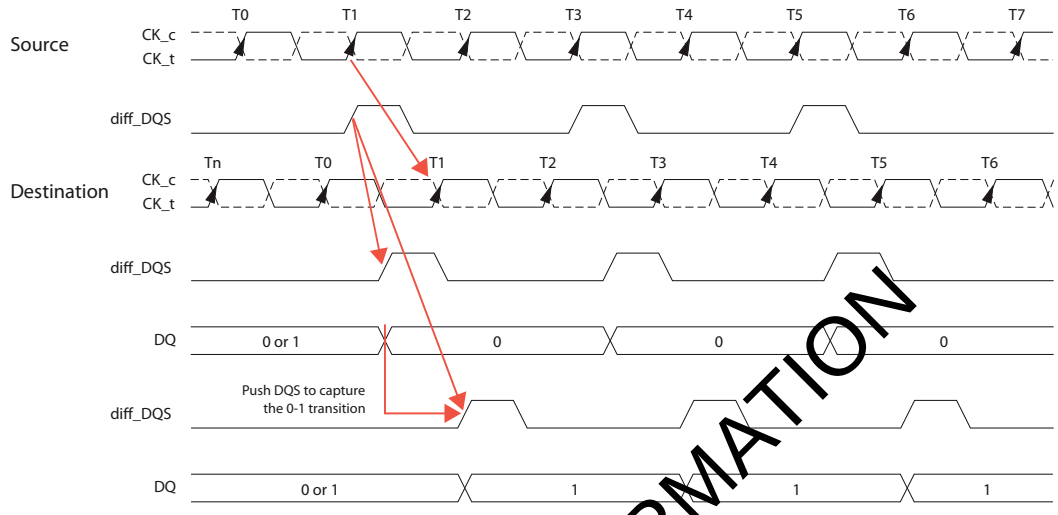
The device input clock frequency can change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL-on mode to DLL- off mode transition sequence (see DLL-On/Off Switching Procedures).

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain ^{t}DQSS, ^{t}DSS, and ^{t}DSH specifications. Therefore, the device supports a write-leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the ^{t}DQSS, tDSS, and tDSH specifications.

The memory controller can use the write-leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the tDQSS specification. Besides ^{t}DQSS, ^{t}DSS and ^{t}DSH specifications also need to be fulfilled. One way to achieve this is to combine the actual ^{t}DQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual ^{t}DQSS in the application, the actual values for ^{t}DQSL and ^{t}DQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy tDSS and ^{t}DSH specifications. A conceptual timing of this scheme is shown below.

Write Leveling

FIGURE 57: WRITE-LEVELING CONCEPT, EXAMPLE 1

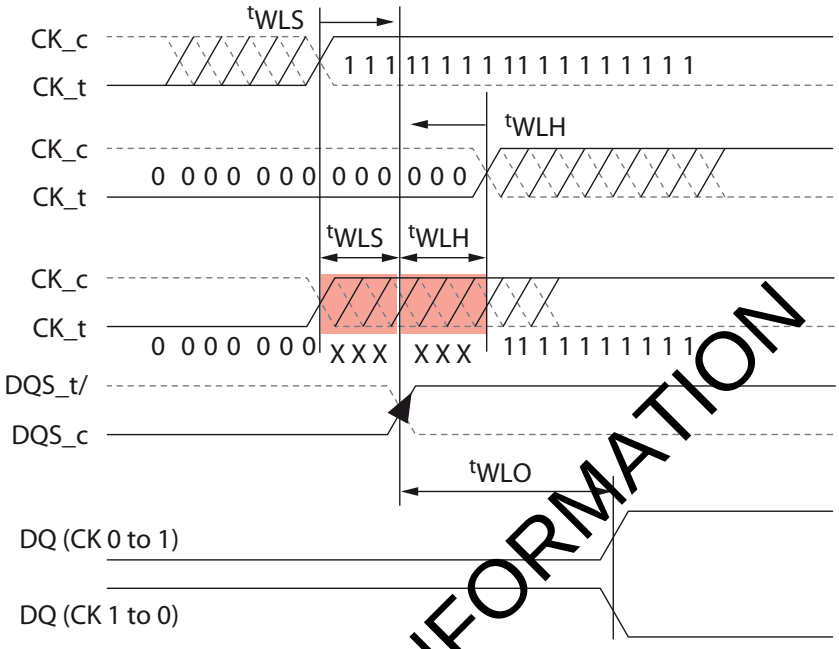


DQS driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations. All byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane.

The figure below is another representative way to view the write-leveling procedure. Although it shows the clock varying to a static strobe, this is for illustrative purpose only; the clock does not actually change phase, the strobe is what actually varies. By issuing multiple WL bursts, the DQS strobe can be varied to capture with fair accuracy the time at which the clock edge arrives at the DRAM clock input buffer.

FIGURE 58: WRITE-LEVELING CONCEPT, EXAMPLE 2



DRAM Setting for Write Leveling and DRAM TERMINATION Function in that Mode

The DRAM enters into write-leveling mode if A7 in MR1 is HIGH. When leveling is finished, the DRAM exits write-leveling mode if A7 in MR1 is LOW (see the MR Leveling Procedures table). Note that in write-leveling mode, only DQS terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM DRAM TERMINATION Function in Leveling Mode table).

TABLE 101: MR SETTINGS FOR LEVELING PROCEDURES

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Q off)	A12	0	1

TABLE 102: DRAM TERMINATION FUNCTION IN LEVELING MODE

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination
$R_{TT(NOM)}$ with ODT HIGH	On	Off

Table 102: DRAM TERMINATION Function in Leveling Mode (continued)

ODT Pin at DRAM	DQS_t/DQS_c Termination	DQ Termination
$R_{TT(Park)}$ with ODT LOW	On	Off

Notes:
1. In write-leveling mode, with the mode's output buffer either disabled (MR1[bit7] = 1 and MR1[bit12] = 1) or with its output buffer enabled (MR1[bit7] = 1 and MR1[bit12] = 0), all $R_{TT(NOM)}$ and $R_{TT(Park)}$ settings are supported.
2. $R_{TT(WR)}$ is not allowed in write-leveling mode and must be set to disable prior to entering write-leveling mode.

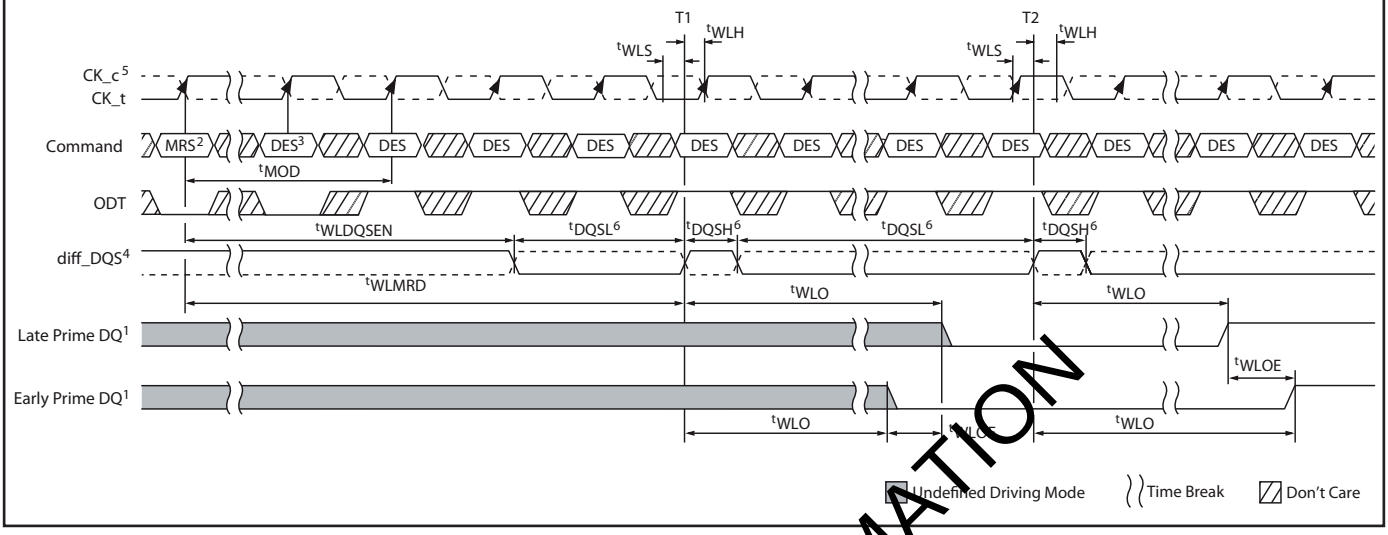
Procedure Description

The memory controller initiates the leveling mode of all DRAM by setting bit 7 of MR1 to 1. When entering write-leveling mode, the DQ pins are in undefined driving mode.
During write-leveling mode, only the DESELECT command is supported, other than MRS commands to change the Qoff bit (MR1[A12]) and to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change the MR1 bits of TBD. Because the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT
signal.

The controller may drive DQS_t LOW and DQS_c HIGH after a delay of tWLDQSEN, at which time the DRAM has applied ODT to these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge, which is used by the DRAM to sample CK driven from the controller. tWLMRD (MAX) timing is controller dependent.

The DRAM samples CK status with the rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit.
There are no read strobes (DQS_t, DQS_c) needed for these DQs. The controller sam-ples incoming DQ and either increments or decrements DQS delay setting and launch-es the next DQS pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write-leveling procedure.

Figure 59: Write-Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2)



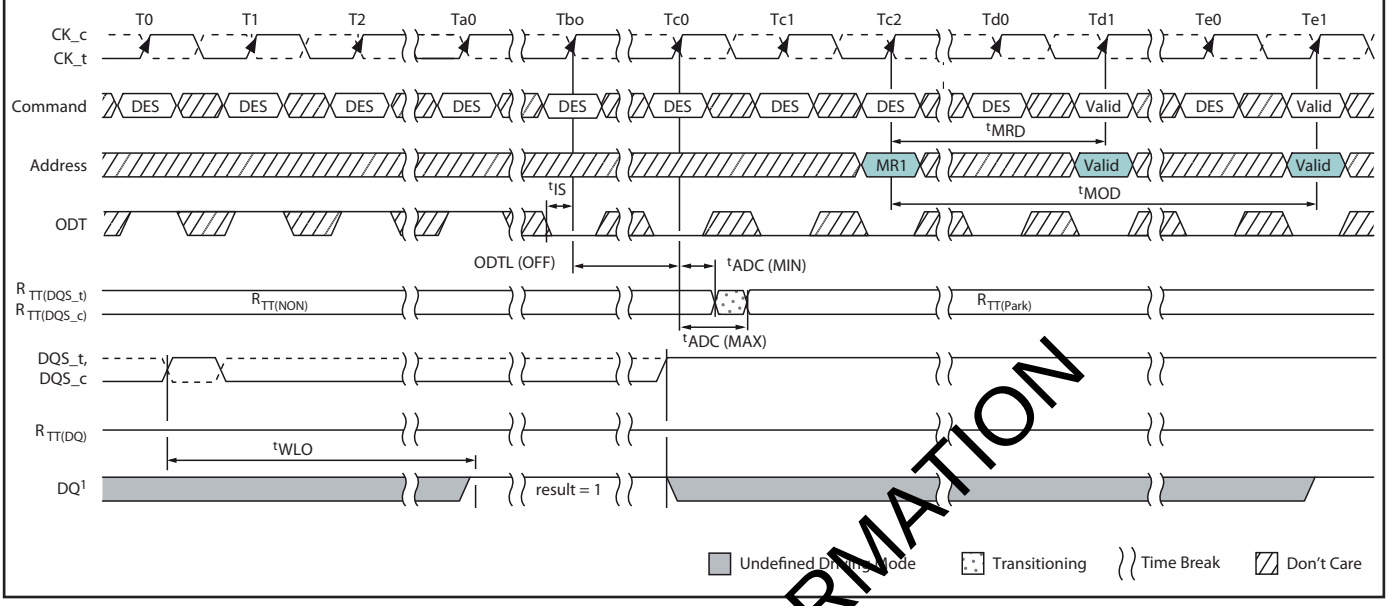
Notes:
1. The device drives leveling feedback on all DQs.
2. MRS: Load MR1 to enter write-leveling mode.
3. diff_DQS is the differential data strobe. Timing reference points are the zero crossings. DQS_t is shown with a solid line; DQS_c is shown with a dotted line.
4. CK_t is shown with a solid dark line; CK_c is shown with a dotted line.
5. DQS needs to fulfill minimum pulse width requirements, tDQSH (MIN) and tDQSL (MIN), as defined for regular WRITEs; the maximum pulse width is system dependent.
6. tWLDQSEN must be satisfied following equation when using ODT:
   - DLL = Enable, then tWLDQSEN > tMOD (MIN) + ODTLon + tADC
   - DLL = Disable, then tWLDQSEN > tMOD (MIN) + tAONAS

Write-Leveling Mode Exit

Write-leveling mode should be exited as follows:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After R_{TT} is switched off, disable write-leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after tMRD [Td1]).

Figure 60: Write-Leveling Exit

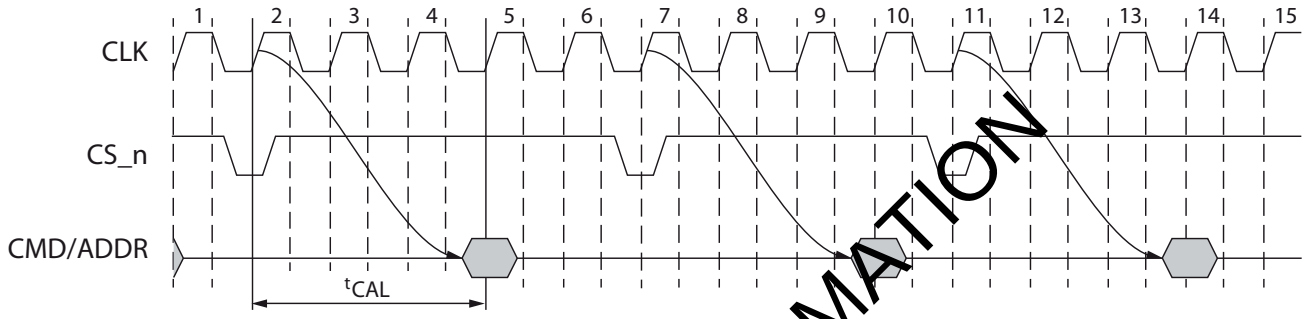


Notes:
1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS signals capturing CK_t HIGH just after the T0 state.
2. See previous figure for specific tWLO timing.

Command Address Latency

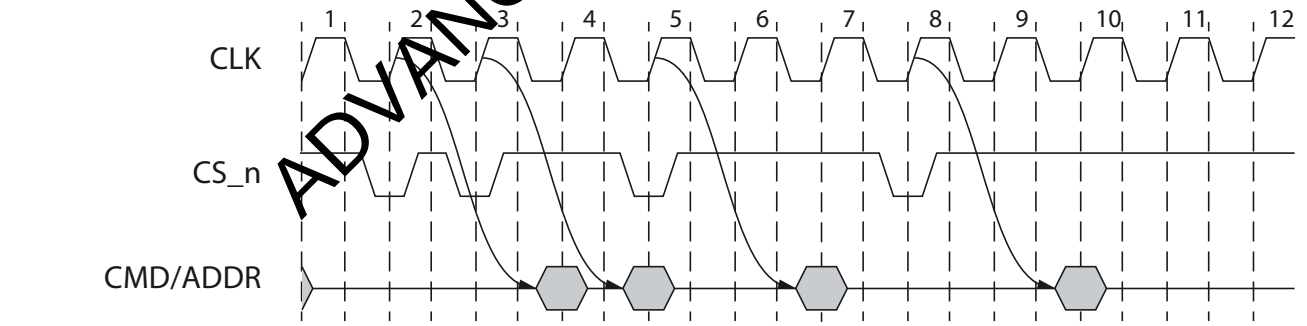
DDR4 supports the command address latency (CAL) function as a power savings feature. This feature can be enabled or disabled via the MRS setting. CAL timing is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL in clocks must be programmed into the mode register (see MR1 Register Definition table) and is based on the equation ^{t}CK(ns)/ ^{t}CAL(ns), rounded up in clocks.

FIGURE 61: CAL TIMING DEFINITION



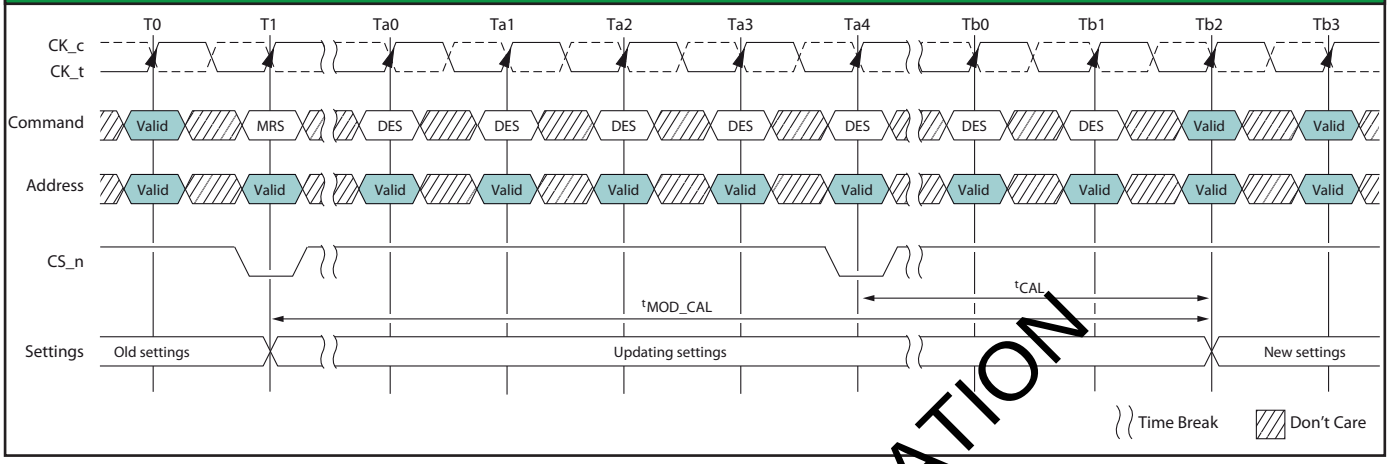
CAL gives the DRAM time to enable the command and address receivers before a command is issued. After the command and the address are latched, the receivers can be disabled if CS_n returns to HIGH. For consecutive commands, the DRAM will keep the command and address input receivers enabled for the duration of the command se-quence.

FIGURE 62: CAL TIMING EXAMPLE (CONSECUTIVE CS_N = LOW)



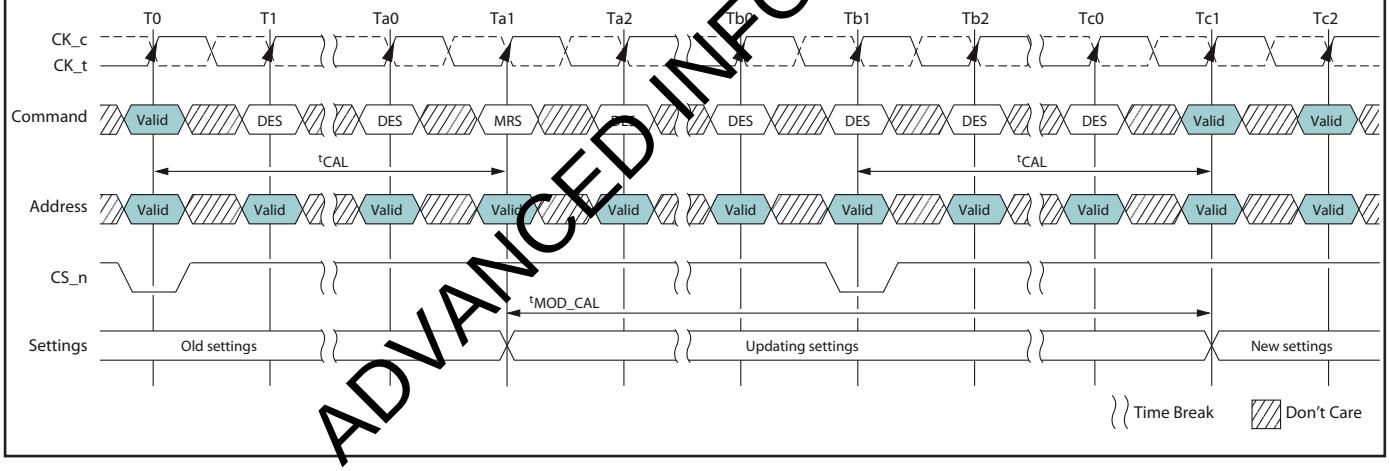
When the CAL mode is enabled, additional time is required for the MRS command to complete. The earliest the next valid command can be issued is ^{t}MOD_CAL, which should be equal to ^{t}MOD + ^{t}CAL. The two following figures are examples.

FIGURE 63: CAL ENABLE TIMING - TMOD_CAL



Note: 1. CAL mode is enabled at T1.

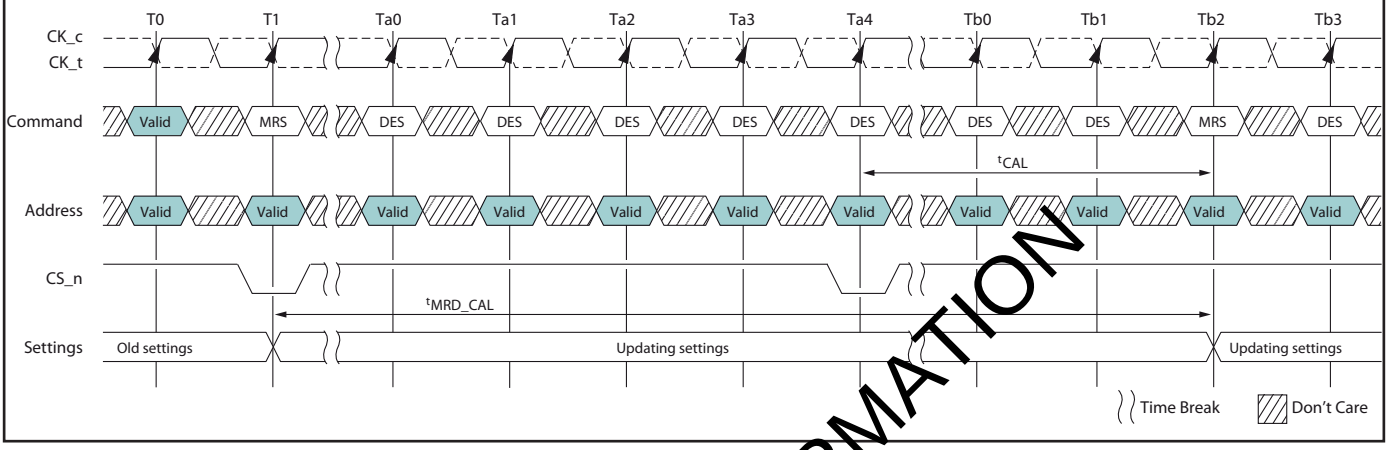
FIGURE 64: TMOD_CAL, MRS TO VALID COMMAND TIMING WITH CAL ENABLED



Note: 1. MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting if modified.

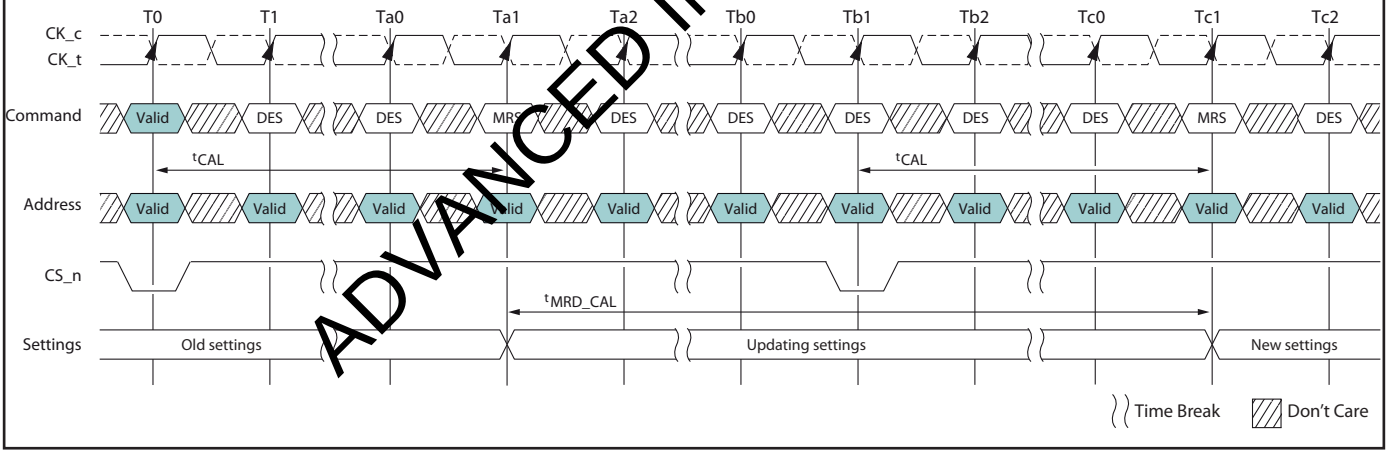
When the CAL mode is enabled or being enabled, the earliest the next MRS command can be issued is ^{t}MRD_CAL is equal to ^{t}MOD + ^{t}CAL. The two following figures are examples.

FIGURE 65: CAL ENABLE MRS TO NEXT MRS COMMAND, ^{T}MRD_CAL



Notes: 1. Command address latency mode is enabled at T1.

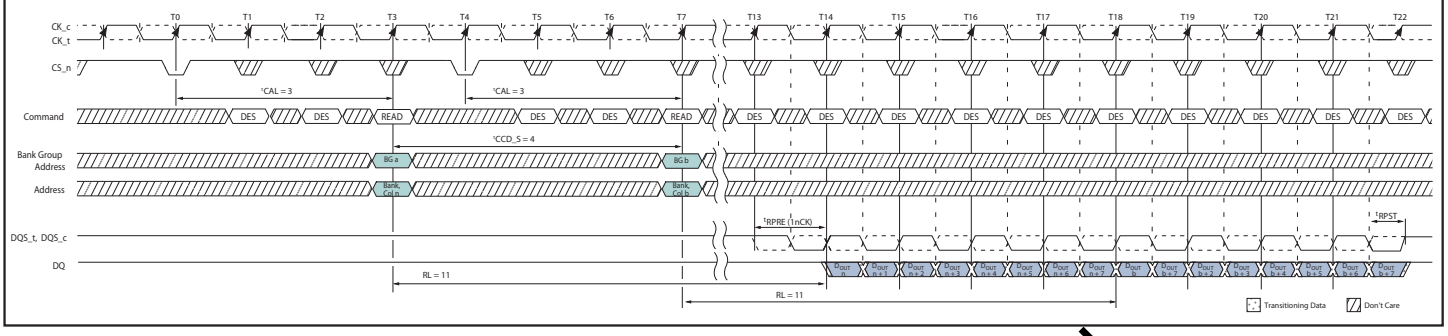
FIGURE 66: ^{T}MRD_CAL, MODE REGISTER CYCLE TIME CAL ENABLED



Notes: 1. MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting if modified.

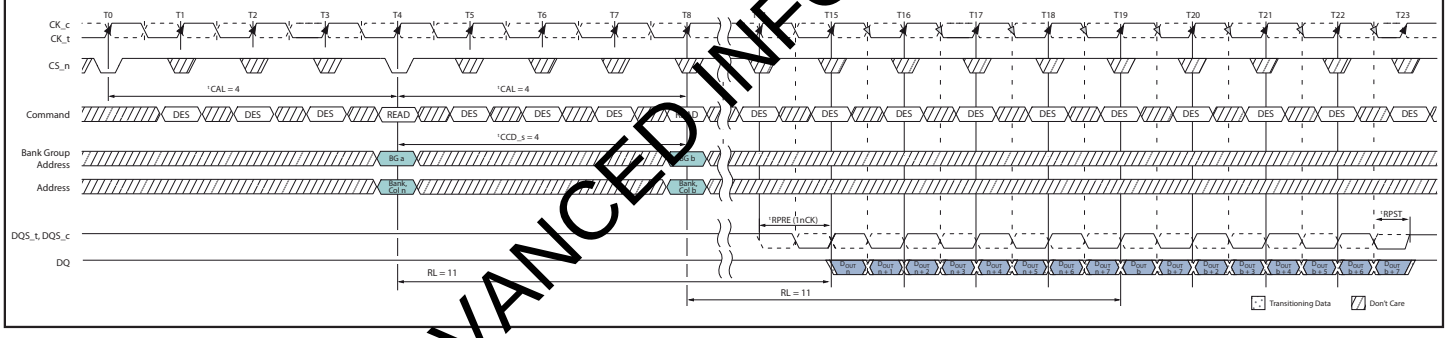
CAL Examples: Consecutive READ BL8 with two different CALs and 1tCK preamble in different bank group shown in the following figures.

FIGURE 67: CONSECUTIVE READ BL8, CAL3, 1TCK PREAMBLE, DIFFERENT BANK GROUP



Notes:
1. BL = 8, AL = 0, CL = 11, CAL = 3, Preamble = 1tCK.
2. DOUT n = data-out from column n; DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T3 and T7.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

FIGURE 68: CONSECUTIVE READ BL8, CAL4, 1TCK PREAMBLE, DIFFERENT BANK GROUP



Notes:
1. BL = 8, AL = 0, CL = 11, CAL = 4, Preamble = 1tCK.
2. DOUT n = data-out from column n; DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration, other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T4 and T8.
5. CA parity = Disable, CS to CA latency = Enable, Read DBI = Disable.
6. Enabling CAL mode does not impact ODT control timings. ODT control timings should be maintained with the same timing relationship relative to the command/address bus as when CAL is disabled.

Low-Power Auto Self Refresh Mode

An auto self refresh mode is provided for application ease. Auto self refresh mode is enabled by setting MR2[6] = 1 and MR2[7] = 1. The device will manage self refresh entry
over the supported temperature range of the DRAM. In this mode, the device will change its self refresh rate as the DRAM operating temperature changes, going lower at low temperatures and higher at high temperatures.

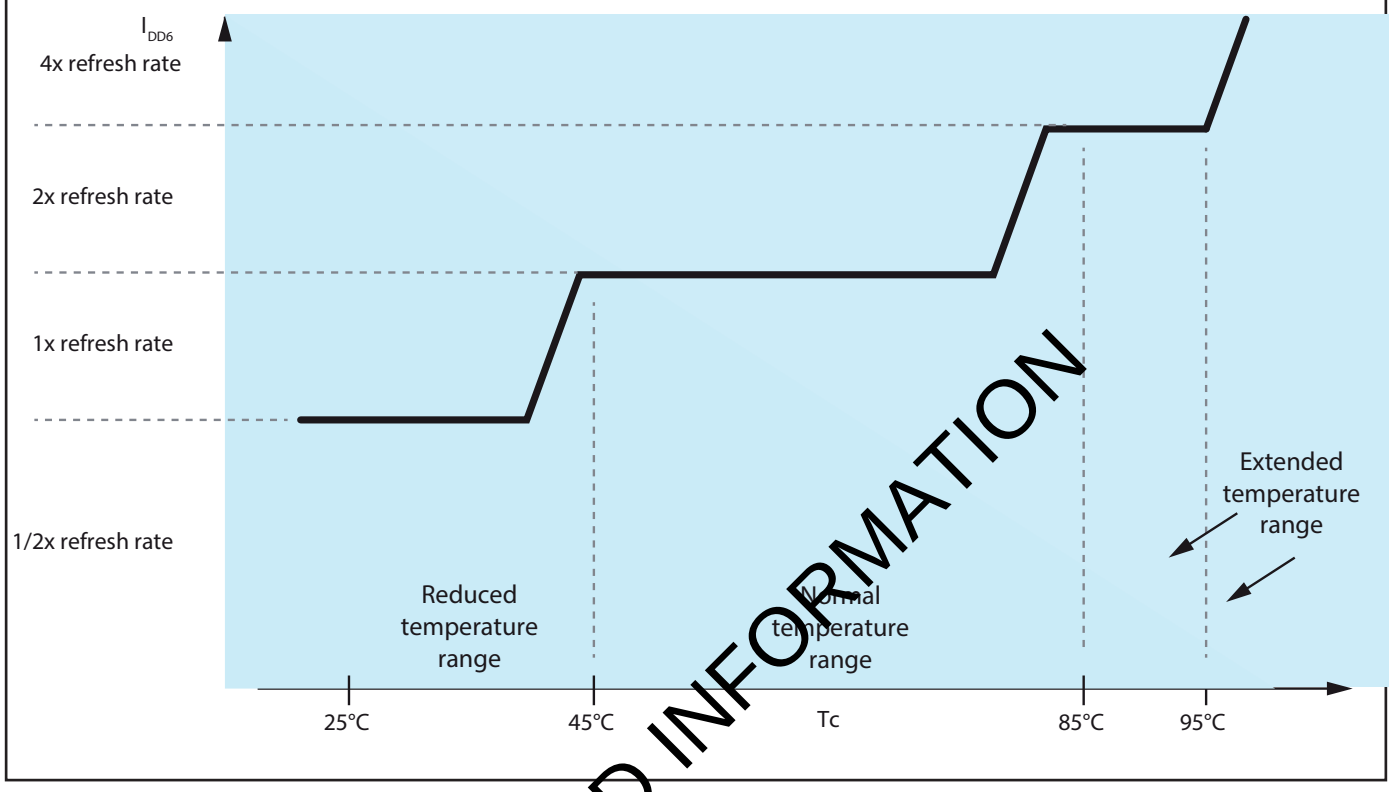
Manual Self Refresh Mode

If auto self refresh mode is not enabled, the low-power auto self refresh mode register must be manually programmed to one of the three self refresh operating modes. This mode provides the flexibility to select a fixed self refresh operating mode at the entry of the self refresh, according to the system memory temperature conditions. The user is responsible for maintaining the required memory temperature condition for the mode selected during the SELF REFRESH operation. The user may change the selected mode after exiting self refresh and before entering the next self refresh. If the temperature condition is exceeded for the mode selected, there is a risk to data retention resulting in loss of data.

Table 103: Auto Self Refresh Mode

MR2[7]	MR2[6]	Low-Power Auto Self Refresh Mode	SELF REFRESH Operation	Operating Temperature Range for Self Refresh Mode (DRAM T_{CASE})
0	0	Normal	Fixed normal self refresh rate maintains data retention at the normal operating temperature. User is required to ensure that 85°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	0°C to 85°C
1	1	Extended temperature	Fixed high self refresh rate optimizes data retention to support the extended temperature range.	0°C to 95°C
0	1	Reduced temperature	Variable or fixed self refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM T_{CASE} (MAX) is not exceeded to avoid any risk of data loss.	0°C to 45°C
1	1	Auto self refresh	Auto self refresh mode enabled. Self refresh power consumption and data retention are optimized for any given operating temperature condition.	All of the above

FIGURE 69: AUTO SELF REFRESH RANGES



Multipurpose Register

The MULTIPURPOSE REGISTER (MPR) function, MPR access mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical pages, MPR Page 0 through MPR Page 3, with each page having four 8-bit registers, MPR0 through MPR3. Page 0 can be read by any of three readout modes (serial, parallel, or staggered) while Pages 1, 2, and 3 can be read by only the serial readout mode. Page 3 is for DRAM vendor use only. MPR mode enable and page selection is done with MRS commands.Data bus inversion (DBI) is not allowed during MPR READ operation.

Once the MPR access mode is enabled (MR3[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF, and RESET; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. Power-down mode and SELF REFRESH command are not allowed during MPR enable node. No other command can be issued within tRFC after a REF command has been issued; 1x refresh (only) is to be used during MPR access mode. While in MPR access mode, MPR read or write sequences must be completed prior to a REFRESH command.

FIGURE 70: MPR BLOCK DIAGRAM

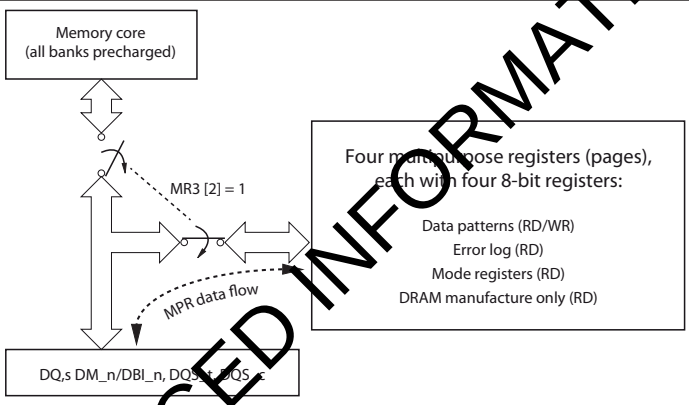


TABLE 104: MR3 SETTING FOR THE MPR ACCESS MODE

Address	Operation Mode	Description
A[12:11]	MPR data read format	00 = Serial ..... 01 = Parallel 10 = Staggered .... 11 = Reserved
A2	MPR access	0 = Standard operation (MPR not enabled) 1 = MPR data flow enabled
A[1:0]	MPR page selection	00 = Page 0 .... 01 = Page 1 10 = Page 2 .... 11 = Page 3

TABLE 105: DRAM ADDRESS TO MPR UI TRANSLATION

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – A*x*	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UI*x*	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

Table 106: MPR Page and MPRx Definitions

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
MPR Page 0 – Read or Write (Data Patterns)										
BA[1:0]	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value listed)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	
MPR Page 1 – Read-only (Error Log)										
BA[1:0]	00 = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	Read-only
	01 = MPR1	CAS_n/A15	WE_n/A14	A13	A12	A11	A10	A9	A8	
	10 = MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/A16	
	11 = MPR3	CRC error status	CA parity error status	CA parity latency: [5] = MR5[2], [4] = MR5[1], [3] = MR5[0]			C2	C1	C0	
MPR Page 2 – Read-only (MRS Readout)										
BA[1:0]	00 = MPR0	PPR support	sPPR support	$R_{TT(WR)}$	Temperature sensor status[2]		CRC write enable	$R_{TT(WR)}$		Read-only
	01 = MPR1	V_{REFDQ} trainging range	V_{REFDQ} training value: [6:1] = MR6[5:0]						Gear-down enable	
		CAS latency: [7:3] = MR0[12,6,4,2] 10 = MPR2					CAS write latency [2:0] = MR2[5:3]			
	11 = MPR3	$R_{TT(NOM)}$: [11:9] = MR1[10:8]		$R_{TT(Park)}$: [4:2] = MR5[8:6]				R_{ON}: [1:0] = MR2[2:1]		
MPR Page 3 – Read-only (Restricted, except for MPR3 [3:0])										
BA[1:0]	00 = MPR0	DC	DC	DC	DC	DC	DC	DC	DC	Read-only
	01 = MPR1	DC	DC	DC	DC	DC	DC	DC	DC	
	10 = MPR2	DC	DC	DC	DC	DC	DC	DC	DC	
	11 = MPR3	DC	DC	DC	DC	MAC	MAC	MAC	MAC	

Notes: 1. DC = "Don't Care"
2. MPR[4:3] 00 = Sub 1X refresh; MPR[4:3] 01 = 1X refresh; MPR[4:3] 10 = 2X refresh; MPR[4:3] 11 = Reserved

MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR READ operation; the device will ignore the Read DBI enable setting in MR5 [12] when in MPR mode. READ commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values, which are de-fined in Table 29. MPR page 0 can be rewritten via an MPR WRITE command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between READ commands; tCCD_L must be used for timing between READ commands

The following steps are required to use the MPR to read out the contents of a mode reg-ister (MPR Page x, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR read format, and MR3[1:0] MPR page.
    a. MR3[12:11] MPR read format:
        1. 00 = Serial read format
        2. 01 = Parallel read format
        3. 10 = staggered read format
        4. 11 = RFU
    b. MR3[1:0] MPR page:
        1. 00 = MPR Page 0
        2. 01 = MPR Page 1
        3. 10 = MPR Page 2
        4. 11 = MPR Page 3
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPRx location.
6. Issue RD or RDA command.
    a. BA1 and BA0 indicate MPRx location:
        1. 00 = MPR0
        2. 01 = MPR1
        3. 10 = MPR2
        4. 11 = MPR3
    b. A12/BC = 0 or 1; BL8 or BC4 fixed only, BC4 OTF not supported.
        1. If BL = 8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR READ commands.
    c. A2 = burst-type dependant:
        1. BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
        2. BL8: A2 = 1 not allowed
        3. BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
        4. BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T
    d. A[1:0] = 00, data burst is fixed nibble start at 00.
    e. Remaining address inputs, including A10, and BG1 and BG0 are “Don’t Care.”
7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3[A12,11,1,0].
8. Steps 5 through 7 may be repeated to read additional MPRx locations.
9. After the last MPRx READ burst, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. After the tMOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR Readout Format

The MPR read data format can be set to three different settings: serial, parallel, and staggered.

MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MRx, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).

Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

Table 107: MPR Readout Serial Format

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
x4 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
x8 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
x16 Device								
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1

Table 107: MPR Readout Serial Format (Continued)

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repea-ted in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

Table 108: MPR Readout - Parallel Format

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
x4 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
x8 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
x16 Device								
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

Table 108: MPR Readout - Parallel Format (Continued)

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations.

A read example to MPR0 is shown below.

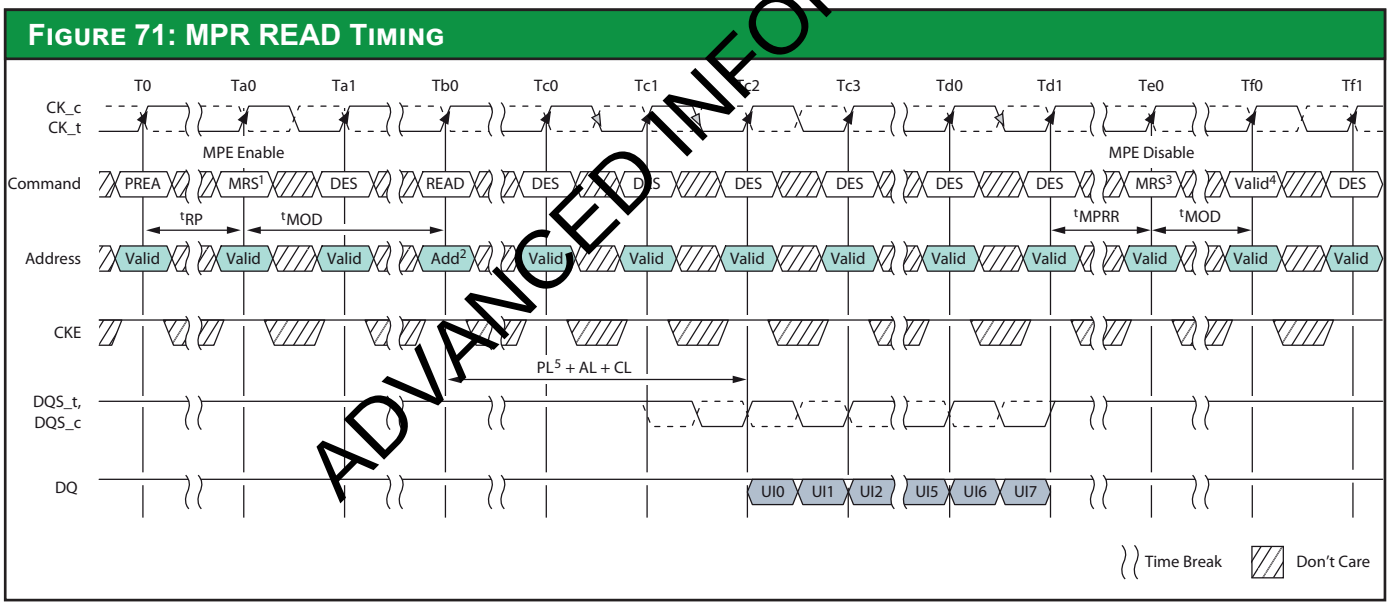
TABLE 109: MPR READOUT STAGGERED FORMAT

x8 READ MPR0 Command		x16 READ MPR0 Command		x16 READ MPR0 Command	
Stagger	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

MPR READ Waveforms

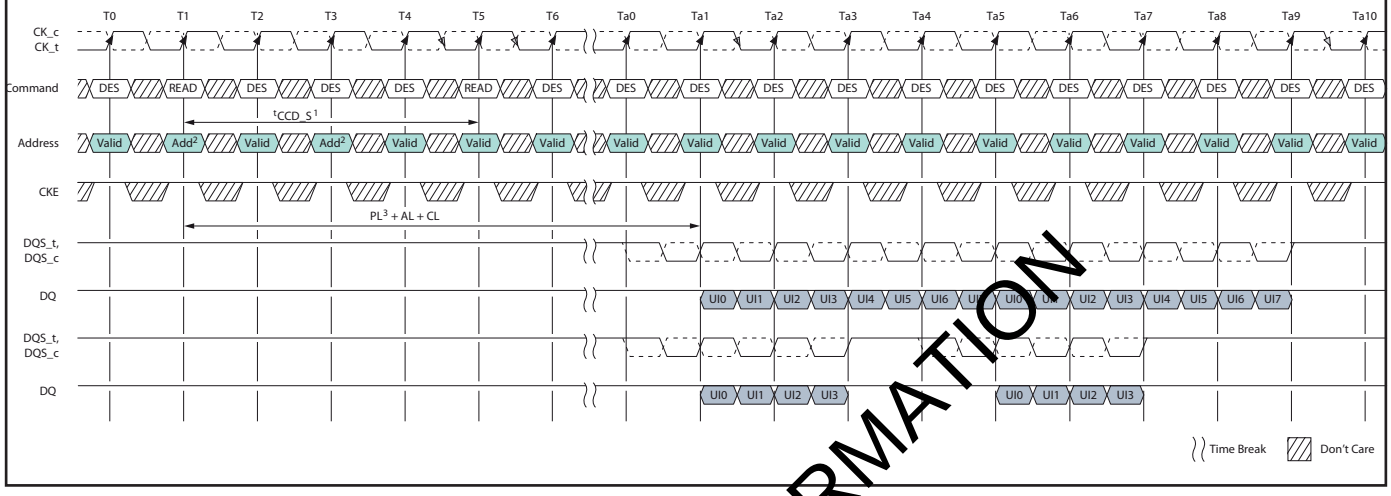
The following waveforms show MPR read accesses.

FIGURE 71: MPR READ TIMING



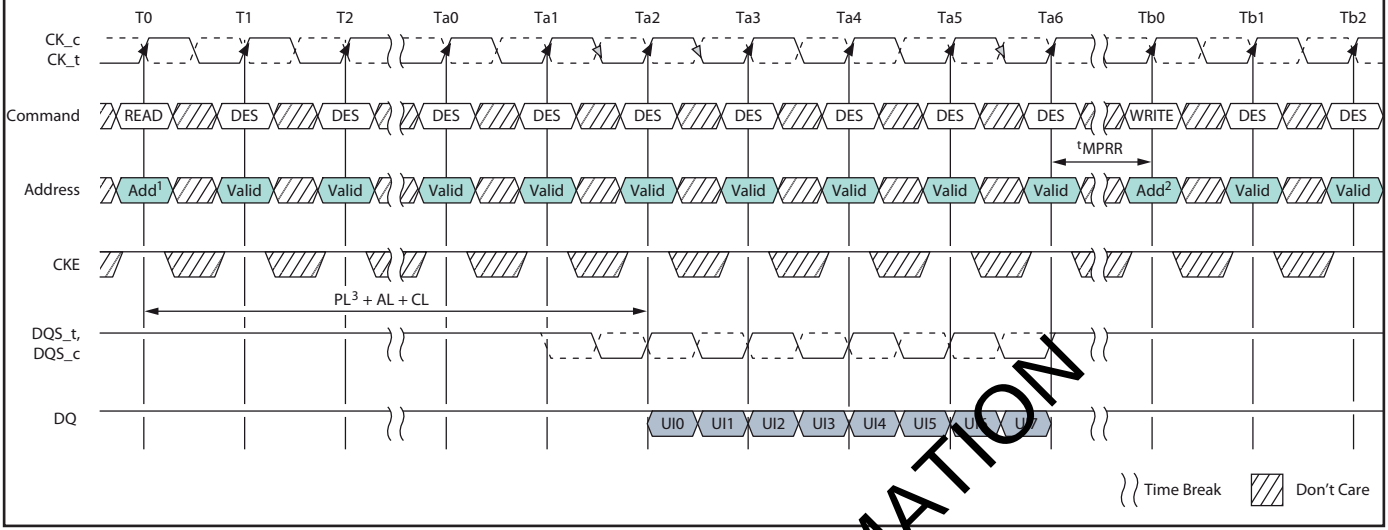
Notes:
1. ^{t}CCD_S = 4tCK, Read Preamble = 1^{t}CK.
2. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Multipurpose registers read/write disable (MR3 A2 = 0).
4. Continue with regular DRAM command.
5. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

FIGURE 72: MPR BACK-TO-BACK READ TIMING



Notes:
1. $^{t}CCD\_S = 4^{t}CK$, Read Preamble = 1 ^{t}CK.
2. 2. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order is fixed at 0, 1, 2, 3, T, T, T, T)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10 and must be 1b when MR0 A[1:0] = 01
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

FIGURE 73: MPR READ-TO-WRITE TIMING



Notes:
1. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 and must be 1b when MR0 A[1:0] = 01
2. Address setting:
   BA1 and BA0 indicate the MPR location
   A[7:0] = data for MPR
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care"
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

MPR Writes

MPR access mode allows 8-bit writes to the MPR location using the address bus A[7:0]. Data bus inversion (DBI) is not allowed during MPR WRITE operation. The DRAM will maintain the new written values unless re-initialized or there is power loss.

The following steps are required to use the MPR to write to mode register MPR Page 0, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (enable MPR data flow) and MR3[1:0] = 00 (MPR Page 0); 01, 10, and 11 are not allowed.
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent WRITE commands to specific MPRx location.
6. Issue WR or WRA command:
   a. BA1 and BA0 indicate MPRx location
      1. 00 = MPR0
      2. 01 = MPR1
      3. 10 = MPR2
      4. 11 = MPR3

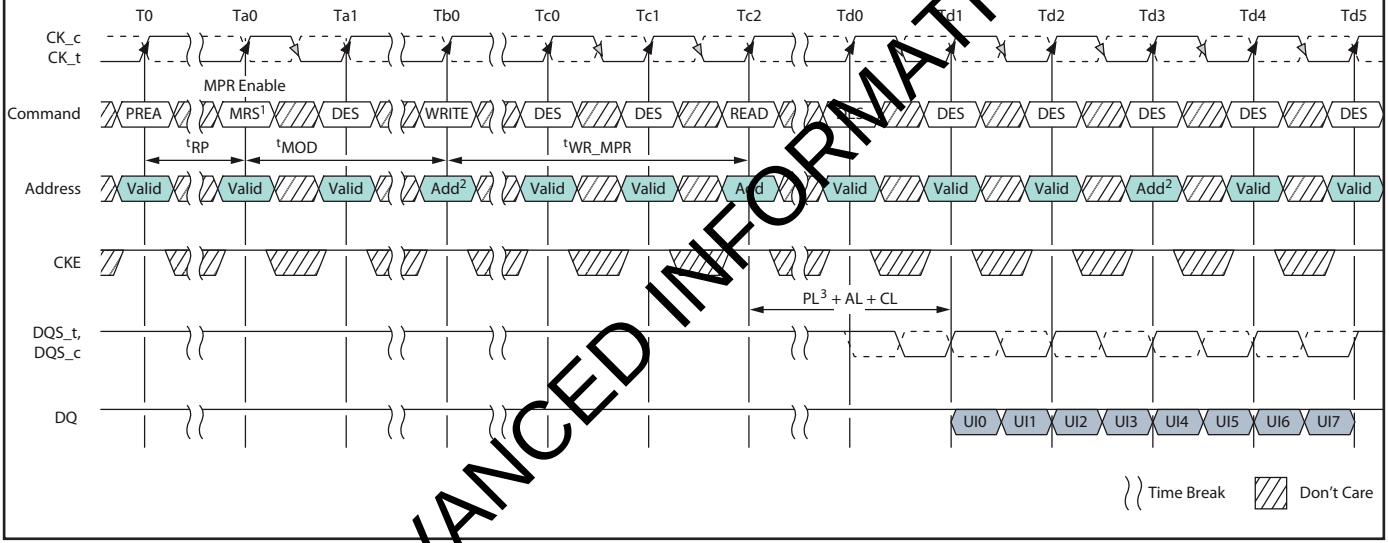
b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[7:0].
c. Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."

7. ^{t}WR_MPR must be satisfied to complete MPR WRITE.
8. Steps 5 through 7 may be repeated to write additional MPRx locations.
9. After the last MPRx WRITE, ^{t}MPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. When the ^{t}MOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR WRITES Waveforms

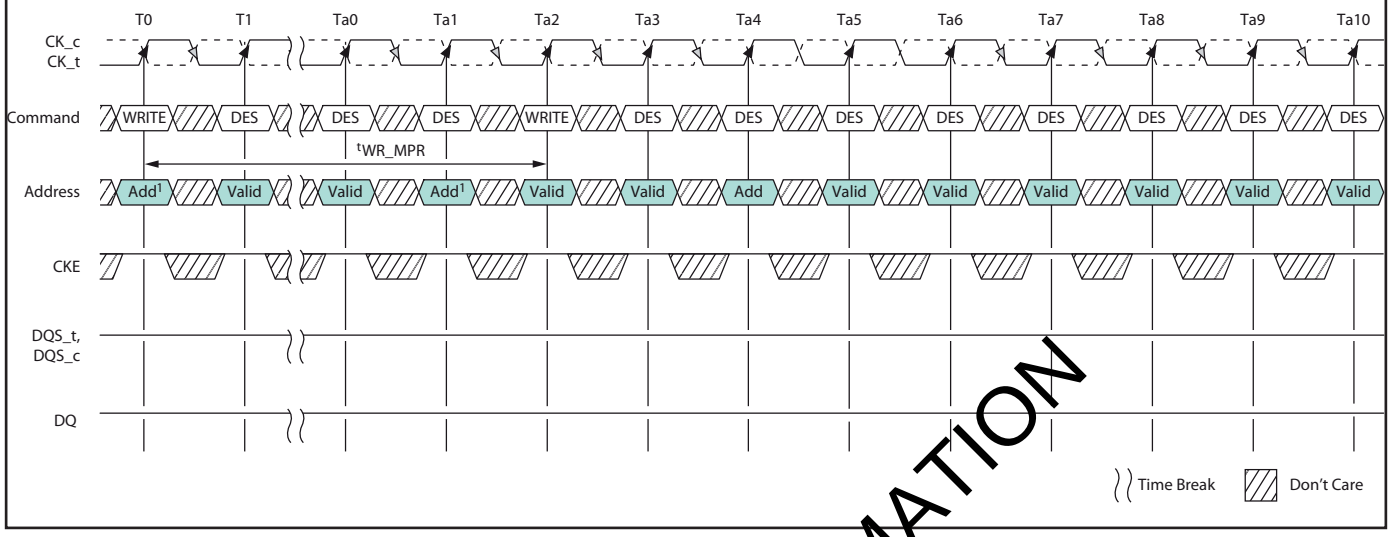
The following waveforms show MPR write accesses.

FIGURE 74: MPR WRITE AND WRITE-TO-READ TIMING



Notes:
1. Multipurpose registers read/write enable (MR3 A2 = 1).
2. Address setting:
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care"
3. Parity latency (PL) is added to data output delay when CA parity latency mode is enabled.

FIGURE 75: MPR BACK-TO-BACK TIMING

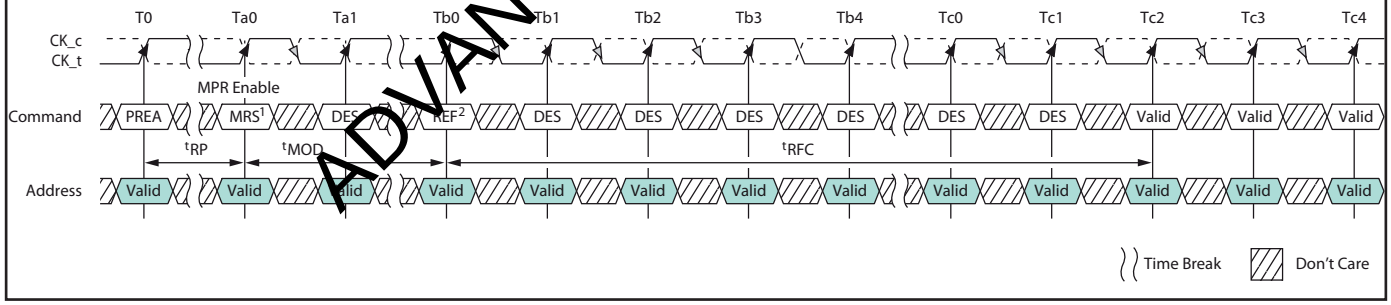


Notes: 1. Address setting:
BA1 and BA0 indicate the MPR location
A[7:0] = data for MPR
A10 and other address pins are "Don't Care"

MPR REFRESH Waveforms

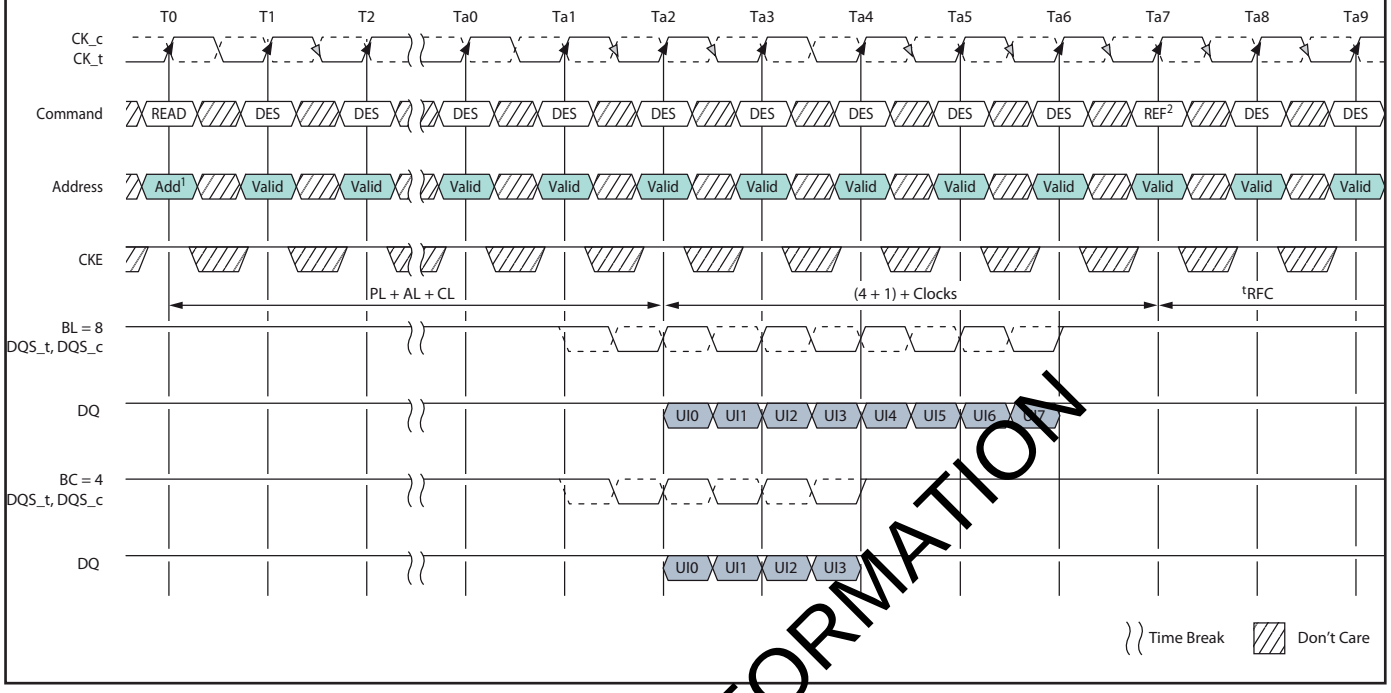
The following waveforms show MPR accesses interaction with refreshes.

FIGURE 76: REFRESH TIMING



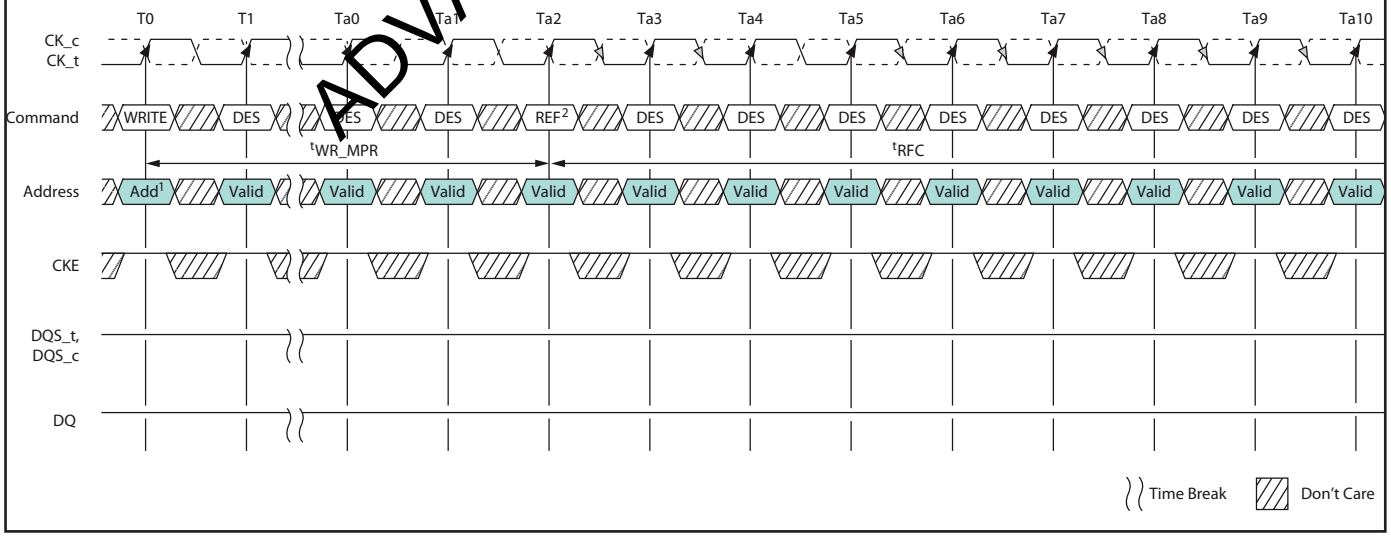
Notes: 1. Multipurpose registers read/write enable (MR3 A2 = 1). Redirect all subsequent read and writes to MPR locations.
2. 1x refresh is only allowed when MPR mode is enabled.

Figure 77: READ-to-REFRESH Timing



Notes:
1. Address setting:
   A[1:0] = 00b (data burst order is fixed starting at nibble, always 00b here)
   A2 = 0b (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   BA1 and BA0 indicate the MPR location
   A10 and other address pins are "Don't Care," including BG1 and BG0. A12 is "Don't Care" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
2. 1x refresh is only allowed when MPR mode is enabled.

Figure 78: WRITE-to-REFRESH Timing



Notes:
1. Address setting:
   BA1 and BA0 indicate the MPR location
   A[7:0] = data for MPR
   A10 and other address pins are "Don't Care"
2. 1x refresh is only allowed when MPR mode is enabled.

Gear-Down Mode

The DDR4 SDRAM defaults in 1/2 rate (1N) clock mode and uses a low-frequency MRS command (the MRS command has relaxed setup and hold) followed by a sync pulse (first CS pulse after MRS setting) to align the proper clock edge for operating the control lines CS_n, CKE, and ODT when in 1/4 rate (2N) mode. Gear-down mode is only supported at DDR4-2666 and faster. For operation in 1/2 rate mode, neither an MRS command or a sync pulse is required. Gear-down mode may only be entered during initialization or self refresh exit and may only be exited during self refresh exit. The general sequence for operation in 1/4 rate during initialization is as follows:

1. The device defaults to a 1N mode internal clock at power-up/reset.
2. Assertion of reset.
3. Assertion of CKE enables the DRAM.
4. MRS is accessed with a low-frequency N × ^{t}CK gear-down MRS command. (NtCK static MRS command is qualified by 1N CS_n.)
5. The memory controller will send a 1N sync pulse with a low-frequency N × ^{t}CK NOP command. ^{t}SYNC_GEAR is an even number of clocks. The sync pulse is on an even edge clock boundary from the MRS command.
6. Initialization sequence, including the expiration of ^{t}DLLK and ^{t}ZQinit, starts in 2N mode after ^{t}CMD_GEAR from 1N sync pulse.

The device resets to 1N gear-down mode after entering self refresh. The general sequence for operation in gear-down after self refresh exit is as follows:

1. MRS is set to 1, via MR3[3], with a low-frequency N × ^{t}CK gear-down MRS command.
   a. The N^{t}CK static MRS command is qualified by 1N CS_n which meets ^{t}XS or ^{t}XS_ABORT.
   b. Only a REFRESH command may be issued to the DRAM before the N^{t}CK static MRS command.
2. The DRAM controller sends a 1N sync pulse with a low-frequency N × ^{t}CK NOP command.
   a. ^{t}SYNC_GEAR is an even number of clocks.
   b. The sync pulse is on even edge clock boundary from the MRS command.
3. A valid command not requiring locked DLL is available in 2N mode after ^{t}CMD_GEAR from the 1N sync pulse.
   a. A valid command requiring locked DLL is available in 2N mode after tXSDLL or ^{t}DLLK from the 1N sync pulse.
4. If operation is in 1N mode after self refresh exit, N × ^{t}CK MRS command or sync pulse is not required during self refresh exit. The minimum exit delay to the first valid command is tXS, or ^{t}XS_ABORT.

The DRAM may be changed from 2N to 1N by entering self refresh mode, which will reset to 1N mode. Changing from 2N to by any other means can result in loss of data and make operation of the DRAM uncertain.

When operating in 2N gear-down mode, the following MR settings apply:

- CAS latency (MR0[6:4,2]): Even number of clocks
- Write recovery and read to precharge (MR0[11:9]): Even number of clocks
- Additive latency (MR1[4:3]): CL - 2
- CAS WRITE latency (MR2 A[5:3]): Even number of clocks
- CS to command/address latency mode (MR4[8:6]): Even number of clocks
- CA parity latency mode (MR5[2:0]): Even number of clocks

FIGURE 79: CLOCK MODE CHANGE FROM 1/2 RATE TO 1/4 RATE (INITIALIZATION)

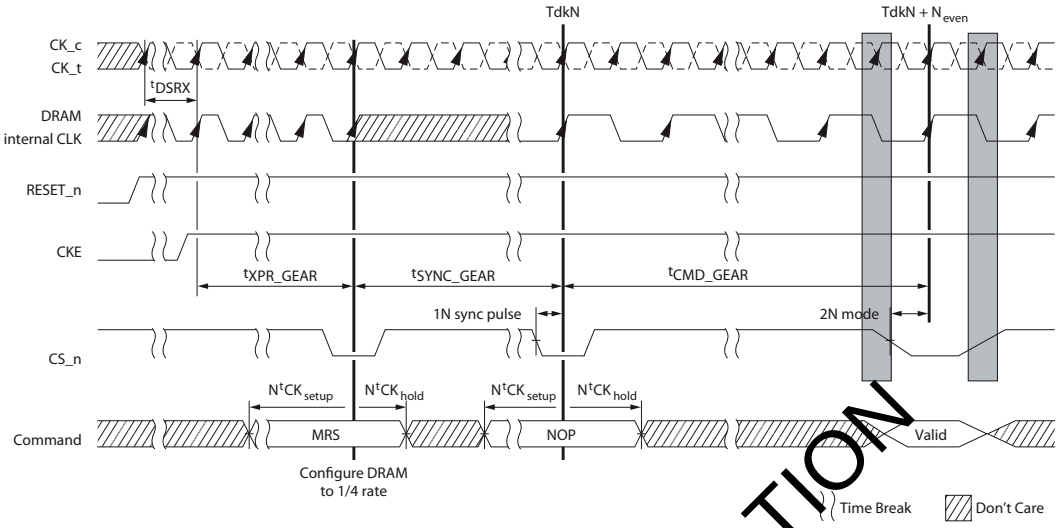


FIGURE 80: CLOCK MODE CHANGE AFTER EXITING SELF REFRESH

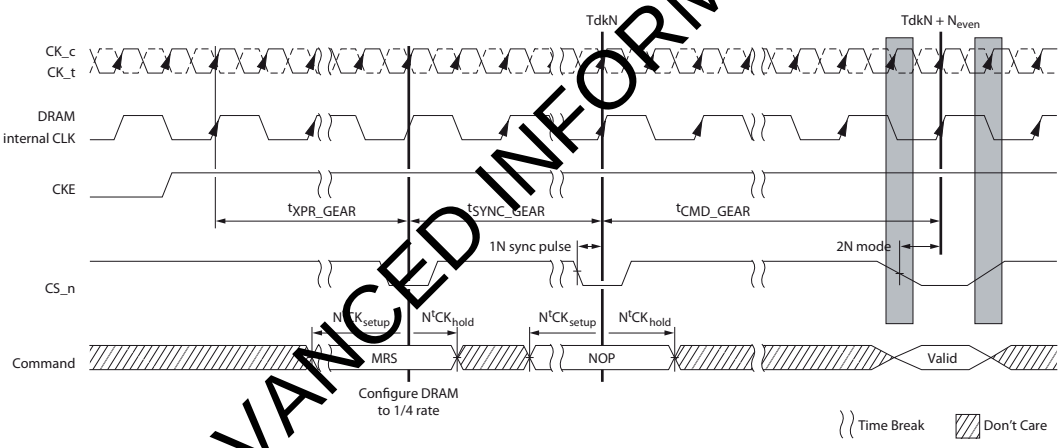
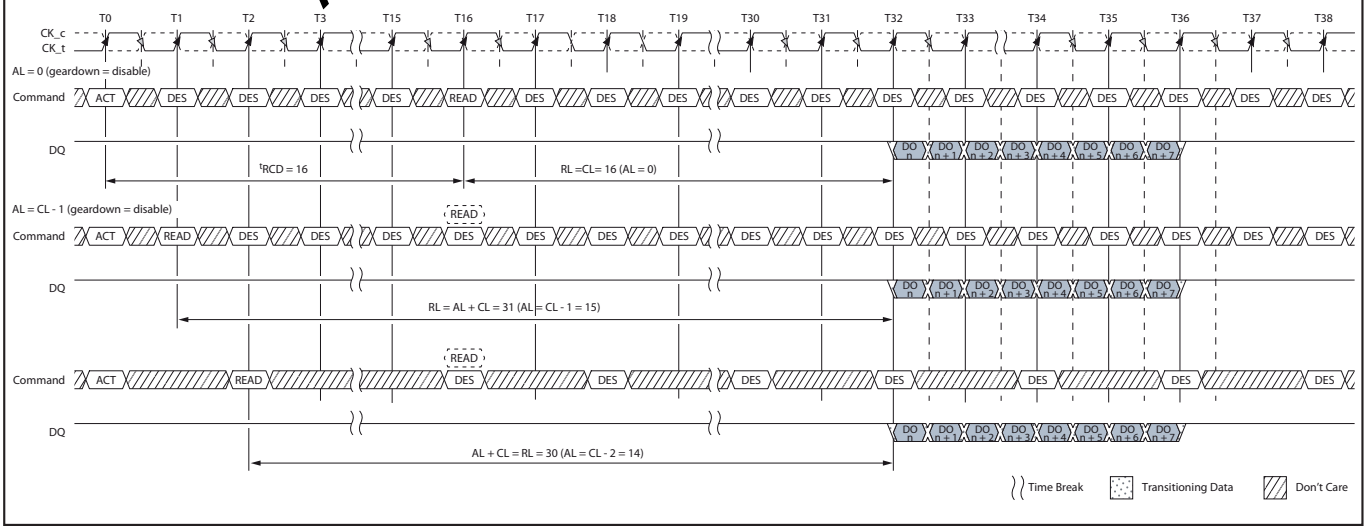


FIGURE 81: COMPARISON BETWEEN GEAR-DOWN DISABLE AND GEAR-DOWN ENABLE



Maximum Power-Saving Mode

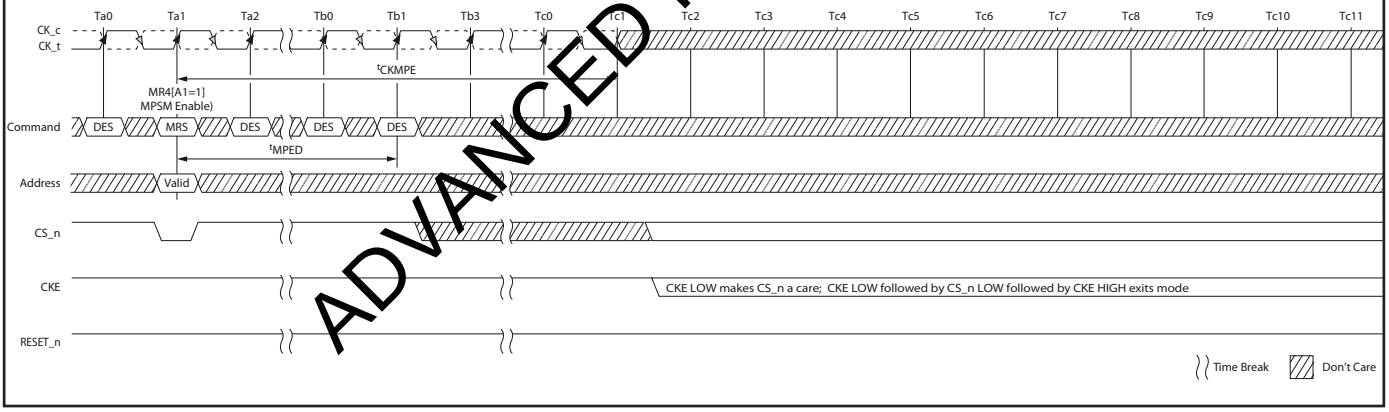
Maximum power-saving mode provides the lowest power mode where data retention is not required. When the device is in the maximum power-saving mode, it does not maintain data retention or respond to any external command, except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW. This mode is more like a “hibernate mode” than a typical power-saving mode. The intent is to be able to park the DRAM at a very low-power state; the device can be switched to an active state via the per-DRAM addressability (PDA) mode.

Maximum Power-Saving Mode Entry

Maximum power-saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the maximum power-saving mode using the per-DRAM addressability MRS command. Large CS_n hold time to CKE upon the mode exit could cause DRAM malfunction; as a result, CA parity, CAL, and gear-down modes must be disabled prior to the maximum powersaving mode entry MRS command.

The MRS command may use both address and DQ information, as defined in the Per-DRAM Addressability section. As illustrated in the figure below, after ^{t}MPED from the mode entry MRS command, the DRAM is not responsive to any input signals except CKE, CS_n, and RESET_n. All other inputs are disabled (external input signals may become High-Z). The system will provide a valid clock until ^{t}CKMPE expires, at which time clock inputs (CK) should be disabled (external clock signals may become High-Z).

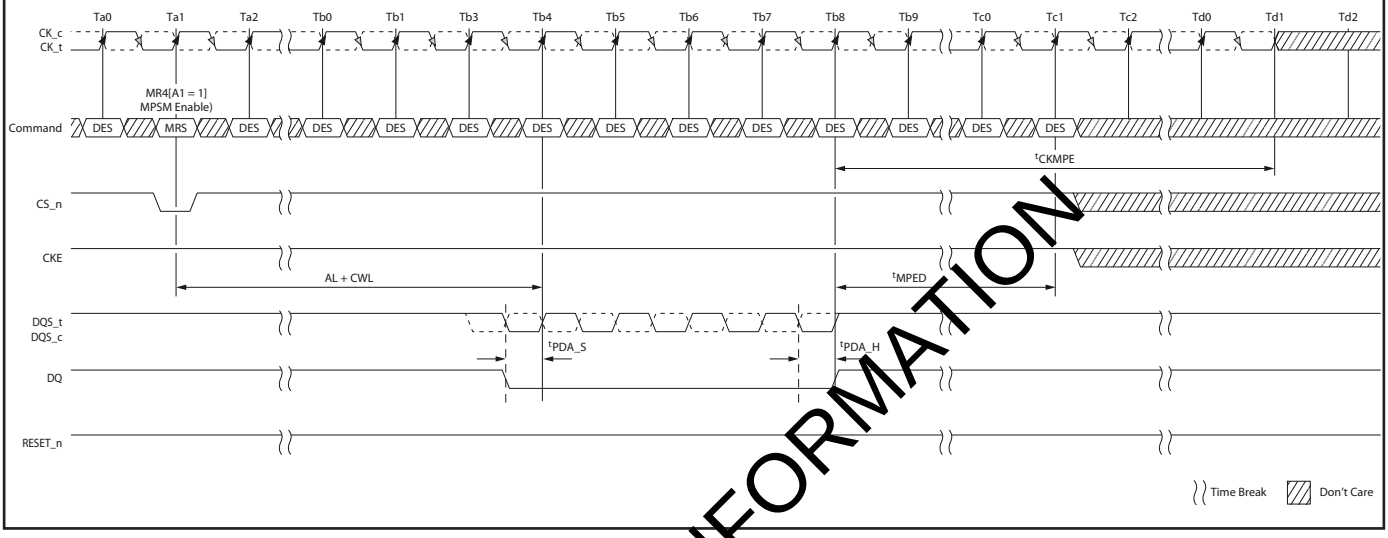
Figure 82: Maximum Power-Saving Mode Entry



Maximum Power-Saving Mode Entry in PDA

The sequence and timing required for the maximum power-saving mode with the per-DRAM addressability enabled is illustrated in the figure below.

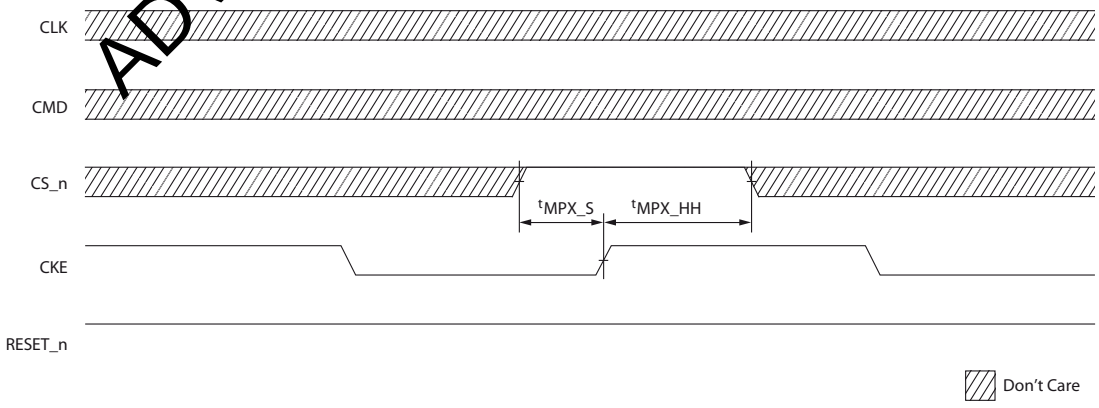
Figure 83: Maximum Power-Saving Mode Entry with PDA



CKE Transition During Maximum Power-Saving Mode

The following figure shows how to maintain maximum power-saving mode even though the CKE input may toggle. To prevent the device from exiting the mode, CS_n should be HIGH at the CKE LOW-to-HIGH edge, with appropriate setup (^{t}MPX_S) and hold (^{t}MPX_H) timings.

Figure 84: Maintining Maximum Power-Saving Mode with CKE Transition

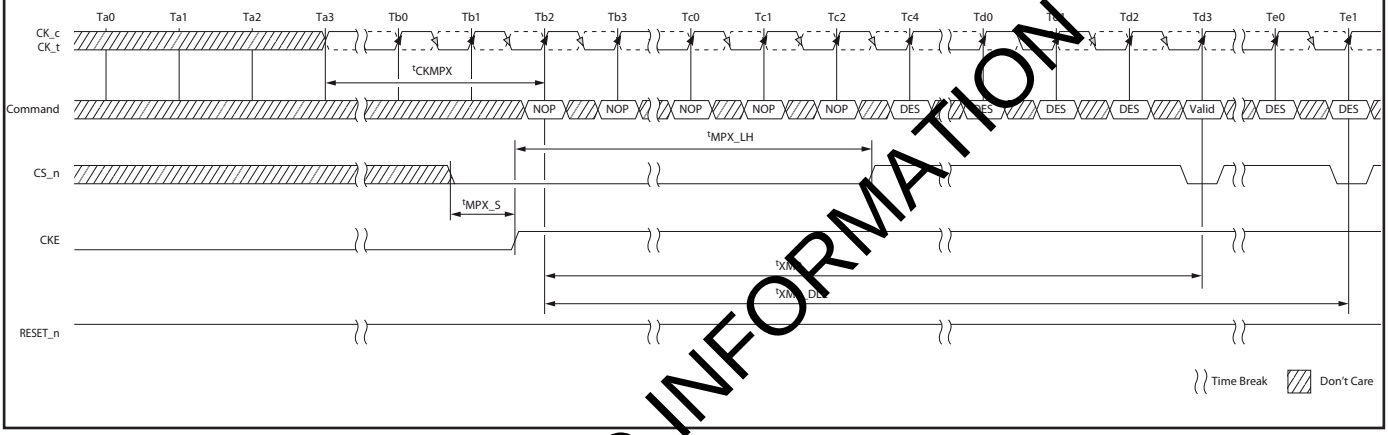


Maximum Power-Saving Mode Exit

To exit the maximum power-saving mode, CS_n should be LOW at the CKE LOW-to-HIGH transition, with appropriate setup (^{t}MPX_S) and hold (^{t}MPX_LH) timings, as shown in the figure below.

Because the clock receivers (CK_t, CK_c) are disabled during this mode, CS_n = LOW is captured by the rising edge of the CKE signal. If the CS_n signal level is detected LOW, the DRAM clears the maximum power-saving mode MRS bit and begins the exit procedure from this mode. The external clock must be restarted and be stable by tCKMPX before the device can exit the maximum power-saving mode. During the exit time (^{t}XMP), only NOP and DES commands are allowed: NOP during ^{t}MPX_LH and DES the remainder of ^{t}XMP. After tXMP expires, valid commands not requiring a locked DLL are allowed; after ^{t}XMP_DLL expires, valid commands requiring a locked DLL are allowed.

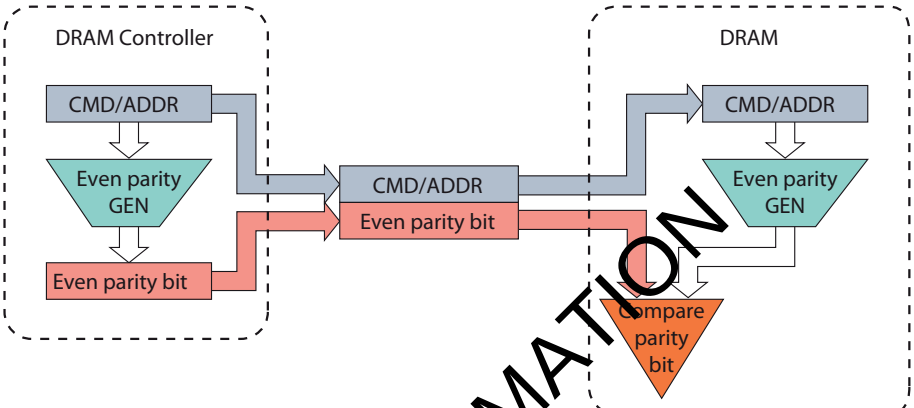
FIGURE 85: MAXIMUM POWER-SAVING MODE EXIT



Command/Address Parity

Command/address (CA) parity takes the CA parity signal (PAR) input carrying the parity bit for the generated address and commands signals and matches it to the internally generated parity from the captured address and commands signals.

FIGURE 86: COMMAND/ADDRESS PARITY OPERATION



CA parity is disabled or enabled via an MRS command. If CA parity is enabled by programming a non-zero value to CA parity latency in the MR, the DRAM will ensure that there is no parity error before executing commands. There is an additional delay required for executing the commands versus when parity is disabled. The delay is programmed in the MR when CA parity is enabled (parity latency) and applied to all commands which are registered by CS_n (rising edge of CK_t and falling CS_n). The command is held for the time of the parity latency (PL) before it is executed inside the device. The command captured by the input clock has an internal delay before executing and is determined with PL. When CA parity is enabled, only DES are allowed between valid commands. PAR will go active when the DRAM detects a CA parity error.

CA parity covers ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, the address bus including bank address and bank group bits, and C[2:0] on 3DS devices; the control signals CKE, ODT, and CS_n are not covered. For example, for a 4Gb x4 monolithic device, parity is computed across BG[1:0], BA[1:0], A16/RAS_n, A15/CAS_n, A14/ WE_n, A[13:0], and ACT_n. The DRAM treats any unused address pins internally as zeros; for example, if a common die has stacked pins but the device is used in a monolithic application, then the address pins used for stacking and not connected are treated internally as zeros.

The convention for parity is even parity; for example, valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words, the parity bit is chosen so that the total number of ones in the transmitted signal, including the parity bit, is even.

If a DRAM device detects a CA parity error in any command qualified by CS_n, it will perform the following steps:

1. Ignore the erroneous command. Commands in the MAX N*n*CK window (^{t}PAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the device does not activate DQS outputs.
2. Log the error by storing the erroneous command and address bits in the MPR error log.
3. Set the parity error status bit in the mode register to 1. The parity error status bit must be set before the ALERT_n signal is released by the DRAM (that is, ^{t}PAR_ALERT_ON + ^{t}PAR_ALERT_PW (MIN)).
4. Assert the ALERT_n signal to the host (ALERT_n is active LOW) within ^{t}PAR_ALERT_ON time.
5. Wait for all in-progress commands to complete. These commands were received ^{t}PAR_UNKOWN before the erroneous command.
6. Wait for ^{t}RAS (MIN) before closing all the open pages. The DRAM is not executing any commands during the window defined by (^{t}PAR_ALERT_ON + ^{t}PAR_ALERT_PW).

7. After ^{t}PAR_ALERT_PW (MIN) has been satisfied, the device may de-assert ALERT_n.
   a. When the device is returned to a known precharged state, ALERT_n is allowed to be de-asserted.
8. After (^{t}PAR_ALERT_PW (MAX)) the DRAM is ready to accept commands for normal operation. Parity latency will be in effect; however, parity checking will not resume until the memory controller has cleared the parity error status bit by writing a zero. The DRAM will execute any erroneous commands until the bit is cleared; unless persistent mode is enabled.

- The DRAM should have only DES commands issued around ALERT_n going HIGH such that at least 3 clocks prior and 1 clock plus 3ns after the release of ALERT_n.
- It is possible that the device might have ignored a REFRESH command during ^{t}PAR_ALERT_PW or the REFRESH command is the first erroneous frame, so it is recommended that extra REFRESH cycles be issued, as needed.
- The parity error status bit may be read anytime after ^{t}PAR_ALERT_ON + ^{t}PAR_ALERT_PW to determine which DRAM had the error. The device maintains the error log for the first erroneous command until the parity error status bit is reset to a zero or a second CA parity occurs prior to resetting.

The mode register for the CA parity error is defined as follows: CA parity latency bits are write only, the parity error status bit is read/write, and error logs are read-only bits. The DRAM controller can only program the parity error status bit to zero. If the DRAM controller illegally attempts to write a 1 to the parity error status bit, the DRAM can not be certain that parity will be checked; the DRAM may opt to block the DRAM controller from writing a 1 to the parity error status bit.

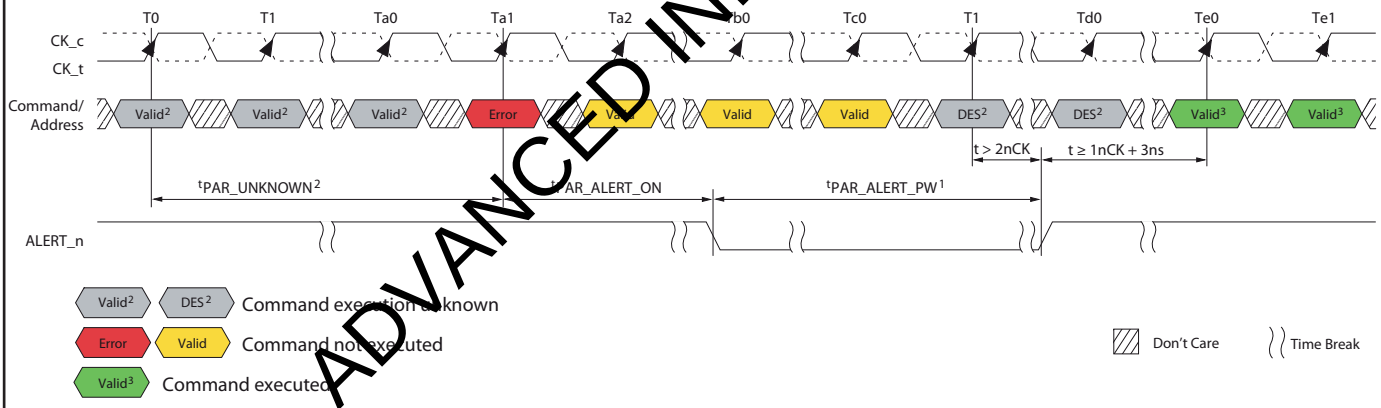
The device supports persistent parity error mode. This mode is enabled by setting MR5[9] = 1; when enabled, CA parity resumes checking after the ALERT_n is de-asserted, even if the parity error status bit remains a 1. If multiple errors occur before the error status bit is cleared the error log in MPR Page 1 should be treated as “Don’t Care.” In persistent parity error mode the ALERT_n pulse will be asserted and de-asserted by the DRAM as defined with the MIN and MAX value ^{t}PAR_ALERT_PW. The DRAM controller must issue DESELECT commands once it detects the ALERT_n signal, this response time is defined as ^{t}PAR_ALERT_RSP. The following figures capture the flow of events on the CA bus and the ALERT_n signal.

Table 110: Mode Register Setting for CA Parity

CA Parity Latency MR5[2:0][1]	Applicable Speed Bin	Parity Error Status	Parity Persistent Mode	Erroneous CA Frame
000 = Disabled	N/A	MR5 [4] 0 = Clear MR5 [4] 1 = Error	MR5 [9] 0 = DisabledMR5 [9] 1 = Enabled	C[2:0], ACT_n, BG1, BG0, BA[1:0], PAR, A17, A16/RAS_n, A15/CAS_n, A14/WE_n, A[13:0]
001 = 4 clocks	1600, 1866, 2133			
010 = 5 clocks	2400			
011 = 6 clocks	2666			
100 = 8 clocks	2933, 3200			
101 = Reserved	RFU			
110 = Reserved	RFU			
111 = Reserved	RFU			

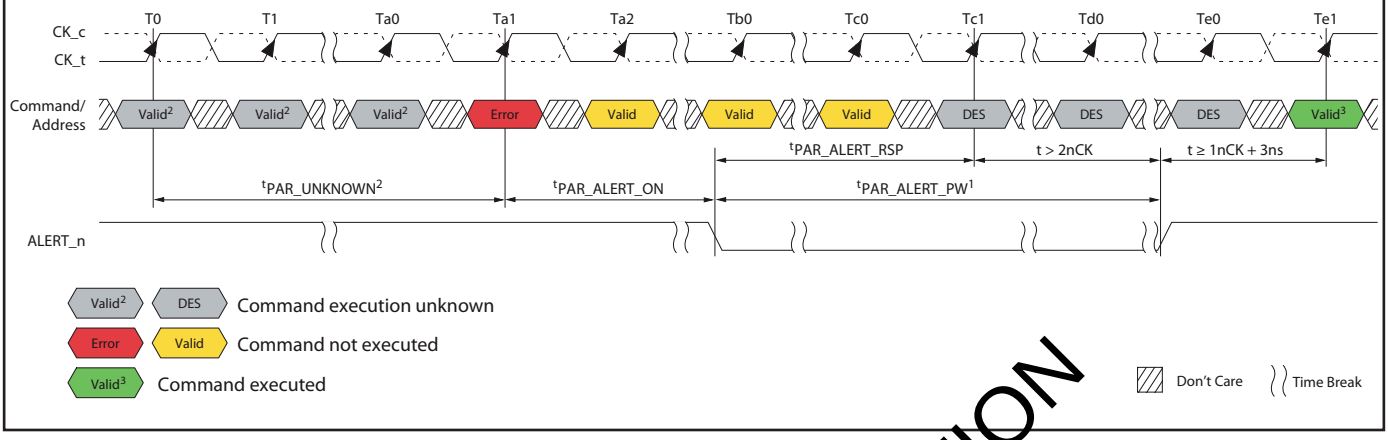
Notes:
1. Parity latency is applied to all commands.
2. 2. Parity latency can be changed only from a CA parity disabled state; for example, a direct change from PL = 3 to PL = 4 is not allowed. The correct sequence is PL = 3 to disabled to PL = 4.
3. 3. Parity latency is applied to WRITE and READ latency. WRITE latency = AL + CWL + PL. READ latency = AL + CL + PL.

Figure 87: Command/Address Parity During Normal Operation



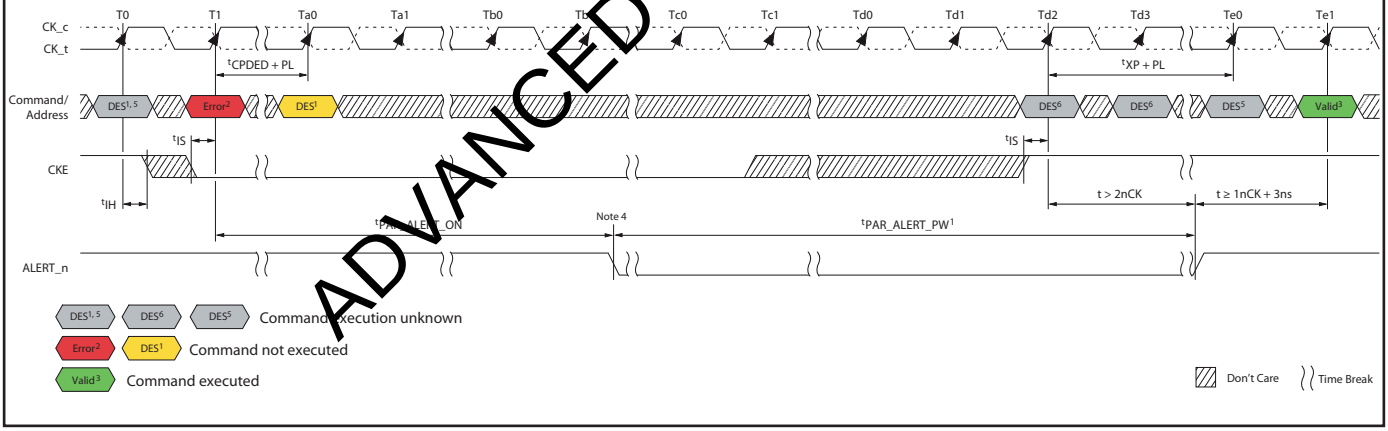
Notes:
1. DRAM is emptying queues. Precharge all and parity checking are off until parity error status bit is cleared.
2. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit is cleared.

FIGURE 88: PERSISTENT CA PARITY ERROR CHECKING OPERATION



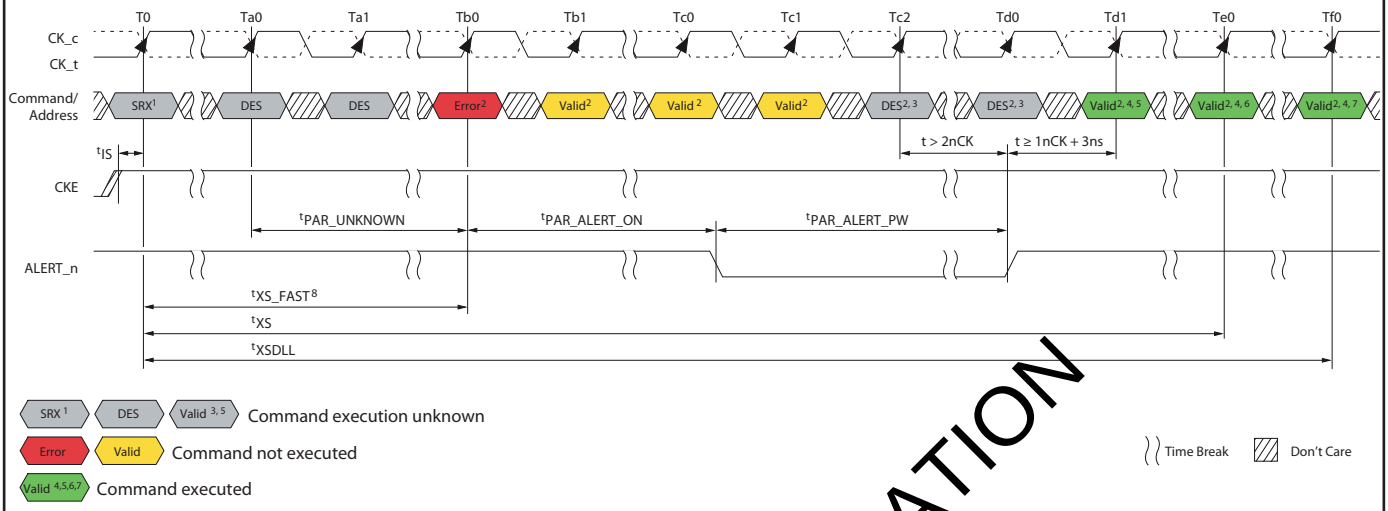
Notes:
1. DRAM is emptying queues. Precharge all and parity check re-enable finished by tPAR_ALERT_PW.
2. 2. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
3. 3. Normal operation with parity latency and parity checking (CA parity persistent error mode enabled).

FIGURE 89: CA PARITY ERROR CHECKING - SRE ATTEMPT



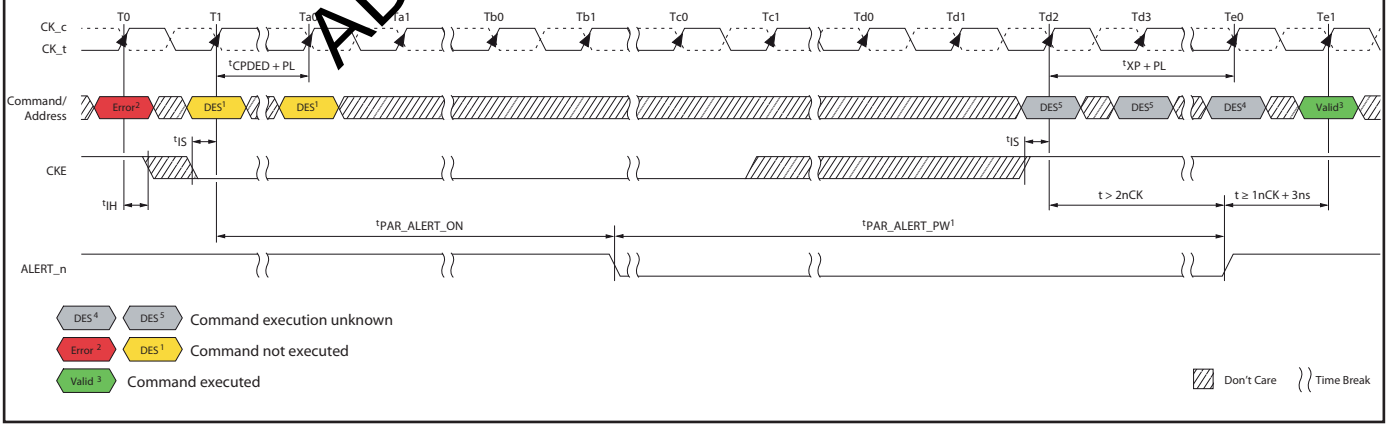
Notes:
1. Only DESELECT command is allowed.
2. SELF REFRESH command error. The DRAM masks the intended SRE command and enters precharge power-down.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until the parity error status bit cleared.
4. The controller cannot disable the clock until it has been capable of detecting a possible CA parity error.
5. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
6. Only a DESELECT command is allowed; CKE may go HIGH prior to Tc2 as long as DES commands are issued.

FIGURE 90: CA PARITY ERROR CHECKING - SRX ATTEMPT



Notes:
1. Self refresh abort = disable: MR4 [9] = 0.
2. Input commands are bounded by tXSDLL, tXS, tXS_ABORT, and tXS_FAST timing.
3. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
4. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking off until parity error status bit cleared.
5. Only an MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL command is allowed.
6. Valid commands not requiring a locked DLL.
7. Valid commands requiring a locked DLL.
8. This figure shows the case from which the error occurred after tXS_FAST. An error may also occur after tXS_ABORT and tXS.

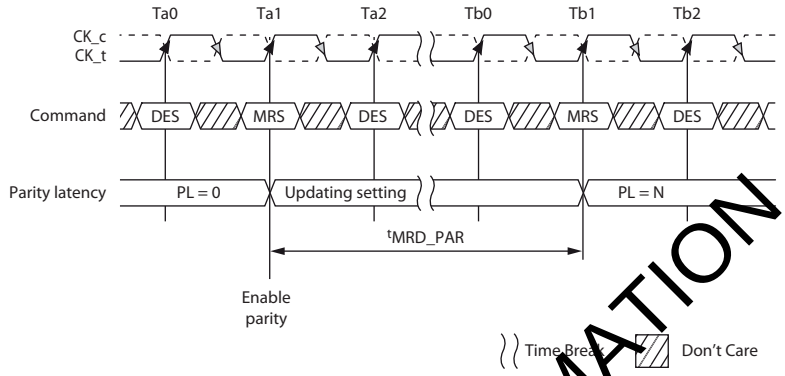
FIGURE 91: CA PARITY ERROR CHECKING - PDE/PDX



Notes:
1. Only DESELECT command is allowed.
2. Error could be precharge or activate.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit cleared.

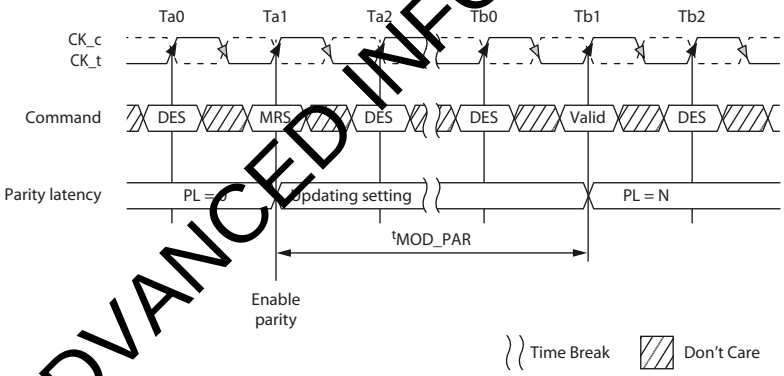
4. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
5. Only a DESELECT command is allowed; CKE may go HIGH prior to Td2 as long as DES commands are issued.

Figure 92: Parity Entry Timing Example - tMRD_PAR



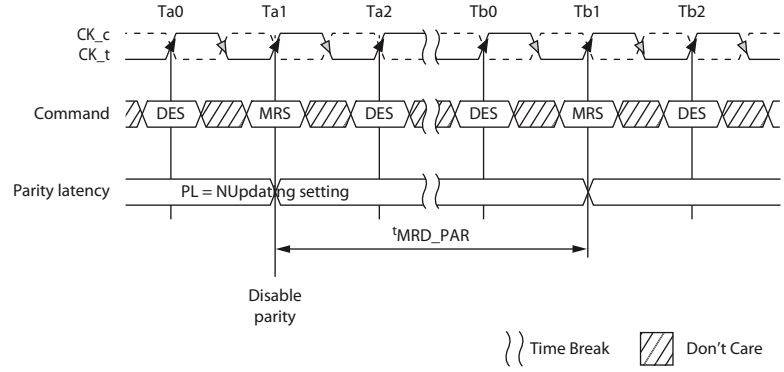
Note: 1. tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 93: Parity Entry Timing Example - tMOD_PAR



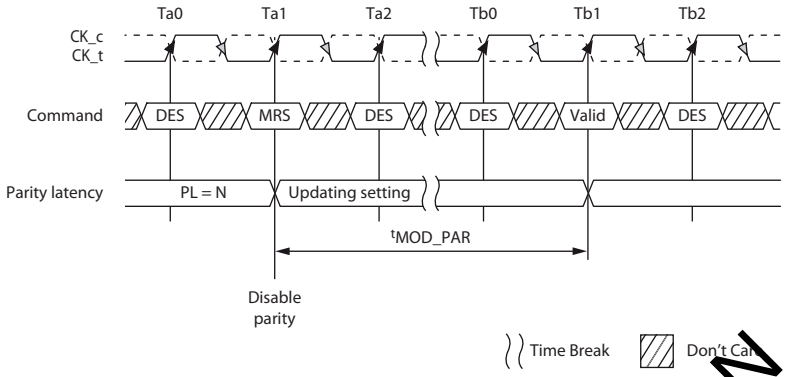
Note: 1. tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 94: Parity Exit Timing Example - tMRD_PAR



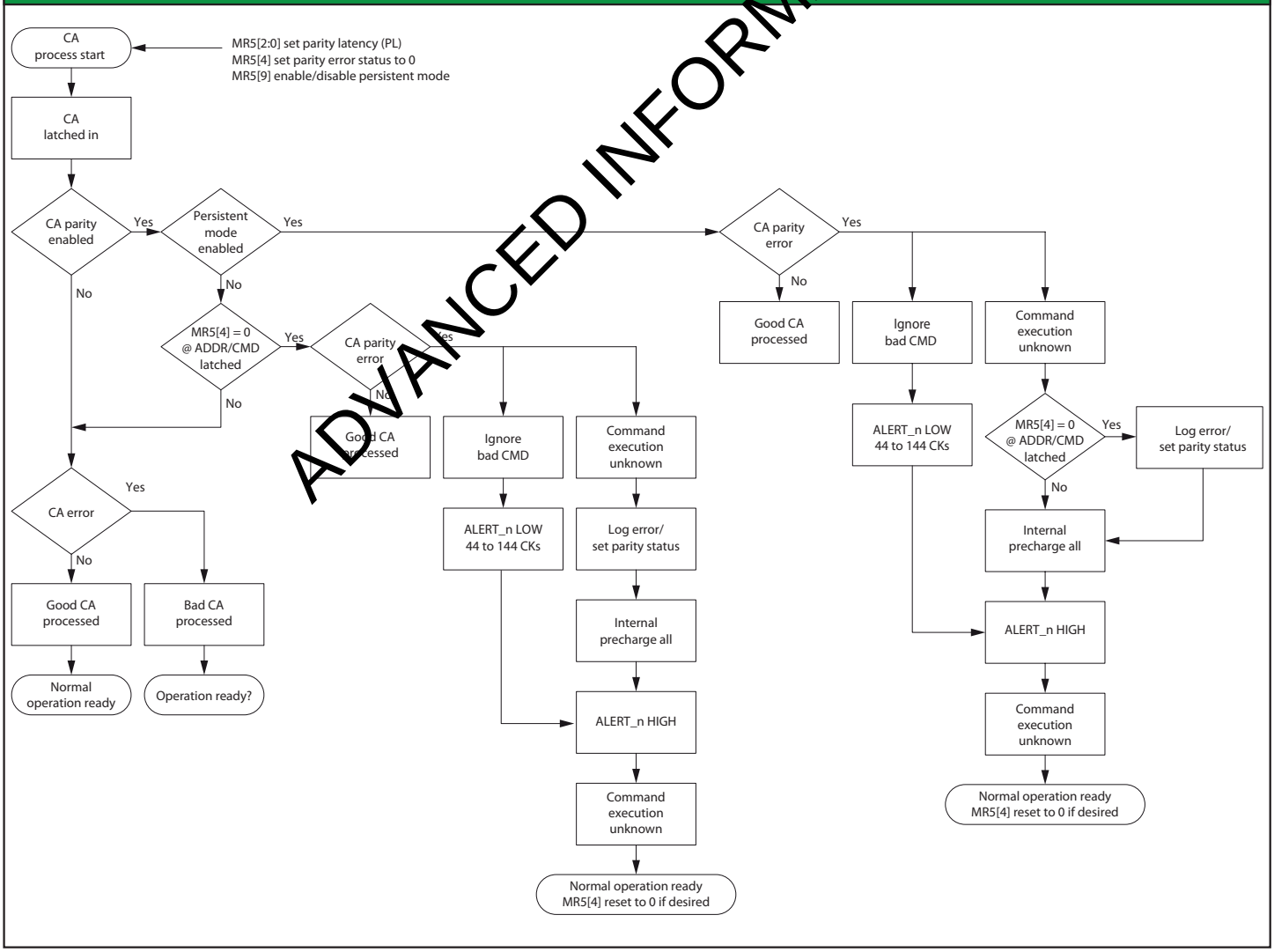
Note: 1. tMRD_PAR = tMOD + N; where N is the programmed parity latency.

FIGURE 95: PARITY EXIT TIMING EXAMPLE - ^{t}MOD_PAR



Note: 1. ^{t}MOD_PAR = ^{t}MOD + N; where N is the programmed parity latency.

FIGURE 96: CA PARITY FLOW DIAGRAM



Per-DRAM Addressability

DDR4 allows programmability of a single, specific DRAM on a rank. As an example, this feature can be used to program different ODT or V_{REF} values on each DRAM on a given rank. Because per-DRAM addressability (PDA) mode may be used to program optimal V_{REF} for the DRAM, the data set up for first DQ0 transfer or the hold time for the last DQ0 transfer cannot be guaranteed. The DRAM may sample DQ0 on either the first falling or second rising DQS transfer edge. This supports a common implementation between BC4 and BL8 modes on the DRAM. The DRAM controller is required to drive DQ0 to a stable LOW or HIGH state during the length of the data transfer for BC4 and BL8
cases.

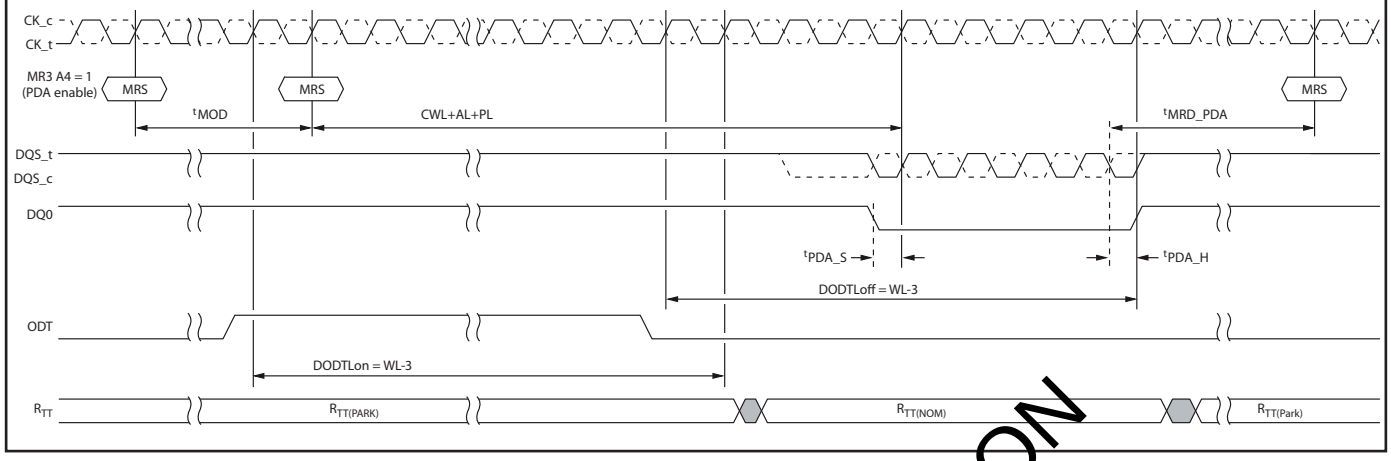
1. Before entering PDA mode, write leveling is required.
   - BL8 or BC4 may be used.
2. Before entering PDA mode, the following MR settings are possible:
   - $R_{TT(Park)}$ MR5 A[8:6] = Enable
   - $R_{TT(NOM)}$ MR1 A[10:8] = Enable
3. Enable PDA mode using MR3 [4] = 1. (The default programed value of MR3 [4] = 0.)
4. In PDA mode, all MRS commands are qualified with DQ0. The device captures DQ0 by using DQS signals. If the value on DQ0 is LOW, the DRAM executes the MRS command. If the value on DQ0 is HIGH, the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired DRAM and mode registers using the MRS command and DQ0.
6. In PDA mode, only MRS commands are allowed.
7. The MODE REGISTER SET command cycle time in PDA mode, AL + CWL + BL/2 - 0.5tCK + ^{t}MRD_PDA + PL, is required to complete the WRITE operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the device from PDA mode by setting MR3[4] = 0. (This command requires DQ0 = 0.)

Note: Removing the device from PDA mode will require programming the entire MR3 when the MRS command is issued. This may impact some PDA values programmed within a rank as the EXIT command is sent to the rank. To avoid such a case, the PDA enable/disable control bit is located in a mode register that does not have any PDA mode controls.

In PDA mode, the device captures DQ0 using DQS signals the same as in a normal WRITE operation; however, dynamic ODT is not supported. Extra care is required for the ODT setting. If $R_{TT(NOM)}$ MR1 [10:8] = enable, device data termination needs to be controlled by the ODT pin, and applies the same timing parameters (defined below).

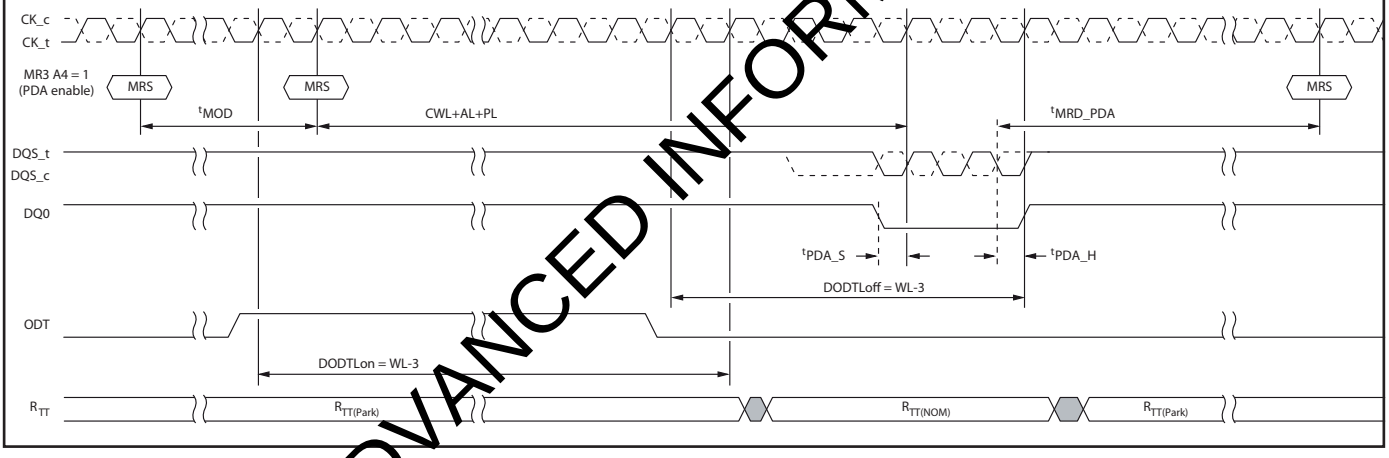
Symbol	Parameter
DODTLon	Direct ODT turnon latency
DODTLoff	Direct ODT turn off latency
^{t}ADC	R_{TT} change timing skew
^{t}AONAS	Asynchronous $R_{TT(NOM)}$ turn-on delay
^{t}AOFAS	Asynchronous $R_{TT(NOM)}$ turn-off delay

FIGURE 97: PDA OPERATION ENABLED, BL8



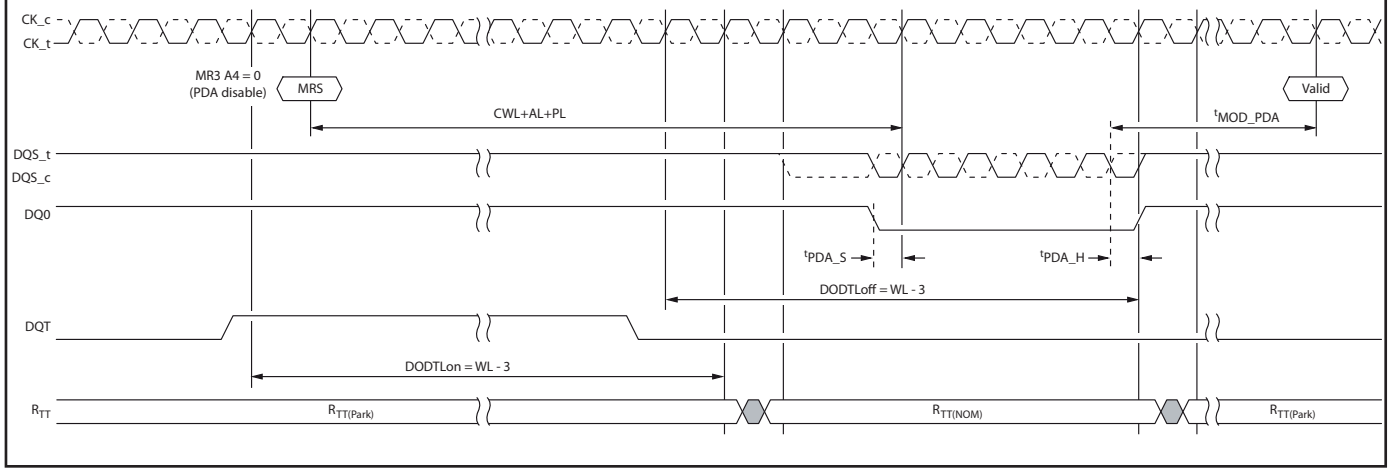
Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

FIGURE 98: PDA OPERATION ENABLED, BC4



Note: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

FIGURE 99: MRS PDA EXIT



Notes: 1. $R_{TT(Park)}$ = Enable; $R_{TT(NOM)}$ = Enable; WRITE preamble set = 2^{t}CK; and DLL = On.

V_{REFDQ} Calibration

The V_{REFDQ} level, which is used by the DRAM DQ input receivers, is internally generated. The DRAM V_{REFDQ} does not have a default value upon power-up and must be set to the desired value, usually via V_{REFDQ} calibration mode. If PDA or PPR modes are used prior to V_{REFDQ} calibration, V_{REFDQ} should initially be set at the midpoint between the $V_{DD,max}$, and the LOW as determined by the driver and ODT termination selected with wide voltage swing on the input levels and setup and hold times of approximately 0.75UI. The memory controller is responsible for V_{REFDQ} calibration to determine the best internal V_{REFDQ} level. The V_{REFDQ} calibration is enabled/disabled via MR6[7], MR6[6] selects Range 1 (60% to 92.5% of V_{DDQ}) or Range 2 (45% to 77.5% of V_{DDQ}), and an MRS protocol using MR6[5:0] to adjust the V_{REFDQ} level up and down. MR6[6:0] bits can be altered using the MRS command if MR6[7] is disabled. The DRAM controller will likely use a series of writes and reads in conjunction with V_{REFDQ} adjustments to obtain the best V_{REFDQ}, which in turn optimizes the data eye.

The internal V_{REFDQ} specification parameters are voltage range, step size, V_{REF} step time, V_{REF} full step time, and V_{REF} valid level. The voltage operating range specifies the minimum required V_{REF} setting range for DDR4 SDRAM devices. The minimum range is defined by $V_{REFDQ,min}$ and $V_{REFDQ,max}$. As noted, a calibration sequence, determined by the DRAM controller, should be performed to adjust V_{REFDQ} and optimize the timing and voltage margin of the DRAM data input receivers. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

FIGURE 100: V_{REFDQ} VOLTAGE RANGE

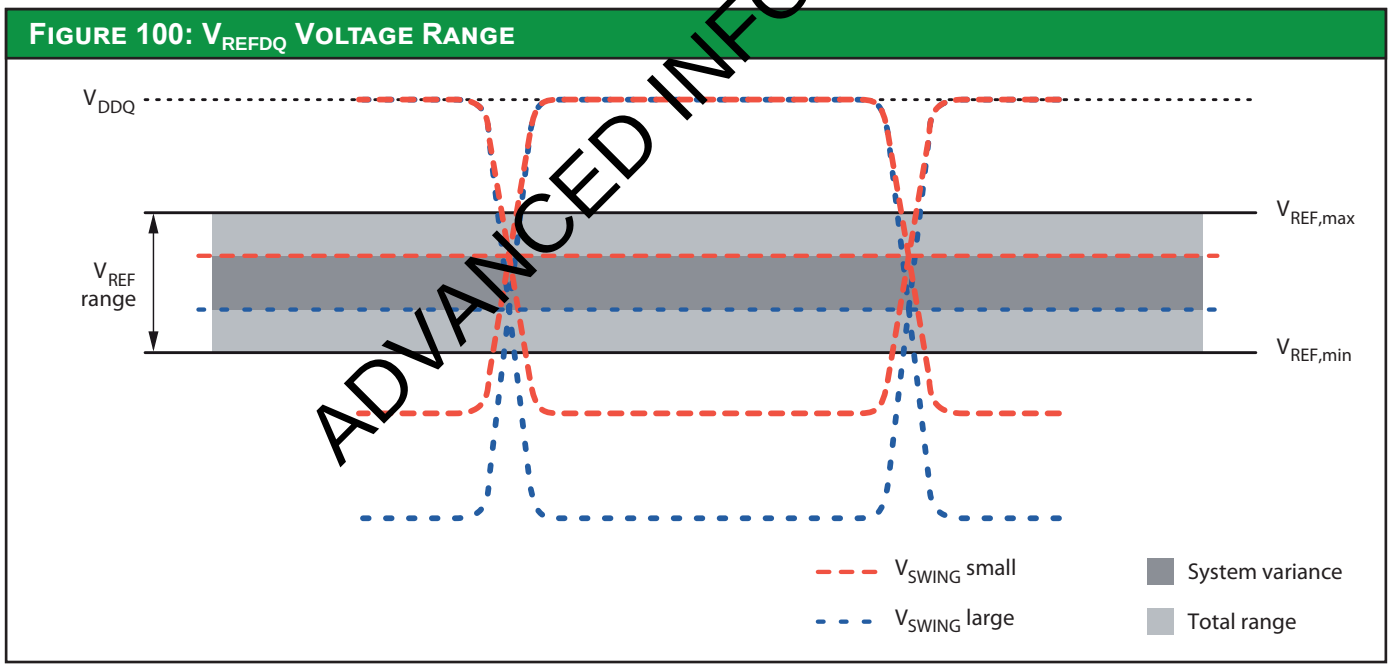


Table 111: V_{REFDQ} Range and Levels

MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1	MR6[5:0]	Range 1 MR6[6] 0	Range 2 MR6[6] 1
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15.%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 = Reserved		

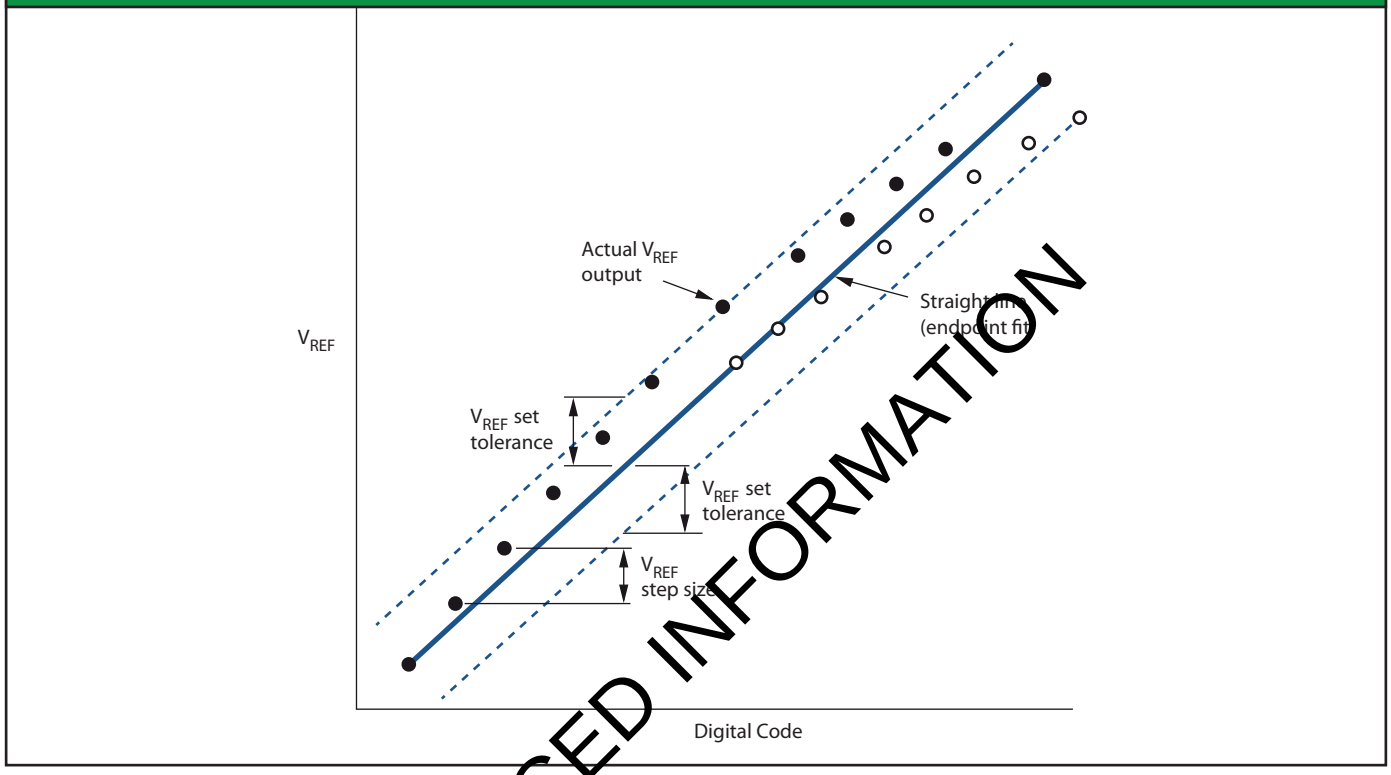
V_{REFDQ} Step Size

The V_{REF} step size is defined as the step size between adjacent steps. V_{REF} step size ranges from 0.5% V_{DDQ} to 0.8% V_{DDQ}. However, for a given design, the device has one value for V_{REF} step size that falls within the range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line, which is based on the MIN and MAX V_{REF} value endpoints for a specified range. The internal V_{REFDQ} voltage value may not be exactly within the voltage range setting coupled with the V_{REF} set tolerance; the device must be calibrated to the correct internal V_{REFDQ} voltage.

Figure 101: Example of V_{REF} Set Tolerance and Step Size



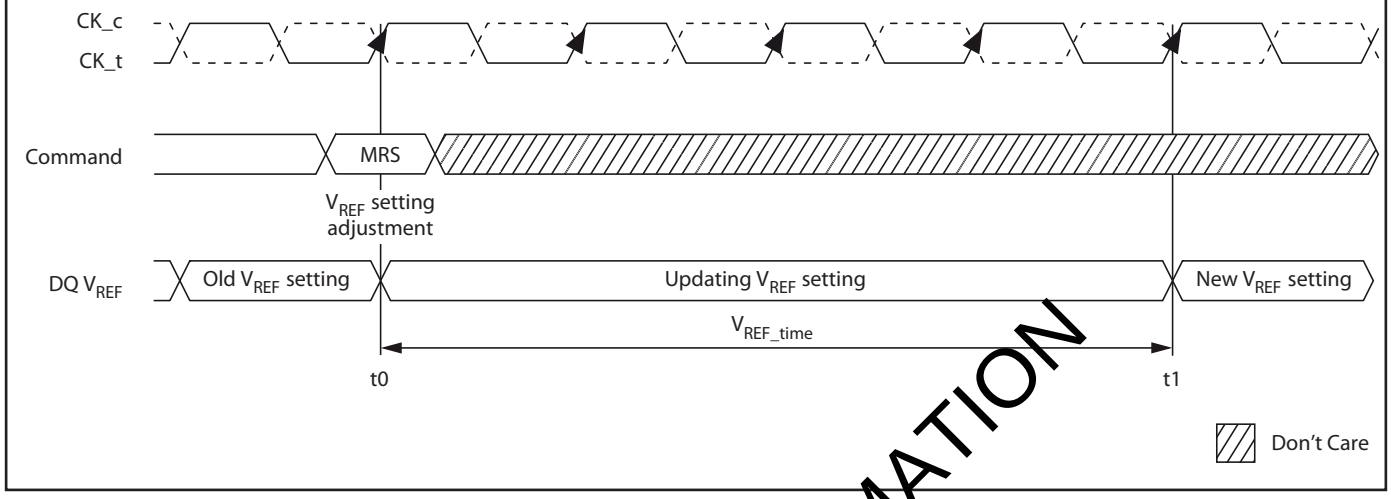
V_{REFDQ} Increment and Decrement Timing

The V_{REF} increment/decrement step times are defined by $V_{REF,time}$. $V_{REF,time}$ is defined from t0 to t1, where t1 is referenced to the VREF voltage at the final DC level within the V_{REF} valid tolerance (V_{REF,val_tol}). The V_{REF} valid level is defined by $V_{REF,val}$ tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment.

Note:

1. t0 is referenced to the MRS command clock
2. t1 is referenced to $V_{REF,tol}$

FIGURE 102: V_{REFDQ} TIMING DIAGRAM FOR $V_{REF,TIME}$ PARAMETERS



V_{REFDQ} calibration mode is entered via an MRS command, setting MR6[7] to 1 (0 disables V_{REFDQ} calibration mode) and setting MR6[6] to either 0 or 1 to select the desired range (MR6[5:0] are "Don't Care"). After V_{REFDQ} calibration mode has been entered, V_{REFDQ} calibration mode legal commands may be issued once $t_{VREFDQE}$ has been satisfied. Legal commands for V_{REFDQ} calibration mode are ACT, WR, WRA, RD, RDA, PRE, DES, and MRS to set V_{REFDQ} values, and MRS to exit V_{REFDQ} calibration mode. Also, after V_{REFDQ} calibration mode has been entered, "dummy" WRITE commands are allowed prior to adjusting the V_{REFDQ} value the first time V_{REFDQ} calibration is performed after initialization.

Setting V_{REFDQ} values requires MR6[7] be set to 1 and MR6[6] be unchanged from the initial range selection; MR6[5:0] may be set to the desired V_{REFDQ} values. If MR6[7] is set to 0, MR6[6:0] are not written. $V_{REF,time\text{-}short}$ or $V_{REF,time\text{-}long}$ must be satisfied after each MR6 command to set V_{REFDQ} value before the internal V_{REFDQ} value is valid.

If PDA mode is used in conjunction with V_{REFDQ} calibration, the PDA mode requirement that only MRS commands are allowed while PDA mode is enabled is not waived. That is, the only V_{REFDQ} calibration mode legal commands noted above that may be used are the MRS commands: MRS to set V_{REFDQ} values and MRS to exit V_{REFDQ} calibration mode.

The last MR6[6:0] setting written to MR6 prior to exiting V_{REFDQ} calibration mode is the range and value used for the internal V_{REFDQ} setting. V_{REFDQ} calibration mode may be exited when the DRAM is in idle state. After the MRS command to exit V_{REFDQ} calibration mode has been issued, DES must be issued until $^{t}V_{REFDQX}$ has been satisfied where any legal command may then be issued. V_{REFDQ} setting should be updated if the die temperature changes too much from the calibration temperature.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 1:

- MR6[7:6]10 [5:0]XXXXXXX.
  - Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).

- All subsequent V_{REFDQ} calibration MR setting commands are MR6[7:6]10 [5:0]VVVVVV.

  – "VVVVVV" are desired settings for V_{REFDQ}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- To exit V_{REFDQ} calibration, the last two V_{REFDQ} calibration MR commands are:

  – MR6[7:6]10 [5:0]VVVVVV* where VVVVVV* = desired value for V_{REFDQ}.

  – MR6[7]0 [6:0]XXXXXXX to exit V_{REFDQ} calibration mode.

The following are typical script when applying the above rules for V_{REFDQ} calibration routine when performing V_{REFDQ} calibration in Range 2:

- MR6[7:6]11 [5:0]XXXXXXX.

  Subsequent legal commands while in V_{REFDQ} calibration mode: ACT, WR, WRA, RD, RDA, PRE, DES, and MRS (to set V_{REFDQ} values and exit V_{REFDQ} calibration mode).
- All subsequent V_{REFDQ} calibration MR setting commands are MR6[7:6]11 [5:0]VVVVVV.

  – "VVVVVV" are desired settings for V_{REFDQ}.
- Issue ACT/WR/RD looking for pass/fail to determine V_{CENT} (midpoint) as needed.
- To exit V_{REFDQ} calibration, the last two VREFDQ calibration MR commands are:

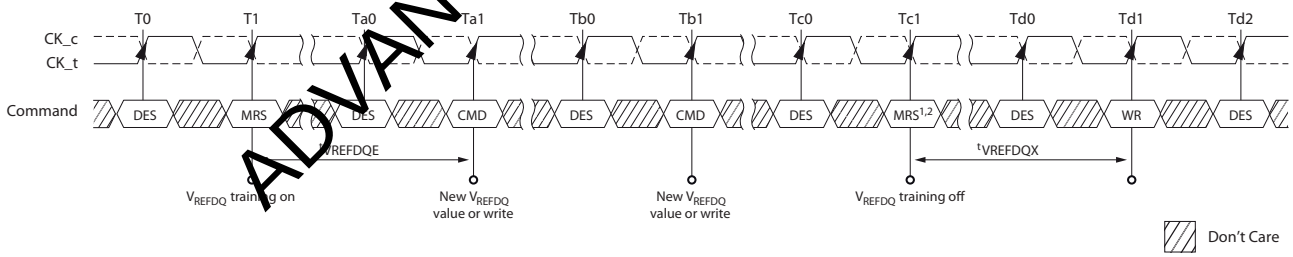
  – MR6[7:6]11 [5:0]VVVVVV* where VVVVVV* = desired value for V_{REFDQ}.

  – MR6[7]0 [6:0]XXXXXXX to exit V_{REFDQ} calibration mode.

Note:

Range may only be set or changed when entering V_{REFDQ} calibration mode; changing range while in or exiting V_{REFDQ} calibration mode is illegal.

FIGURE 103: V_{REFDQ} TRAINING MODE ENTRY AND EXIT TIMING DIAGRAM



Notes:
1. New V_{REFDQ} values are not allowed with an MRS command during calibration mode entry.
2. Depending on the step size of the latest programmed V_{REF} value, V_{REF} must be satisfied before disabling V_{REFDQ} training mode.

FIGURE 104: V_{REF} STEP: SINGLE STEP SIZE INCREMENT CASE

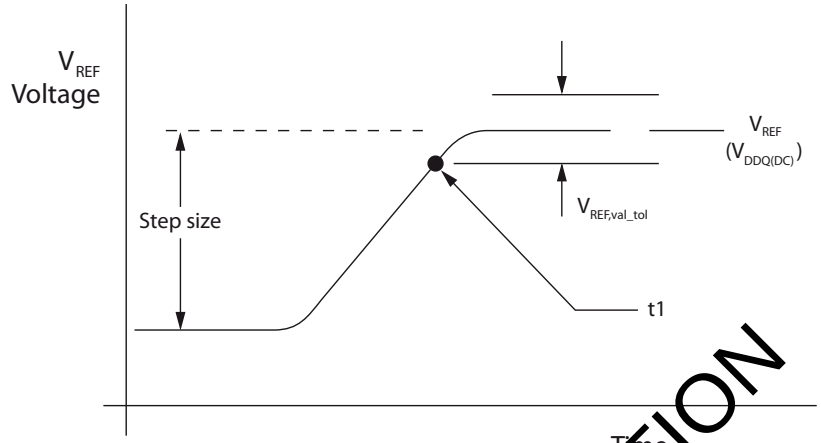


FIGURE 105: V_{REF} STEP: SINGLE STEP SIZE DECREMENT CASE

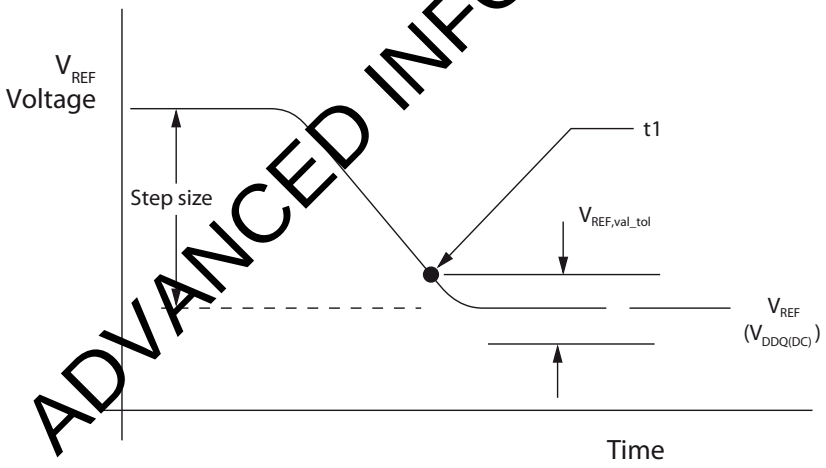


FIGURE 106: V_{REF} FULL STEP: FROM $V_{REF,MIN}$ TO $V_{REF,MAX}$ CASE

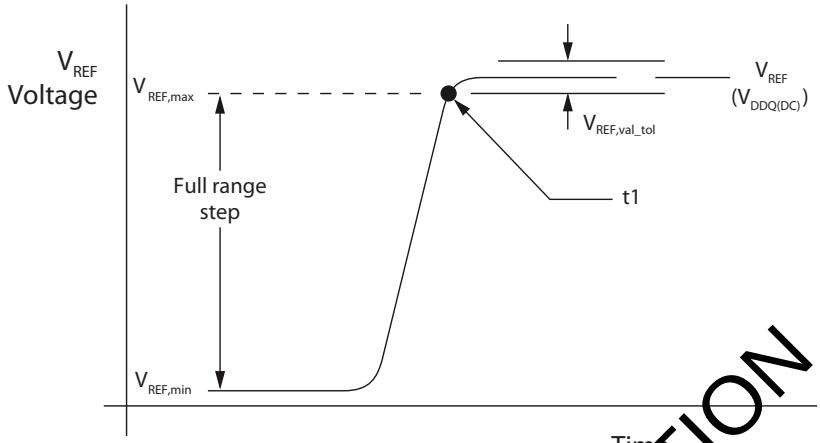
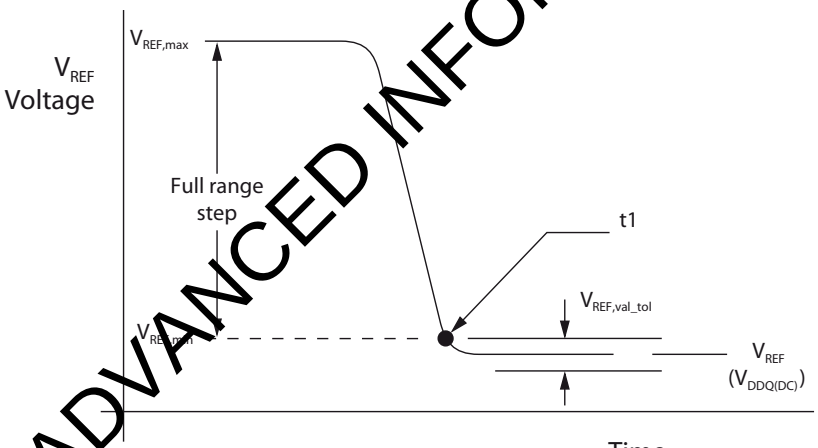


FIGURE 107: V_{REF} FULL STEP: FROM $V_{REF,MAX}$ TO $V_{REF,MIN}$ CASE



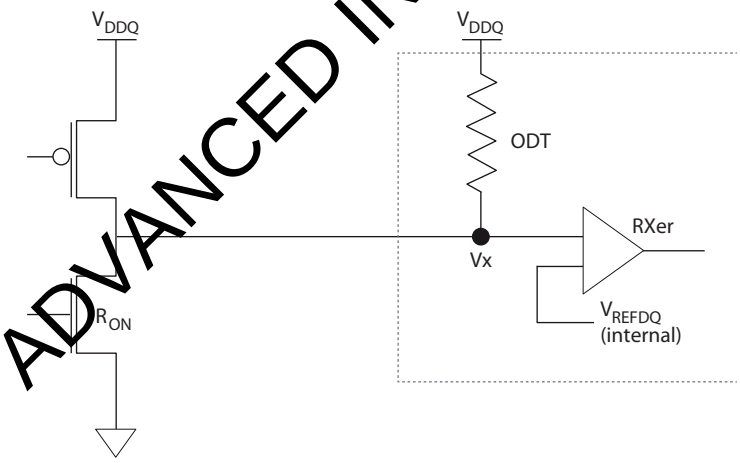
V_{REFDQ} Target Settings

The V_{REFDQ} initial settings are largely dependant on the ODT termination settings. The table below shows all of the possible initial settings available for V_{REFDQ} training; it is unlikely the lower ODT settings would be used in most cases.

TABLE 112: V_{REFDQ} SETTINGS (V_{DDQ} = 1.2V)

R_{ON}	ODT	Vx – V_{IN} LOW (mV)	V_{REFDQ} (mv)	V_{REFDQ} (%V_{DDQ})
34 ohm	34 ohm	600	900	75%
	40 ohm	550	875	73%
	48 ohm	500	850	71%
	60 ohm	435	815	68%
	80 ohm	360	780	65%
	120 ohm	265	732	61%
	240 ohm	150	675	56%
48 ohm	34 ohm	700	950	79%
	40 ohm	655	925	77%
	48 ohm	600	900	75%
	60 ohm	535	865	72%
	80 ohm	450	825	69%
	120 ohm	345	77[illegible]	64%
	240 ohm	200	[illegible]	58%

FIGURE 108: V_{REFDQ} EQUIVALENT CIRCUIT



Connectivity Test Mode

Connectivity test (CT) mode is similar to boundary scan testing but is designed to significantly speed up the testing of electrical continuity of pin interconnections between the device and the memory controller on the PC boards. Designed to work seamlessly with any boundary scan device,

Contrary to other conventional shift-register-based test modes, where test patterns are shifted in and out of the memory devices serially during each clock, the CT mode allows test patterns to be entered on the test input pins in parallel and the test results to be extracted from the test output pins of the device in parallel. These two functions are also performed at the same time, significantly increasing the speed of the connectivity check. When placed in CT mode, the device appears as an asynchronous device to the external controlling agent. After the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay time.

Note: A reset of the device is required after exiting CT mode (see RESET and Initialization Procedure).

Pin Mapping

Only digital pins can be tested using the CT mode. For the purposes of a connectivity check, all the pins used for digital logic in the device are classified as one of the following types:

- Test enable (TEN): When asserted HIGH, this pin causes the device to enter CT mode. In CT mode, the normal memory function inside the device is bypassed and the I/O pins appear as a set of test input and output pins to the external controlling agent. Additionally, the device will set the internal V_{REFDQ} to $V_{DDQ} \times 0.5$ during CT mode (this is the only time the DRAM takes direct control over setting the internal V_{REFDQ}). The TEN pin is dedicated to the connectivity check function and will not be used during normal device operation.
- Chip select (CS_n): When asserted LOW, this pin enables the test output pins in the device. When de-asserted, these output pins will be High-Z. The CS_n pin in the device serves as the CS_n pin in CT mode.
- Test input: A group of pins used during normal device operation designated as test input pins. These pins are used to enter the test pattern in CT mode.
- Test output: A group of pins used during normal device operation designated as test output pins. These pins are used for extraction of the connectivity test results in CT mode.
- RESET_n: This pin must be fixed high level during CT mode, as in normal function.

Table 113: Connectivity Mode Pin Description and Switching Levels

CT Mode Pins		Pin Name During Normal Memory Operation	Switching Level	Notes
Test enable		TEN	CMOS (20%/80% V_{DD})	1, 2
Chip select		CS_n	V_{REFCA} ±200mV	3
Test input	A	BA[1:0], BG[1:0], A[9:0], A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_c, PAR	V_{REFCA} ±200mV	3
	B	LDM_n/LDBI_n, UDM_n/LDBI_n; DM_n/DBI_n	V_{REFDQ} ±200mV	4
	C	ALERT_n	CMOS (20%/80% V_{DD})	2, 5
	D	RESET_n	CMOS (20%/80% V_{DD})	
Test output		DQ[15:0], UDQS_t, UDQS_c, LDQS_t, LDQS_c; DQS_t, DQS_c	V_{TT} ±100mV	6

Notes:
1. TEN: Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation.
2. CMOS is a rail-to-rail signal with DC HIGH at 80% and DC LOW at 20% of V_{DD} (960mV for DC HIGH and 240mV for DC LOW.)
3. V_{REFCA} should be $V_{DD}/2$.
4. V_{REFDQ} should be $V_{DDQ}/2$.
5. ALERT_n switching level is not a final setting.
6. V_{TT} should be set to $V_{DD}/2$.

Minimum Terms Definition for Login Equations

The test input and output pins are related by the following equations, where INV denotes
a logical inversion operation and XOR a logical exclusive OR operation:

MT0 = XOR (A13, A16, PAR)
MT1 = XOR (A6, ALERT_n, A9)
MT2 = XOR (A2, A5, A13)
MT3 = XOR (A0, A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n/A15)
MT5 = XOR (CKE, RAS_n/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = x16: XOR (DMU_n/DBIU_n , DML_n/DBIL_n, CK_t)
= x8: XOR (BG1, DML_n/DBIL_n, CK_t)
= x4: XOR (BG1, CK_t)
MT8 = XOR (WE_n/A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, RESET_n and TEN)

Logic Equations

DQ0 = MT0	DQ10 = INV DQ2
DQ1 = MT1	DQ11 = INV DQ3
DQ2 = MT2	DQ12 = INV DQ4
DQ3 = MT3	DQ13 = INV DQ5
DQ4 = MT4	DQ14 = INV DQ6
DQ5 = MT5	DQ15 = INV DQ7
DQ6 = MT6	LDQS_t = MT8
DQ7 = MT7	LDQS_c = MT9
DQ8 = INV DQ0	UDQS_t = INV LDQS_t
DQ9 = INV DQ1	UDQS_c = INV LDQS_c

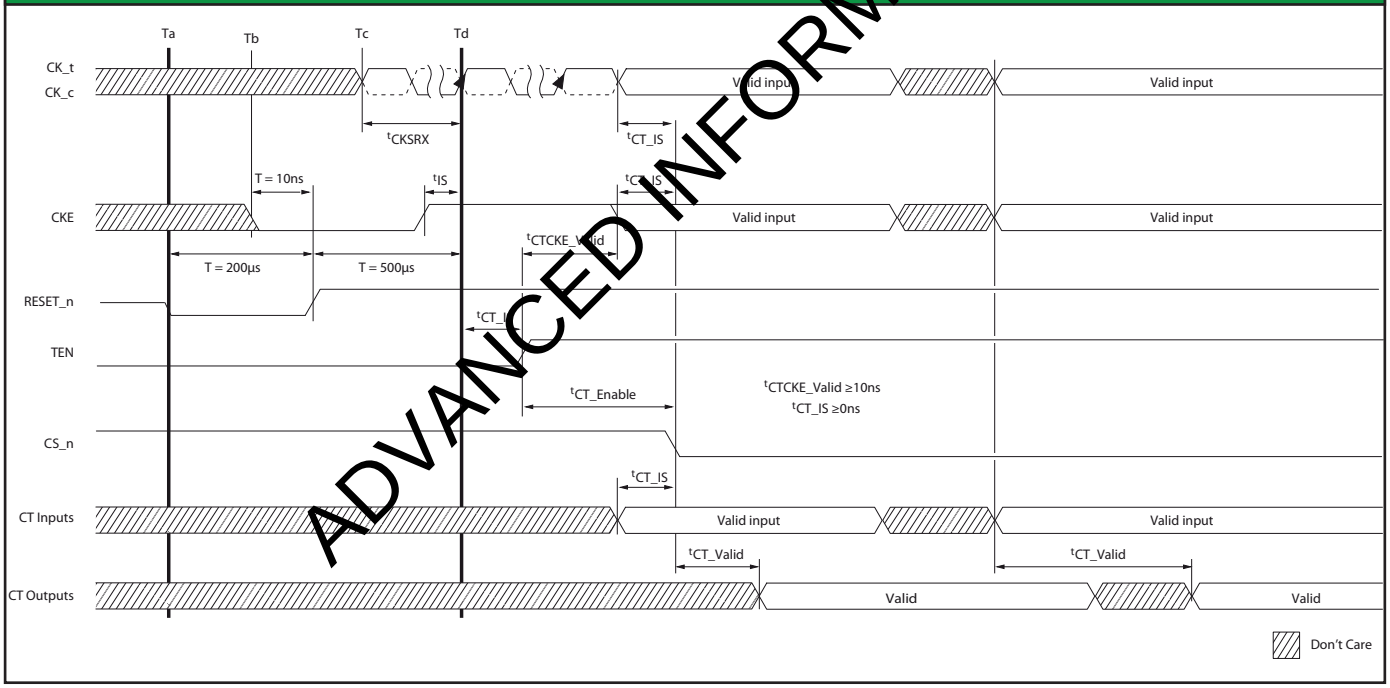
CT Input Timing Requirements

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable. Upon the assertion of the TEN pin HIGH with RESET_n, CKE and CS_n held HIGH; CLK_t, CLK_c, and CKE signals become test inputs within ^{t}CTECT_Valid. The remaining CT in-puts become valid ^{t}CT_Enable after TEN goes HIGH when CS_n allows input to begin sampling, provided inputs were valid for at least tCT_Valid. While in CT mode, refresh activities in the memory arrays are not allowed; they are initiated either externally (auto refresh) or internally (self refresh).

The TEN pin may be asserted after the DRAM has completed power-on. After the DRAM is initialized and V_{REFDQ} is calibrated, CT mode may no longer be used. The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the states and the integrity of the original content of the memory array are unknown. A full reset of the memory device is required.

After CT mode has been entered, the output signals will be stable within ^{t}CT_Valid after the test inputs have been applied as long as TEN is maintained HIGH and CS_n is maintained LOW.

Figure 109: Connectivity Test Mode Entry



Target Row Refresh Mode

Rows can be accessed a limited number of times within a certain time period before adjacent rows require refresh. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the maximum activate window (^{t}MAW) before the adjacent rows need to be refreshed, regardless of how the activates are distributed over ^{t}MAW. The row receiving the excessive actives is the target row (TRn). The two adjacent rows to be refreshed are the victim rows. The MAC values are encoded in MPR Page 3 MPR3[4:0].

Target row refresh (TTR) mode is not required to be used, and in some cases has been rendered inoperable. DDR4 devices automatically perform TRR mode in the background. Most die will provide an MPR Page 3 MPR3[3:0] of 1000, indicating there is no restriction to the number of ACTIVATE commands to a given row in a refresh period provided DRAM timing specifications are not violated.

Table 114: MAC Encoding of MPR Page 3 MPR3

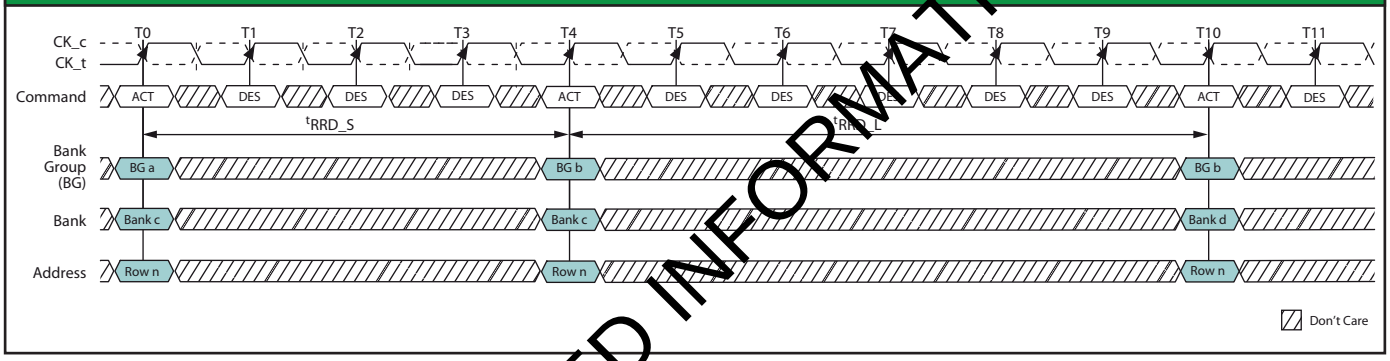
0	0	0	0	Untested	The device has not been tested for MAC.
0	0	0	1	^{t}MAC = 700K	
0	0	1	0	^{t}MAC = 700K	
0	0	1	1	^{t}MAC = 700K	
0	1	0	0	^{t}MAC = 700K	
0	1	0	1	^{t}MAC = 700K	
0	1	1	0	Reserved	
0	1	1	1	^{t}MAC = 200K	
1	0	0	0	Unlimited	There is no restriction to the number of ACTIVATE commands to a given row in a refresh period provided DRAM timing specifications are not violated.
1	0	0	1	Reserved	
:	:	:	:	Reserved	
1	1	1	1	Reserved	

Note: 1. MAC encoding in MPR Page 3 MPR3.

ACTIVATE Command

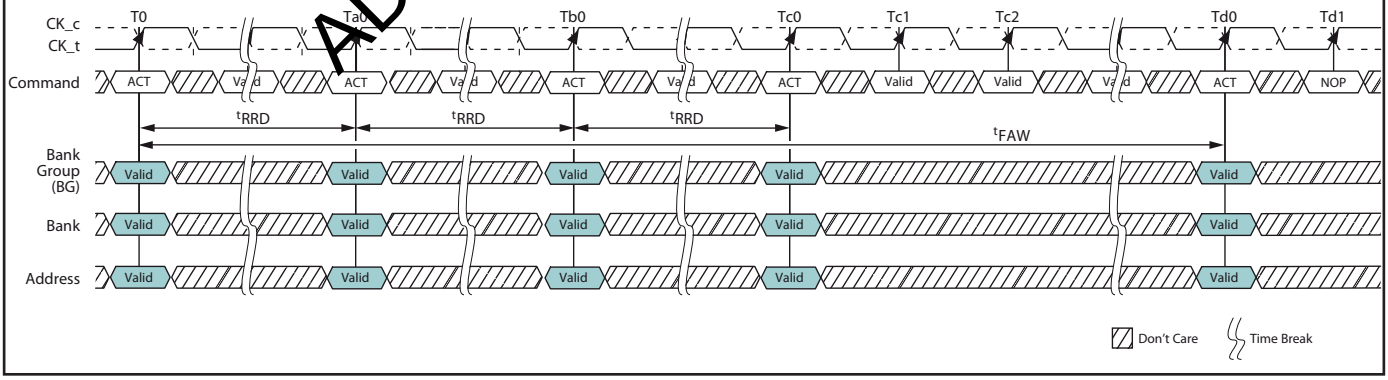
The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access. The value on the BG[0] input select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[16:0] selects 4the row within the bank. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. tRRD_S (short) is used for timing between banks located in different bank groups. tRRD_L (long) is used for timing between banks located in the same bank group. Another timing restriction for consecutive ACTIVATE commands [issued at tRRD (MIN)] is tFAW (fifth activate window). Because there is a maximum of four banks in a bank group, the tFAW parameter applies across different bank groups (five ACTIVATE commands issued at tRRD_L (MIN) to the same bank group would be limited by tRC).

FIGURE 110: TRRD TIMING



Notes:
1. tRRD_S; ACTIVATE-to-ACTIVATE command period (short); applies to consecutive ACTIVATE commands to different bank groups (that is, T0 and T4).
2. 2. tRRD_L; ACTIVATE-to-ACTIVATE command period (long); applies to consecutive ACTIVATE commands to the different banks in the same bank group (that is, T4 and T10).

FIGURE 111: TFAW TIMING



Note: 1. tFAW; four activate windows.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto precharge feature is engaged when a READ or WRITE command is issued with A10 HIGH. The auto precharge feature uses the RAS lockout circuit to internally delay the PRECHARGE operation until the ARRAY RESTORE operation has completed. The RAS lockout circuit feature allows the PRECHARGE operation to be partially or completely hidden during burst READ cycles when the auto precharge feature is engaged. The PRECHARGE operation will not begin until after the last data of the burst write sequence is properly stored in the memory array.

REFRESH Command

REFRESH Command

The REFRESH command (REF) is used during normal operation of the device. This command is nonpersistent, so it must be issued each time a refresh is required. The device requires REFRESH cycles at an average periodic interval of ^{t}REFI. When CS_n, RAS_n/A16, and CAS_n/A15 are held LOW and WE_n/A14 HIGH at the rising edge of the clock, the device enters a REFRESH cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time, ^{t}RP (MIN), before the REFRESH command can be applied. The refresh addressing is generated by the internal DRAM refresh controller. This makes the address bits “Don’t Care” during a REFRESH command. An internal address counter supplies the addresses during the REFRESH cycle. No con-trol of the external address bus is required once this cycle has started. When the REFRESH cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the REFRESH command and the next valid command, except DES, must be greater than or equal to the minimum REFRESH cycle time ^{t}RFC (MIN).

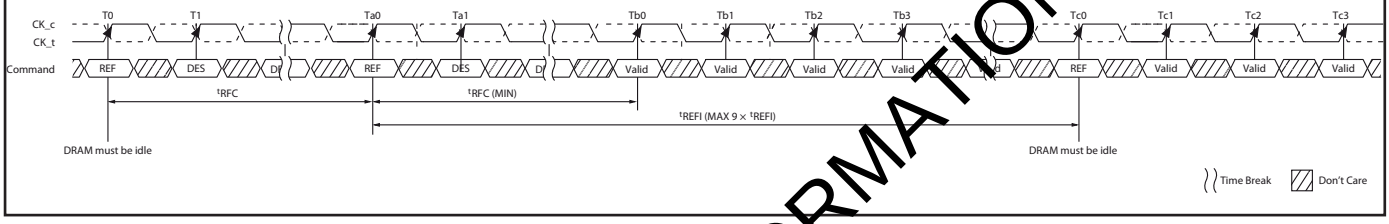
Note: The ^{t}RFC timing parameter depends on memory density.

In general, a REFRESH command needs to be issued to the device regularly every ^{t}REFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pullingin the REFRESH command. A limited number REFRESH commands can be postponed depending on refresh mode: a maximum of 8 REFRESH commands can be postponed when the device is in 1X refresh mode; a maximum of 16 REFRESH commands can be postponed when the device is in 2X refresh mode; and a maximum of 32 REFRESH commands can be postponed when the device is in 4X refresh mode.

When 8 consecutive REFRESH commands are postponed, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × ^{t}REFI. For both the 2X and 4X refresh modes, the maximum consecutive RE-FRESH commands allowed is limited to 17 × ^{t}REFI2 and 36 × ^{t}REFI4, respectively.

A limited number REFRESH commands can be pulled-in as well. A maximum of 8 additional REFRESH commands can be issued in advance or “pulled-in” in 1X refresh mode, a maximum of 16 additional REFRESH commands can be issued when in advance in 2X refresh mode, and a maximum of 32 additional REFRESH commands can be issued in advance when in 4X refresh mode. Each of these REFRESH commands reduces the number of regular REFRESH commands required later by one. Note that pulling in more than the maximum allowed REFRESH commands in advance does not further reduce the number of regular REFRESH commands required later, so that the resulting maximum interval between two surrounding REFRESH commands is limited to 9 × ^{t}REFI (Figure 77 (page 134)), 18 × ^{t}RFEI2, or 36 × ^{t}REFI4. At any given time, a maximum of 16 REF commands can be issued within 2 × ^{t}REF, 32 REF2 commands can be issued within 4 × ^{t}REF, and 64 REF4 commands can be issued within 8 × ^{t}REFI4.

FIGURE 112: REFRESH COMMAND TIMING



Notes:
1. Only DES commands are allowed after a REFRESH command is registered until ^{t}RFC (MIN) expires.
2. Time interval between two REFRESH commands may be extended to a maximum of 9 × ^{t}REFI.

FIGURE 113: POSTPONING REFRESH COMMANDS (EXAMPLE)

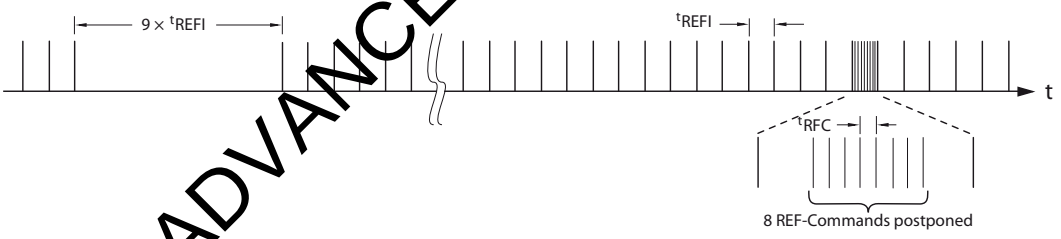
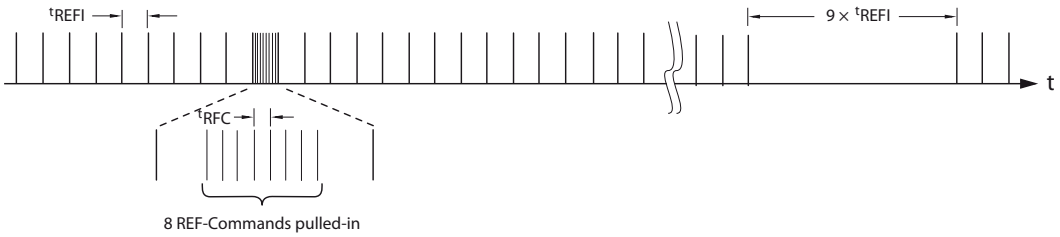


FIGURE 114: PULLING IN REFRESH COMMANDS (EXAMPLE)



Temperature-Controlled Refresh Mode

During normal operation, temperature-controlled refresh (TCR) mode disabled, the device must have a REFRESH command issued once every ^{t}REFI, except for what is allowed by posting (see REFRESH Command section). This means a REFRESH command must be issued once every 2us if TC is greater than 95°C, 3.9µs if TC is greater than or equal to 85°C, and once every 7.8µs if TC is less than 85°C.

Table 115: Normal ^{T}REFI Refresh (TCR Disabled)

	Normal Temperature		Extended Temperature	
Temperature	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
T_C < 45°C	7.8µs	7.8µs	3.9µs [1]	3.9µs [1]
45°C ≤ T_C < 85°C				
85°C ≤ T < 95°C	N/A			
95°C ≤ T_C			1.9µs	1.9µs

Note: 1. If T_C is less than 85°C, the external refresh period can be 7.8µs instead of 3.9µs.

When TCR mode is enabled, the device will register the externally supplied REFRESH command and adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range, when allowed, by skipping REFRESH commands with the proper gear ratio. TCR mode has two ranges to select between the normal temperature range and the extended temperature range; the correct range must be selected so the internal control operates correctly. The DRAM must have the correct refresh rate applied externally; the internal refresh rate is determined by the DRAM based upon the temperature.

TCR Mode - Normal Temperature Range

REFRESH commands should be issued to the device with the refresh period equal to or shorter than ^{t}REFI of normal temperature range (0°C to 85°C). In this mode, the system guarantees that the temperature does not exceed 85°C. The device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when TC is below 45°C. The internal refresh period is automatically adjusted inside the DRAM, and the DRAM controller does not need to provide any additional control.

TCR Mode - Extended Temperature Range

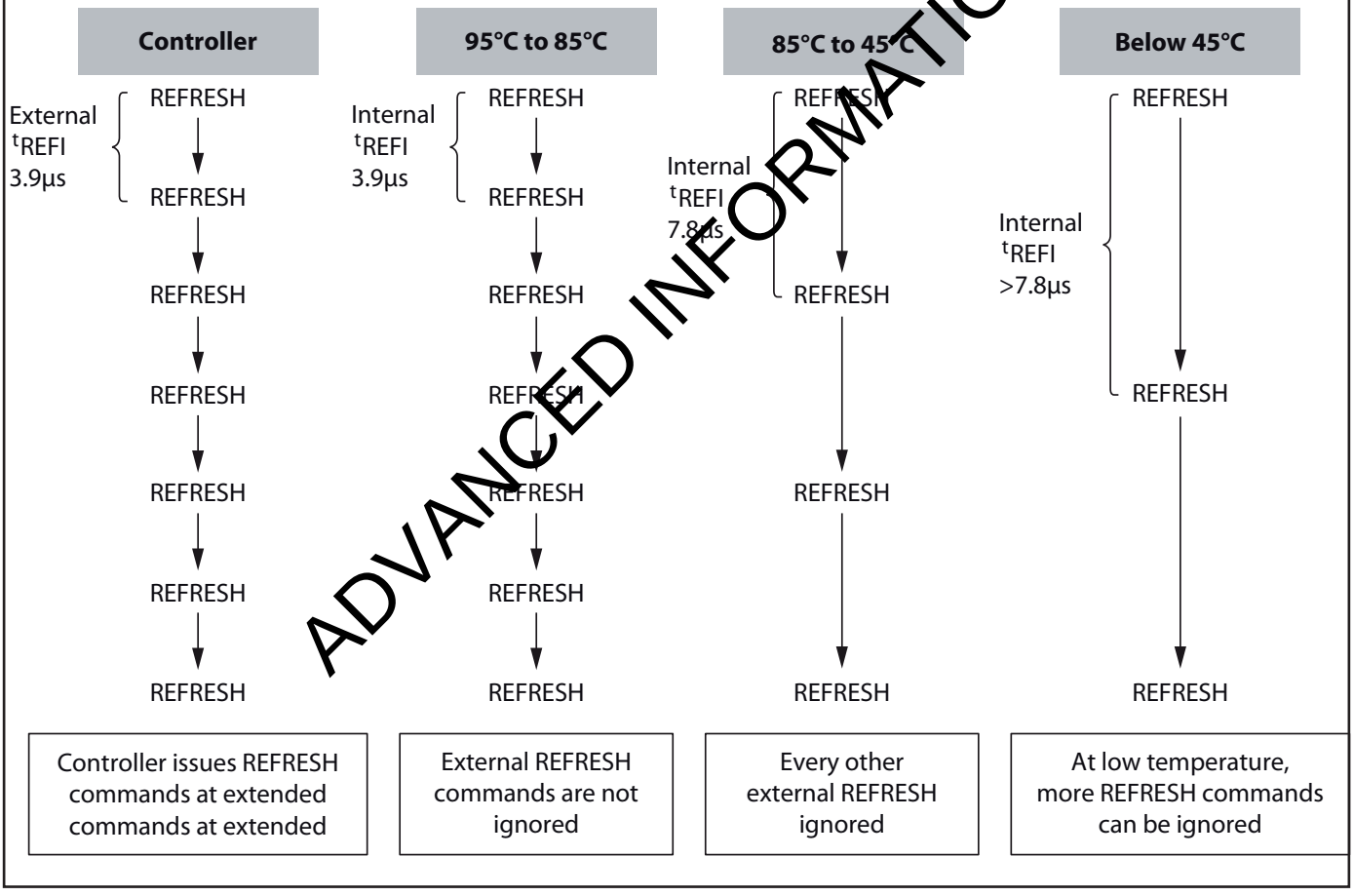
REFRESH commands should be issued to the device with the refresh period equal to or shorter than ^{t}REFI of extended temperature range (greater than 85°C). Even though the external refresh supports the extended temperature range, the device will adjust its internal refresh period to ^{t}REFI of the normal temperature range by skipping external REFRESH commands with proper gear ratio when operating in the normal temperature range (0°C to 85°C). The device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when TC is below 45°C. The internal refresh period is automatically adjusted inside the DRAM, and the DRAM controller does not need to provide any additional
control.

TABLE 116: NORMAL TREFI REFRESH (TCR ENABLED)

	Normal Temperature Range		Extended Temperature Range	
Temperature	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
T_C < 45°C	7.8µs	>> 7.8µs	3.9µs [1]	>> 7.8µs
45°C ≤ T_C < 85°C	7.8µs	7.8µs		7.8µs
85°C ≤ T_C < 95°C	N/A			3.9µs

Note: 1. If the external refresh period is 7.8µs, the device will refresh internally at half the listed refresh rate and will violate refresh specifications.

FIGURE 115: TCR MODE EXAMPLE[1]



Note: 1. TCR enabled with extended temperature range selected.

Fine Granularity Refresh Mode

Mode Register and Command Truth Table

The REFRESH cycle time (tRFC) and the average refresh interval (tREFI) can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle times and average refresh interval for the device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle times and average refresh interval for the device (on-the-fly mode [OTF]). OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

Table 117: MRS Definition

MR3[8]	MR3[7]	MR3[6]	Refresh Rate Mode
0	0	0	Normal mode (fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two OTF modes is selected, the device evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x and 2x (or 1x and 4x) modes, and then executes the corresponding REFRESH operation.

Table 118: REFRESH Command Truth Table

Refresh	CS_n	ACT_n	RAS_n/A15	CAS_n/A14	WE_n/A13	BG1	BG0	A10/AP	A[9:0], A[12:11], A[20:16]	MR3[8:6]
Fixed rate	L	H	L	L	H	V	V	V	V	0vv
OTF: 1x	L	H	L	L	H	V	L	V	V	1vv
OTF: 2x	L	H	L	L	H	V	H	V	V	101
OTF: 4x	L	H	L	L	H	V	H	V	V	110

tREFI and tRFC Parameters

The default refresh rate mode is fixed 1x mode where REFRESH commands should be issued with the normal rate; that is, tREFI1 = tREFI(base) (for TC ≤ 85°C), and the duration of each REFRESH command is the normal REFRESH cycle time (tRFC1). In 2x mode (either fixed 2x or OTF 2x mode), REFRESH commands should be issued to the device at the double frequency (tREFI2 = tREFI(base)/2) of the normal refresh rate. In 4x mode, the REFRESH command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, the tRFC parameter has different values as defined in the following table.

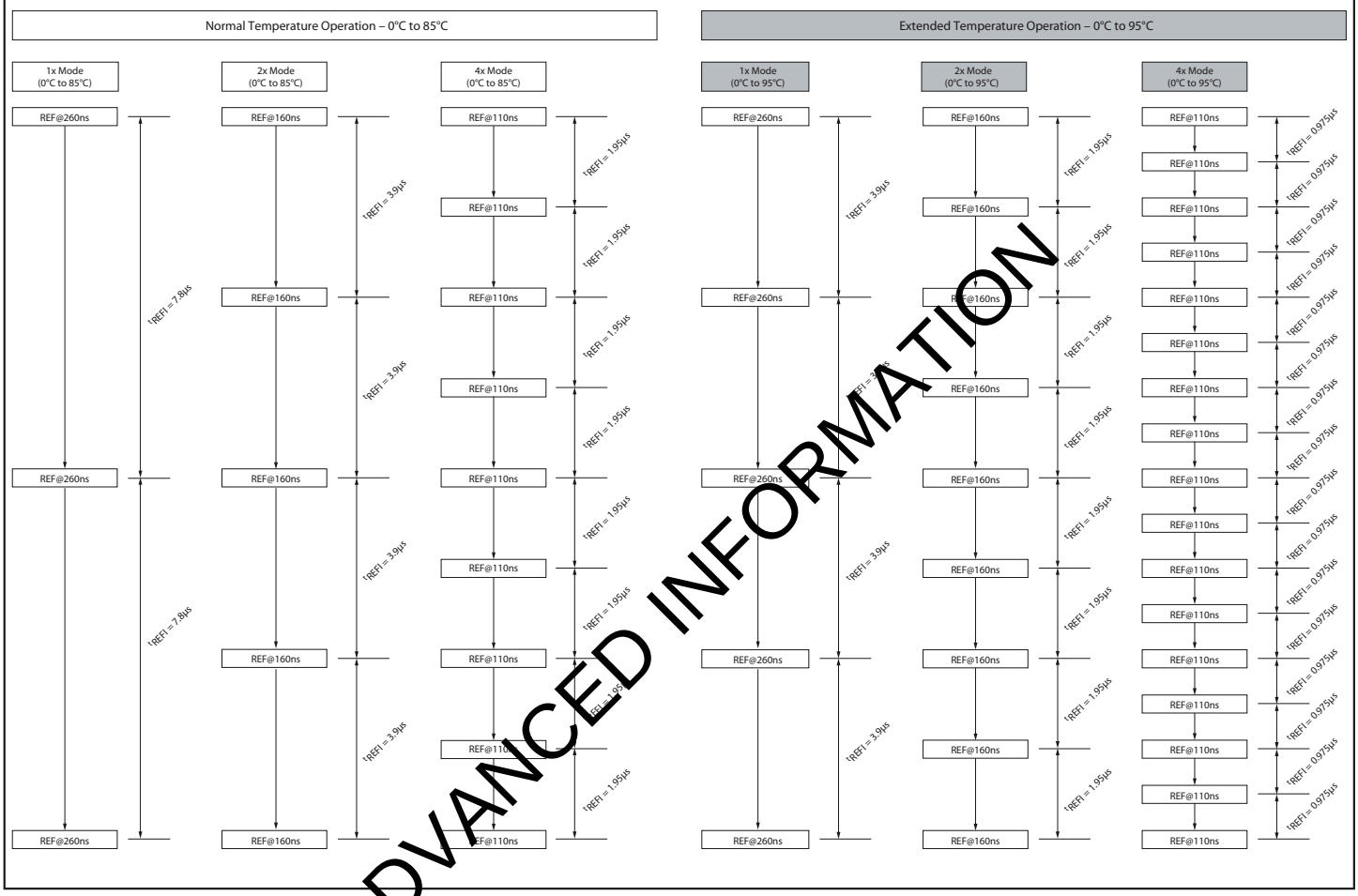
For discussion purposes, the REFRESH command that should be issued at the normal refresh rate and has the normal REFRESH cycle duration may be referred to as an REF1x command. The REFRESH command that should be issued at the double frequency (^{t}REFI2 = ^{t}REFI(base)/2) may be referred to as a REF2x command. Finally, the REFRESH command that should be issued at the quadruple rate (^{t}REFI4 = ^{t}REFI(base)/4) may be referred to as a REF4x command.

In the fixed 1x refresh rate mode, only REF1x commands are permitted. In the fixed 2x refresh rate mode, only REF2x commands are permitted. In the fixed 4x refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the OTF 1x/4x refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

TABLE 119: ^{T}REFI AND ^{T}RFC PARAMETERS

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Units
	^{t}REFI (base)		7.8	7.8	7.8	TBD	µs
1x mode	^{t}REFI1	0°C ≤ T_C ≤ 85°C	^{t}REFI(base)	^{t}REFI(base)	^{t}REFI(base)	^{t}REFI(base)	µs
		85°C ≤ T_C ≤ 95°C	^{t}REFI(base)/2	^{t}REFI(base)/2	^{t}REFI(base)/2	^{t}REFI(base)/2	µs
	^{t}RFC1		160	260	350	TBD	ns
2x mode	^{t}REFI20°C	0°C ≤ T_C ≤ 85°C	^{t}REFI(base)/2	^{t}REFI(base)/2	^{t}REFI(base)/2	^{t}REFI(base)/2	µs
		85°C ≤ T_C ≤ 95°C	^{t}REFI(base)/4	^{t}REFI(base)/4	^{t}REFI(base)/4	^{t}REFI(base)/4	µs
	^{t}RFC2		110	160	260	TBD	ns
4x mode	^{t}REFI40°C	0°C ≤ T_C ≤ 85°C	^{t}REFI(base)/4	^{t}REFI(base)/4	^{t}REFI(base)/4	^{t}REFI(base)/4	µs
		85°C ≤ T_C ≤ 95°C	^{t}REFI(base)/8	^{t}REFI(base)/8	^{t}REFI(base)/8	^{t}REFI(base)/8	µs
	^{t}RFC4		90	110	160	TBD	ns

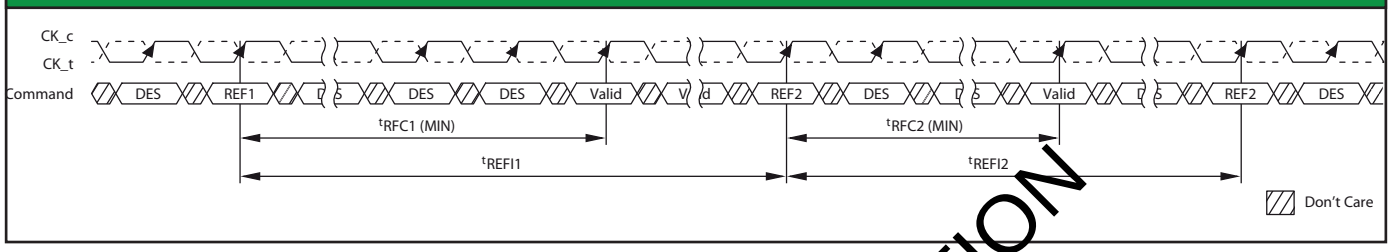
FIGURE 116: FINE GRANULARITY REFRESH MODE EXAMPLE



Changing Refresh Rate

If the refresh rate is changed by either MRS or OTF. New tREFI and tRFC parameters will be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, tREF1 and tRFC1 are applied from the time that the command was issued; when the REF2x command is issued, tREF2 and tRFC2 should be satisfied.

Figure 117: OTF REFRESH Command Timing



The following conditions must be satisfied before the refresh rate can be changed. Otherwise, data retention cannot be guaranteed.

- In the fixed 2x refresh rate mode or the OTF 1x/2x refresh mode, an even number of REF2x commands must be issued because the last change of the refresh rate mode with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/2x refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
- In the fixed 4x refresh rate mode or the OTF 1x/4x refresh mode, a multiple-of-four number of REF4x commands must be issued because the last change of the refresh rate with an MRS command before the refresh rate can be changed by another MRS command.
- In the OTF1x/4x refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x refresh rate mode. Switching between fixed and OTF modes keeping the same rate is not regarded as a refresh rate change.

Usage with TCR Mode

If the temperature controlled refresh mode is enabled, only the normal mode (fixed 1x mode, MR3[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

The device can enter self refresh mode anytime in 1x, 2x, and 4x mode without any restriction on the number of REFRESH commands that have been issued during the mode before the self refresh entry. However, upon self refresh exit, extra REFRESH com-mand(s) may be required, depending on the condition of the self refresh entry.

The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- In the fixed 2x refresh rate mode or the enable-OTF 1x/2x refresh rate mode, it is recommended there be an even number of REF2x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the refresh mode. If this condition is met, no additional REFRESH commands are

required upon self refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^{t}REFI).

- In the fixed 4x refresh rate mode or the enable-OTF 1x/4x refresh rate mode, it is recommended there be a multiple-of-four number of REF4x commands before entry into self refresh after the last self refresh exit, REF1x command, or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon self refresh exit. When this condition is not met, either one extra REF1x command or four extra REF4x commands must be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval (^{t}REFI).

There are no special restrictions on the fixed 1x refresh rate mode.

This section does not change the requirement regarding postponed REFRESH commands. The requirement for the additional REFRESH command(s) described above is independent of the requirement for the postponed REFRESH commands.

SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the device, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is defined by having CS_n, RAS_n, CAS_n, and CKE held LOW with WE_n and ACT_n HIGH at the rising edge of the clock.

Before issuing the SELF REFRESH ENTRY command, the device must be idle with all banks in the precharge state and tRP satisfied. Idle state is defined as: All banks are closed (^{t}RP, ^{t}DAL, and so on, satisfied), no data bursts are in progress, CKE is HIGH, and all timings from previous operations are satisfied (^{t}MRD, ^{t}MOD, ^{t}RFC, ^{t}ZQinit, ^{t}ZQoper, ^{t}ZQCS, and so on). After the SELF REFRESH ENTRY command is registered, CKE must be held LOW to keep the device in self refresh mode. The DRAM automatically disables ODT termination, regardless of the ODT pin, when it enters self refresh mode and automatically enables ODT upon exiting self refresh. During normal operation (DLL_on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL reset) upon exiting self refresh.

When the device has entered self refresh mode, all of the external control signals, except CKE and RESET_n, are "Don't Care." For proper SELF REFRESH operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{PP}, and V_{REFCA}) must be at valid levels. The DRAM internal VREFDQ generator circuitry may remain on or be turned off depending on the MRx bit Y setting. If the internal V_{REFDQ} circuit is on in self refresh, the first WRITE operation or first write-leveling activity may occur after ^{t}XS time after self refresh exit. If the DRAM internal V_{REFDQ} circuitry is turned off in self refresh, it ensures that the V_{REFDQ} generator circuitry is powered up and stable within the ^{t}XSDLL period when the DRAM exits the self refresh state. The first WRITE operation or first write-leveling activity may not occur earlier than ^{t}XSDLL after exiting self refresh. The device initiates a minimum of one REFRESH command internally within the ^{t}CKE period once it enters self refresh mode.

The clock is internally disabled during a SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is ^{t}CKESR/^{t}CKESR_PAR. The user may change the external clock frequency or halt the external clock ^{t}CKSRE/^{t}CKSRE_PAR after self refresh entry is registered; however, the clock must be restarted and tCKSRX must be stable before the device can exit SELF REFRESH operation.

The procedure for exiting self refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a SELF REFRESH EXIT command (SRX, combination of CKE going HIGH and DESELECT on the command bus) is registered, the following timing delay must be satisfied:

Commands that do not require locked DLL:

- ^{t}XS = ACT, PRE, PREA, REF, SRE, and PDE.
- ^{t}XS_FAST = ZQCL, ZQCS, and MRS commands. For an MRS command, only DRAM CL, WR/RTP register, and DLL reset in MR0; $R_{TT(NOM)}$ register in MR1; the CWL and $R_{TT(WR)}$ registers in MR2; and gear-down mode register in MR3; WRITE and READ preamble registers in MR4; $R_{TT(PARK)}$ register in MR5; ^{t}CCD_L/^{t}DLLK and V_{REFDQ} calibration value registers in MR6 may be accessed provided the DRAM is not in per-DRAM mode. Access to other DRAM mode registers must satisfy ^{t}XS timing. WRITE commands (WR, WRS4, WRS8, WRA, WRAS4, and WRAS8) that require synchronous ODT and dynamic ODT controlled by the WRITE command require a locked DLL.

Commands that require locked DLL in the normal operating range:

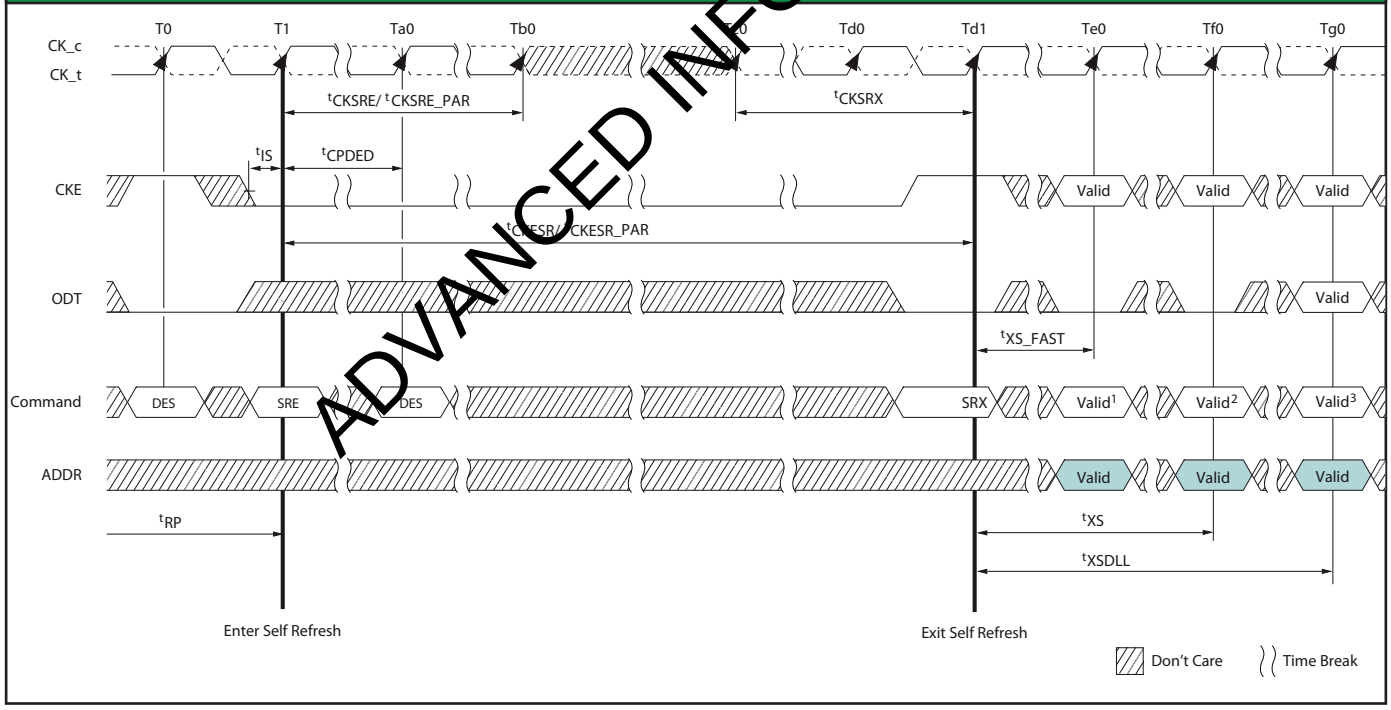
- tXSDLL – RD, RDS4, RDS8, RDA, RDAS4, and RDAS8 (unlike DDR3, WR, WRS4, WRS8, WRA, WRAS4, and WRAS8 because synchronous ODT is required).

Depending on the system environment and the amount of time spent in self refresh, ZQ CALIBRATION commands may be required to compensate for the voltage and temperature drift described in the ZQ CALIBRATION Commands section. To issue ZQ CALIBRATION commands, applicable timing requirements must be satisfied (see the ZQ Calibration Timing figure).

CKE must remain HIGH for the entire self refresh exit period tXSDLL for proper operation except for self refresh re-entry. Upon exit from self refresh, the device can be put back into self refresh mode or power-down mode after waiting at least tXS period and issuing one REFRESH command (refresh period of tRFC). The DESELECT command must be registered on each positive clock edge during the self refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from self refresh mode. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode.

FIGURE 118: SELF REFRESH ENTRY/EXIT TIMING



Notes:
1. Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

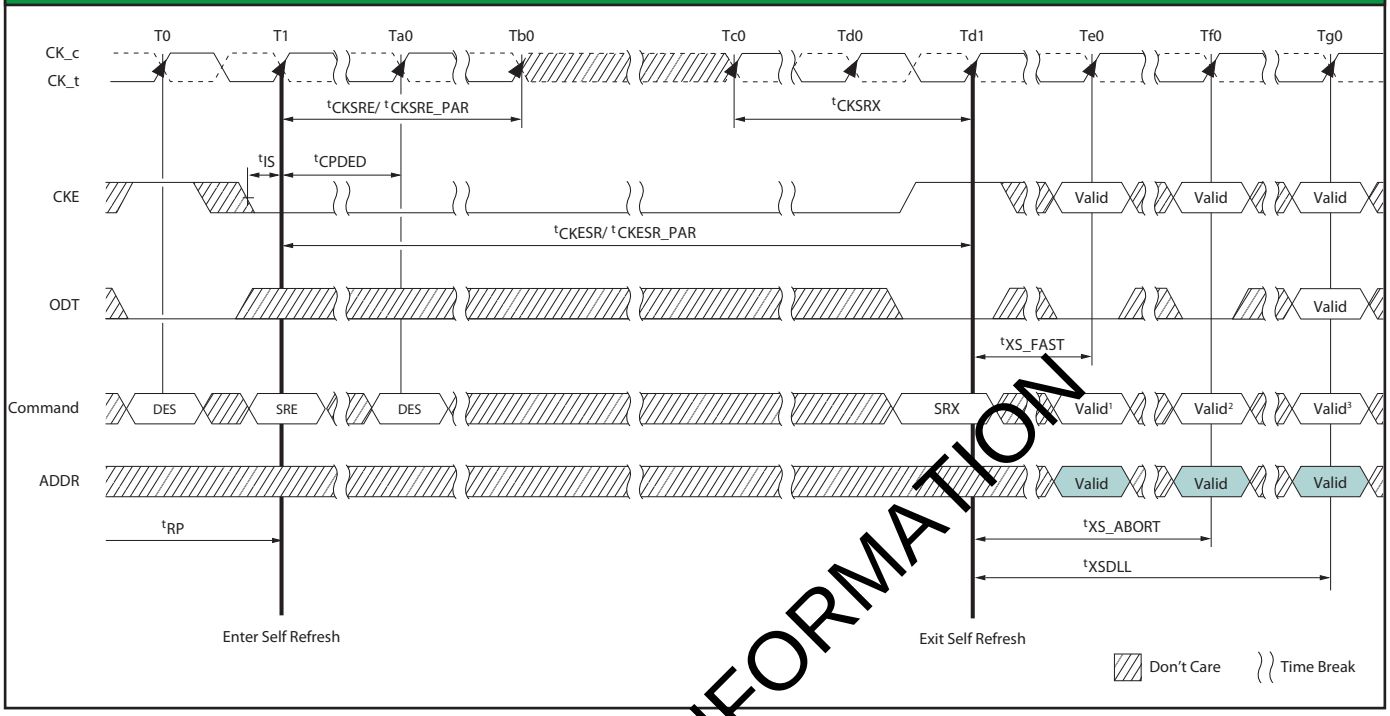
Figure 119: Self Refresh Entry/Exit Timing with CAL Mode

Notes:
1. tCAL = 3*n*CK, tCPDED = 4*n*CK, tCKSRE/tCKSRE_PAR = 8*n*CK, tCKSRX = 8*n*CK, tXS_FAST = tREFC4 (MIN) + 10ns.
2. CS_n = HIGH, ACT_n = "Don't Care," RAS_n/A16 = "Don't Care," CAS_n/A15 = "Don't Care," WE_n/A14 = "Don't Care."
3. 3. Only MRS (limited to those described in the SELF REFRESH Operations section), ZQCS, or ZQCL commands are allowed.

Self Refresh Abort

The exit timing from self refresh exit to the first valid command not requiring a locked DLL is tXS. The value of tXS is (tRFC + 10ns). This delay allows any refreshes started by the device time to complete. tRFC continues to grow with higher density devices, so tXS will grow as well. An MRS bit enables the self refresh abort mode. If the bit is disabled, the controller uses tXS timings (location MR4, bit 9). If the bit is enabled, the device aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_ABORT. Upon exit from self refresh, the device requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

FIGURE 120: SELF REFRESH ABORT



Notes:
1. Only MRS (limited to those described in the SELF REFRESH Operation section), ZQCS, or ZQCL commands are allowed.
2. Valid commands not requiring a locked DLL with self refresh abort mode enabled in the mode register.
3. Valid commands requiring a locked DLL.

Self Refresh Exit with NOP Command

Exiting self refresh mode using the NO OPERATION command (NOP) is allowed under a specific system application. This special use of NOP allows for a common command/address bus between active DRAM devices and DRAM(s) in maximum power saving mode. Self refresh mode may exit with NOP commands provided:

- The device entered self refresh mode with CA parity and CAL disabled.
- tMPX_S and tMPX_LH are satisfied.
- NOP commands are only issued during tMPX_LH window.

No other command is allowed during the tMPX_LH window after an SELF REFRESH EXIT (SRX) command is issued.

FIGURE 121: SELF REFRESH EXIT WITH NOP COMMAND

Power-Down Mode

Power-down is synchronously entered when CKE is registered LOW (along with a DESELECT command). CKE is not allowed to go LOW when the following operations are in progress: MRS command, MPR operations, ZQCAL operations, DLL locking, or READ/ WRITE operations. CKE is allowed to go LOW while any other operations, such as ROW ACTIVATION, PRECHARGE or auto precharge, or REFRESH, are in progress, but the power-down IDD specification will not be applied until those operations are complete. The timing diagrams that follow illustrate power-down entry and exit.

For the fastest power-down exit timing, the DLL should be in a locked state when power-down is entered. If the DLL is not locked during power-down entry, the DLL must bereset after exiting power-down mode for proper READ operation and synchronous ODToperation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as the controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode; if any bank is open after inprogress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on MRx bit Y. If it is configured to 0b, the ODT input buffer remains on and the ODT input signal must be at valid logic level. If it is configured to 1b, the ODT input buffer is deactivated and the DRAM ODT input signal may be floating and the device does not provide $R_{TT(NOM)}$ termination. Note that the device continues to provide $R_{TT(Park)}$ termination if it is enabled in the mode register MRa bit B. To protect internal delay on the CKE line to block the input signals, multiple DES commands are needed during the CKE switch off and on cycle(s); this timing period is defined as tCPDED. CKE LOW will result in deactivation of command and address receivers after tCPDED has expired.

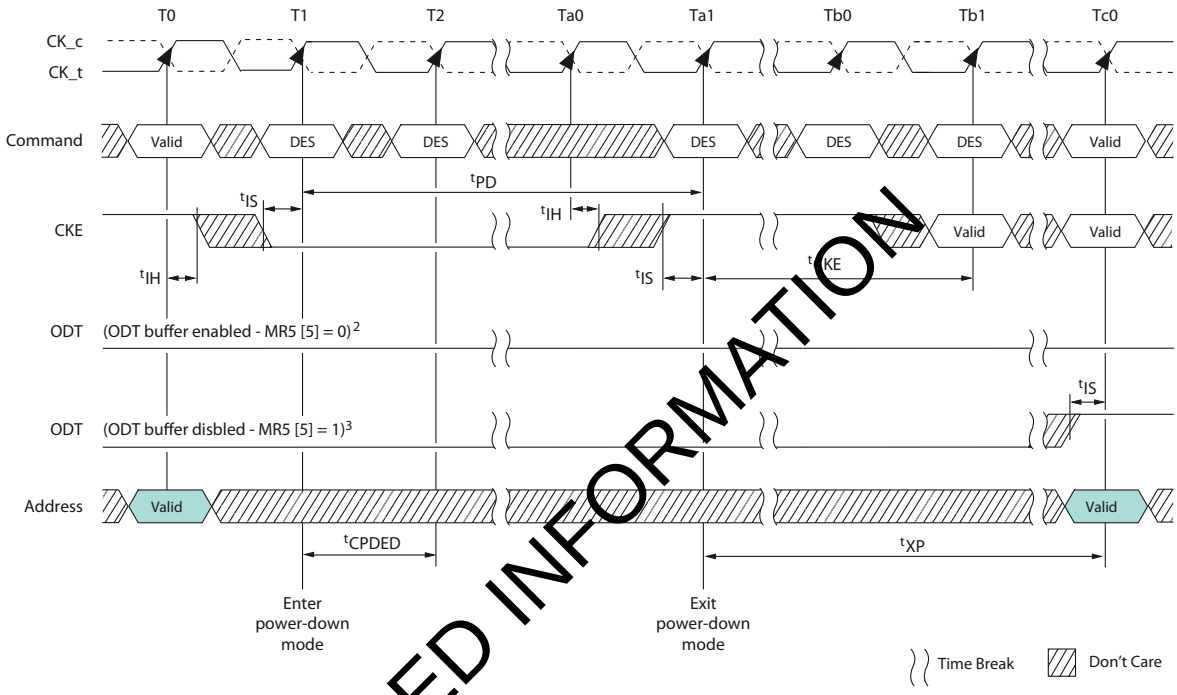
TABLE 120: POWER-DOWN ENTRY DEFINITIONS

DRAM Status	DLL	Power-Down Exit	Relevant Parameters
Active (a bank or more open)	On	Fast	tXP to any valid command.
Precharged (all banks precharged)	On	Fast	tXP to any valid command.

The DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE is LOW, RESET_n is HIGH, and a stable clock signal must be maintained at the inputs of the device. ODT should be in a valid state, but all other input signals are “Don’t Care.” (If RESET_n goes LOW during power-down, the device will be out of power-down mode and in the reset state.) CKE LOW must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 × tREFI.

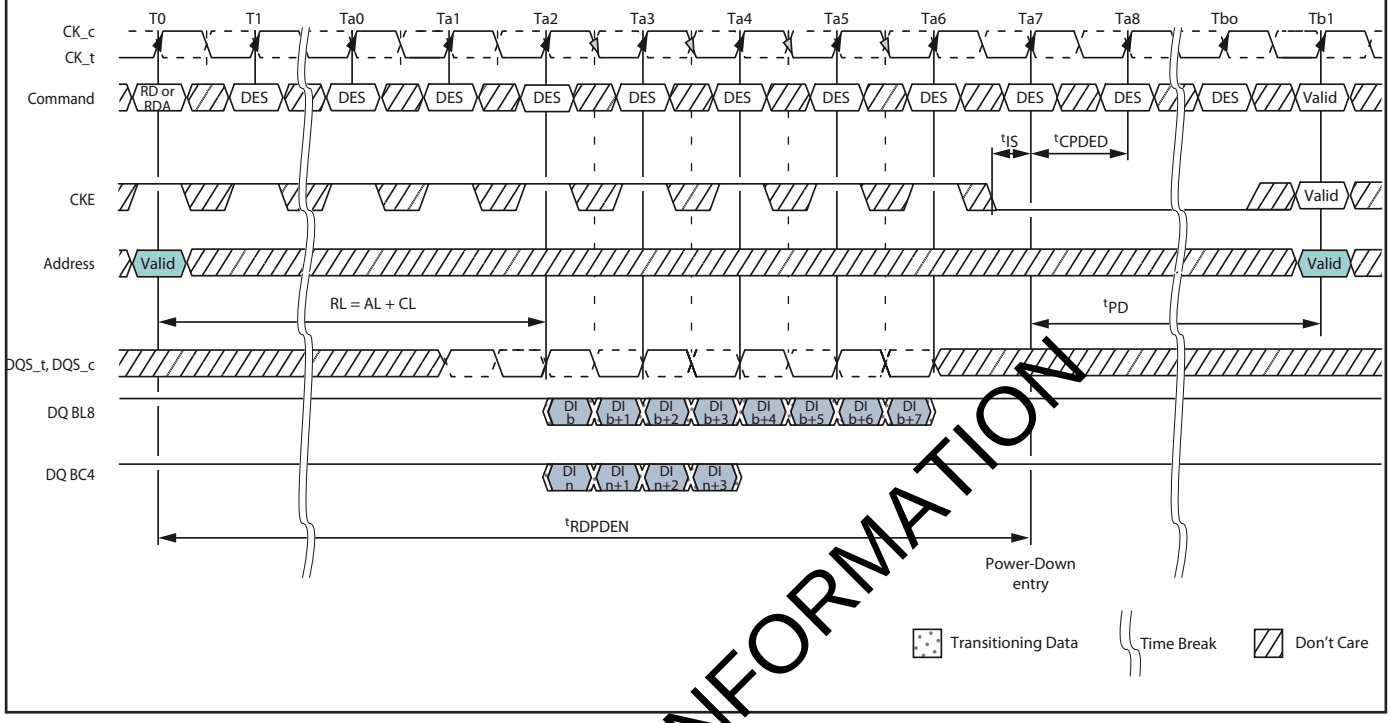
The power-down state is synchronously exited when CKE is registered HIGH (along with DES command). CKE HIGH must be maintained until tCKE has been satisfied. The ODT input signal must be at a valid level when the device exits from power-down mode, independent of MRx bit Y if $R_{TT(NOM)}$ is enabled in the mode register. If $R_{TT(NOM)}$ is dis-abled, the ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP, and/or tXPDLL after CKE goes HIGH. Powerdown exit latency is defined in the AC Specifications table.

FIGURE 122: ACTIVE POWER-DOWN ENTRY AND EXIT



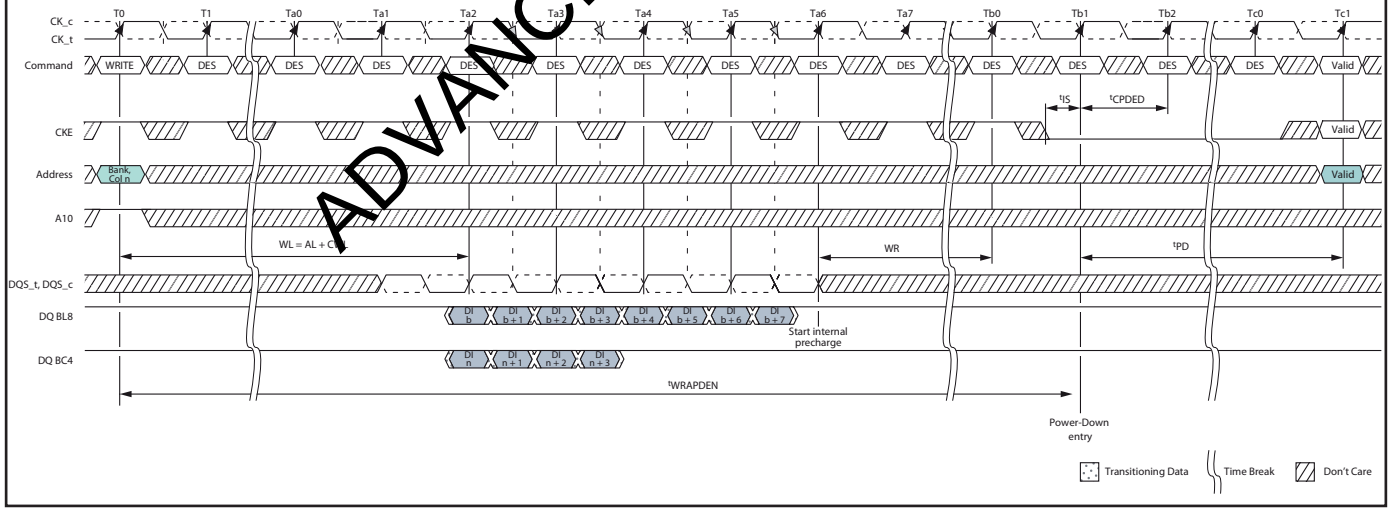
Notes:
1. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.
2. ODT pin driven to a valid state; MR5[5] = 0 (normal setting).
3. ODT pin driven to a valid state; MR5[5] = 1.

FIGURE 123: POWER-DOWN ENTRY AFTER READ AND READ WITH AUTO PRECHARGE



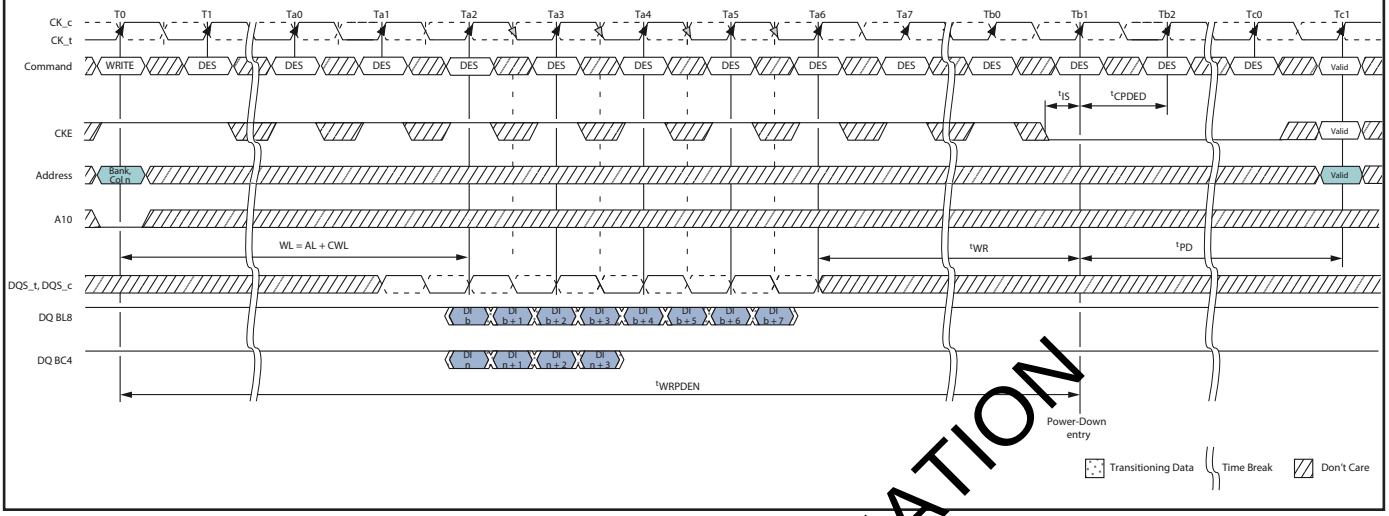
Note: 1. DI n (or b) = data-in from column n (or b).

FIGURE 124: POWER-DOWN ENTRY AFTER WRITE AND WRITE WITH AUTO PRECHARGE



Notes: 1. DI n (or b) = data-in from column n (or b).
2. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.

Figure 125: Power-Down Entry After Write



Note: 1. DI n (or b) = data-in from column n (or b).

Figure 126: Precharge Power-Down Entry and Exit

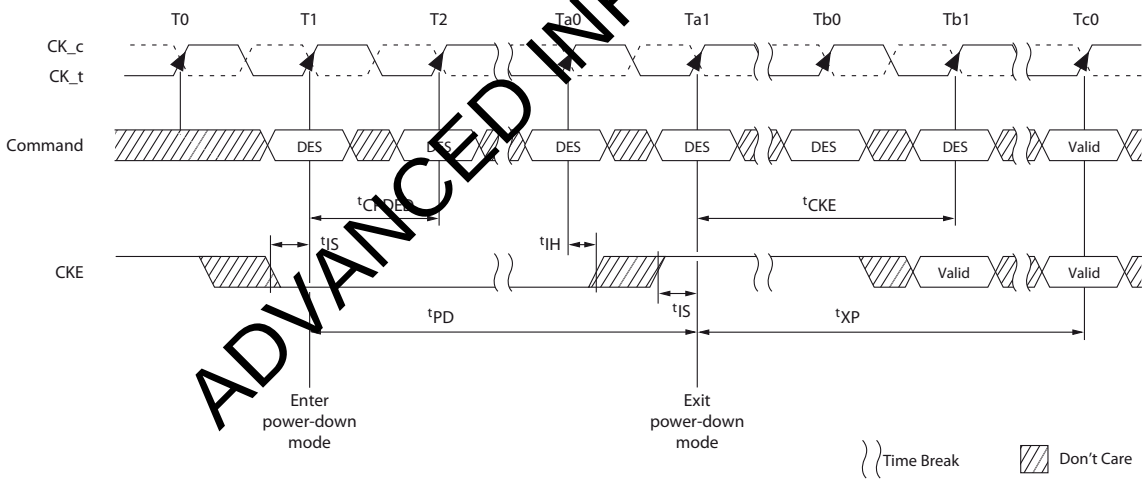


FIGURE 127: REFRESH COMMAND TO POWER-DOWN ENTRY

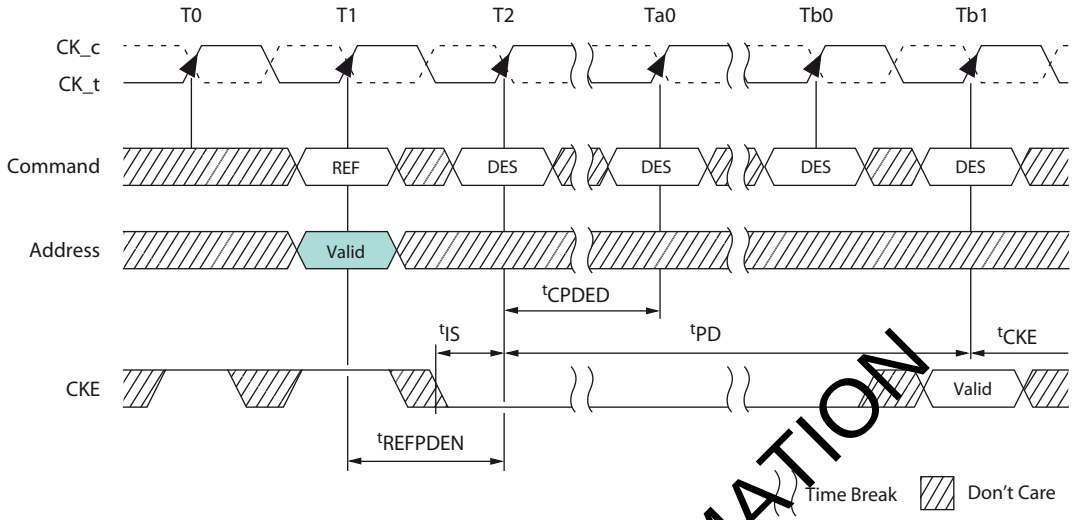


FIGURE 128: ACTIVE COMMAND TO POWER-DOWN ENTRY

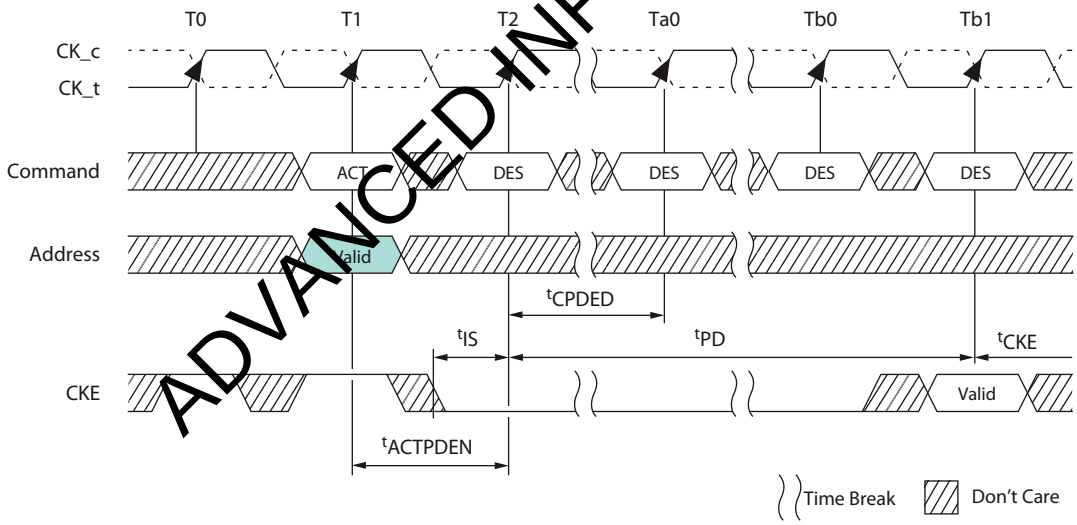


Figure 129: PRECHARGE/PRECHARGE ALL Command to Power Down Entry

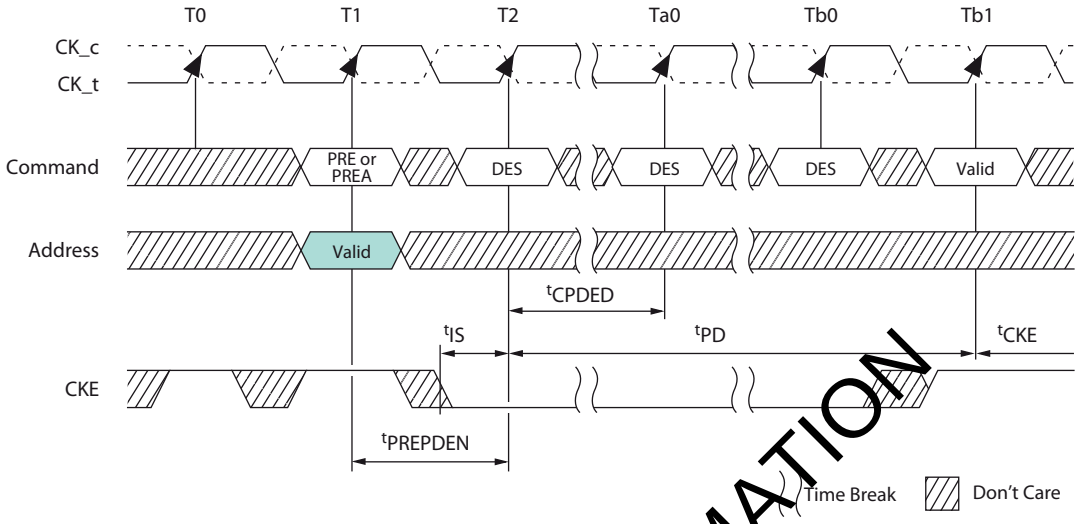
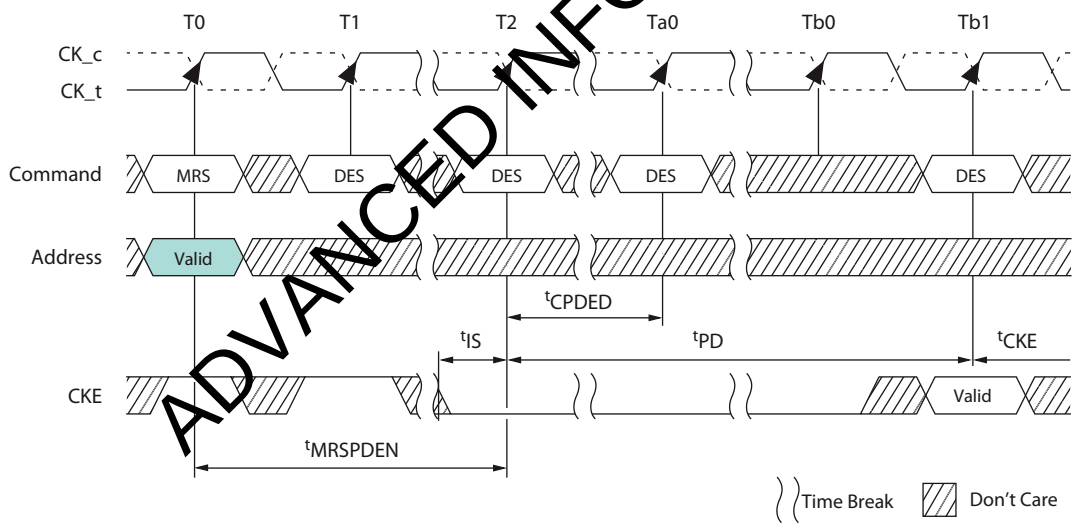


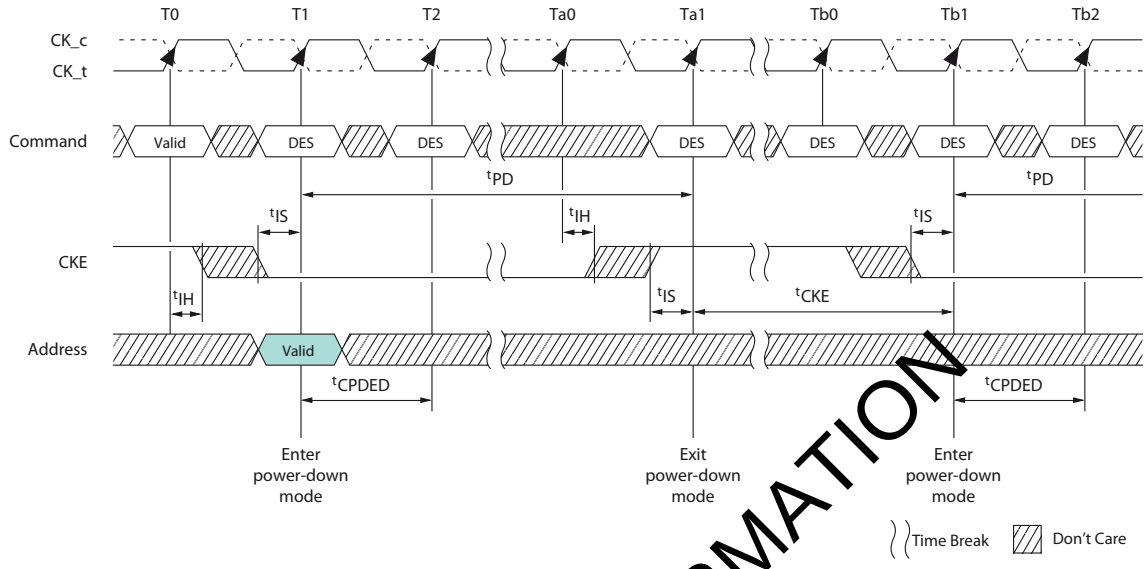
Figure 130: MRS Command to Power-Down Entry



Power-Down Clarifications - Case 1

When CKE is registered LOW for power-down entry, tPD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter tPD (MIN) is equal to the minimum value of parameter tCKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 follows.

Figure 131: Power-Down Entry/Exit Clarifications - Case 1



Power-Down Entry, Exit Timing with CAL

Command/Address latency is used and additional timing restrictions are required when entering power-down, as noted in the following figures.

FIGURE 132: ACTIVE POWER-DOWN ENTRY AND EXIT TIMING WITH CAL

FIGURE 133: REFRESH COMMAND TO POWER-DOWN ENTRY WITH CAL

ODT Input Buffer Disable Mode for Power-Down

ODT Input Buffer Disable Mode for Power-Down

ODT input buffer disable mode, when enabled via MR5[5], will prevent the device from providing $R_{TT(NOM)}$ termination during power-down for additional power savings.

The internal delay on the CKE path to disable the ODT buffer and block the sampled output must be accounted for; therefore, ODT must be continuously driven to a valid level, either LOW or HIGH, when entering power-down. However, after ^{t}CPDED (MIN) has been satisfied, the ODT signal may float.

When ODT input buffer disable mode is enabled, $R_{TT(NOM)}$ termination corresponding to sampled ODT after CKE is first registered LOW (and ^{t}ANPD before that) may not be provided. ^{t}ANPD is equal to (WL - 1) and is counted backward from PDE, with CKE registered LOW.

Figure 134: ODT Power-Down Entry with ODT Buffer disable Mode

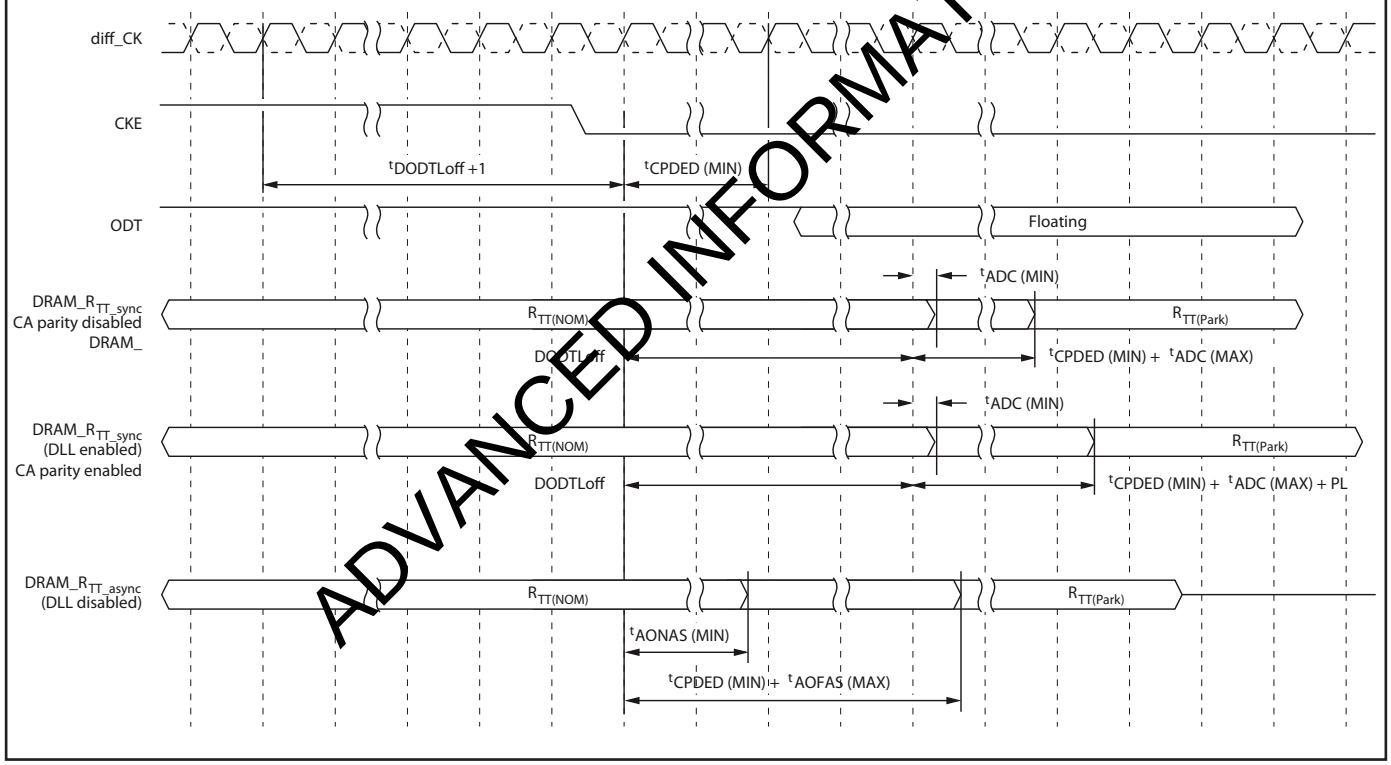
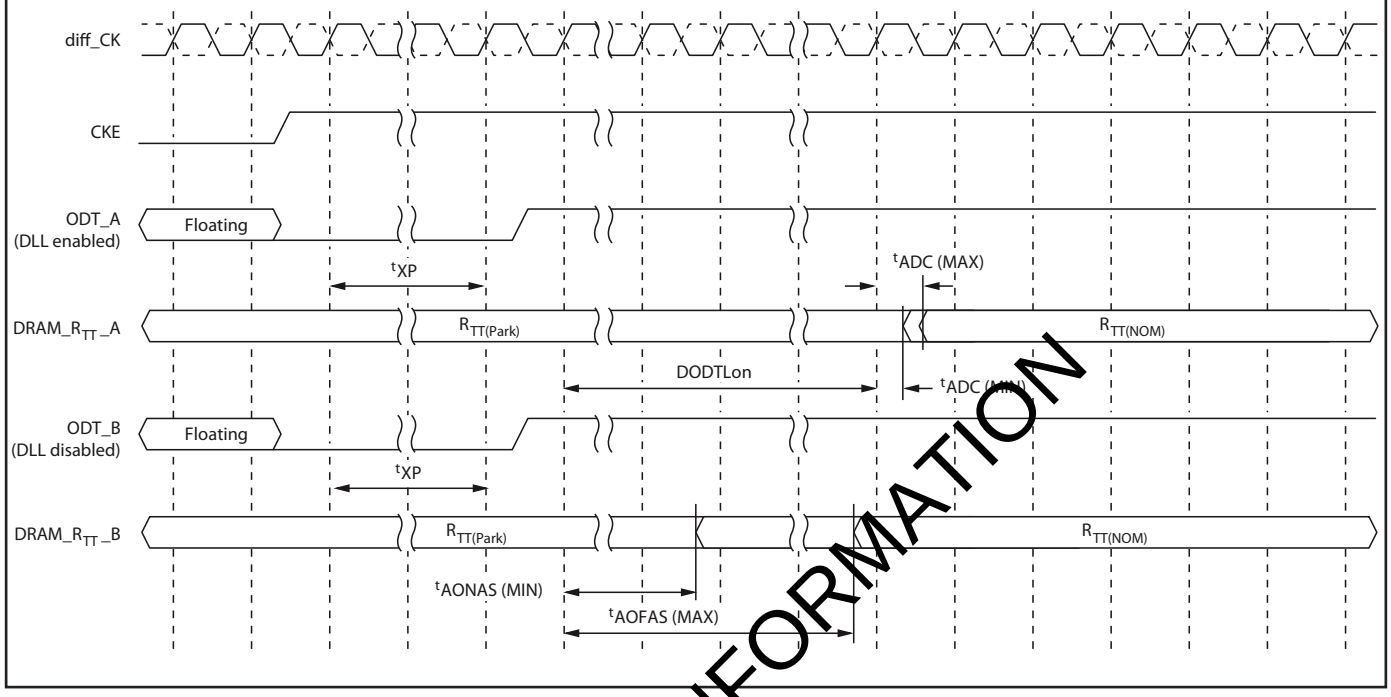


Figure 135: ODT Power-Down Exit with ODT Buffer disable Mode

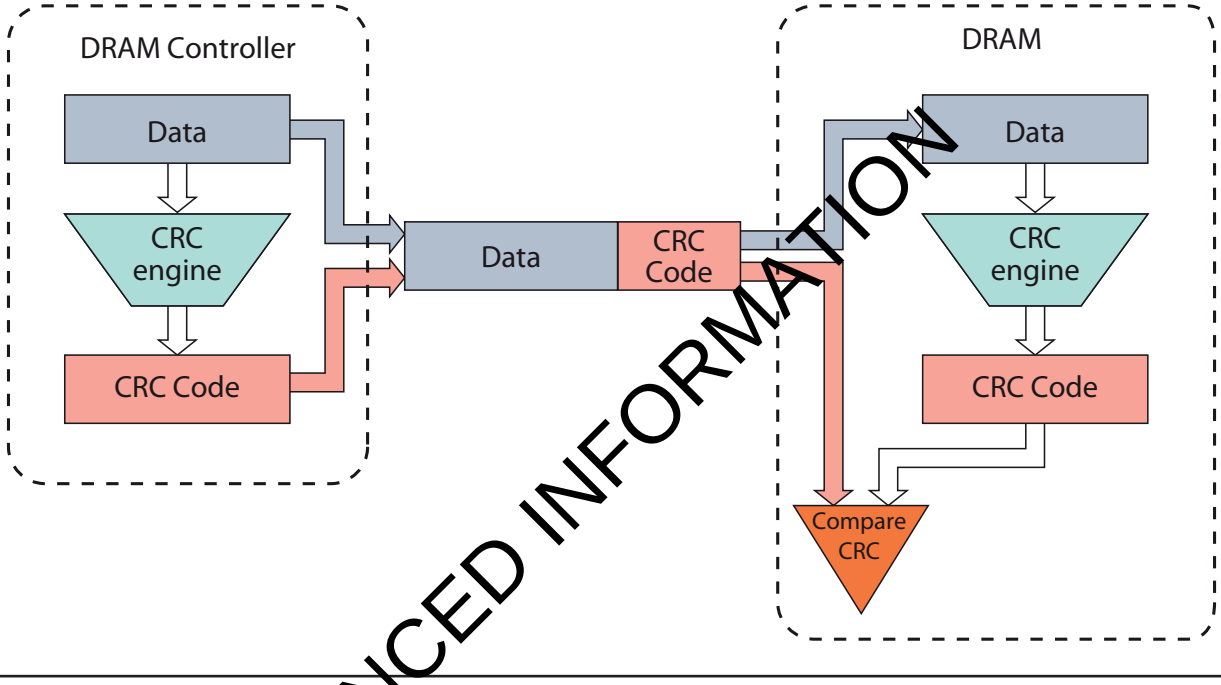


CRC Write Data Feature

CRC Write Data

The CRC write data feature takes the CRC generated data from the DRAM controller and compares it to the internally CRC generated data and determines whether the two match (no CRC error) or do not match (CRC error).

FIGURE 136: CRC WRITE DATA OPERATION



WRITE CRC DATA Operation

A DRAM controller generates a CRC checksum using a 72-bit CRC tree and forms the write data frames, as shown in the following CRC data mapping tables. The device has two identical CRC trees each, one for the lower byte and one for the upper byte, with 64 input data bits used by each, and the remaining upper 8 bits on each byte dependant upon whether DM_n/DBI_n is used (1s are sent when not used). The memory controller must send 1s in transfer 9 location whether or not DM_n/DBI_n is used.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mismatch. The DRAM can write data to the DRAM core without waiting for the CRC check for full writes when DM is disabled. If bad data is written to the DRAM core, the DRAM memory controller will try to overwrite the bad data with good data; this means the DRAM controller is responsible for data coherency when DM is disabled. However, in the case where both CRC and DM are enabled via MRS (that is, persistent mode), the DRAM will not write bad data to the core when a CRC error is detected.

DBI_n and CRC Both Enabled

The DRAM computes the CRC for received written data D[71:0]. Data is not inverted back based on DBI before it is used for computing CRC. The data is inverted back based on DBI before it is written to the DRAM core.

DM_n and CRC Both Enabled

When both DM and write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the WRITE operation and discards the data. The *Nonconsecutive WRITE (BL8/BC4-OTF) with 2tCK Preamble and Write CRC in Same or Different Bank Group and the WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different BankGroup* figures in the WRITE Operation section show timing differences when DM is enabled.

DM_n and DBI_n Conflict During Writes with CRC Enabled

Both write DBI_n and DM_n can not be enabled at the same time; read DBI_n and DM_n can be enabled at the same time.

CRC and Write Preamble Restrictions

When write CRC is enabled:

- And 1^{t}CK WRITE preamble mode is enabled, a ^{t}CCD_S or ^{t}CCD_L of 4 clocks is not allowed.
- And 2^{t}CK WRITE preamble mode is enabled, a ^{t}CCD_S or ^{t}CCD_L of 6 clocks is not allowed.

CRC Simultaneous Operation Restrictions

When write CRC is enabled, neither MPR writes nor per-DRAM mode is allowed.

CRC Polynomial

The CRC polynomial used by DDR4 is the ATM-8 HEC, X8 + X2 + X1 + 1.

A combinatorial logic block implementation of this 8-bit CRC for 72 bits of data in-cludes 272 two-input XOR gates contained in eight 6-XOR-gate-deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

The error coverage from the DDR4 polynomial used is shown in the following table.

TABLE 121: CRC ERROR DETECTION COVERAGE

Error Type	Detection Capability
Random single-bit errors	100%
Random double-bit errors	100%

Table 121: CRC Error Detection Coverage (Continued)

Error Type	Detection Capability
Random odd count errors	100%
Random multibit UI vertical column error detection excluding DBI bits	100%

CRC Combinatorial Logic Equations

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;
```

CRC[0] =
D[69]^D[68]^D[67]^D[66]^D[64]^D[63]^D[60]^D[56]^D[54]^D[53]^D[52]^D[50]^D[49]^D[48]^D[45]^D[43]^D[40]^D[39]^D[35]^D[34]^D[31]^D[30]^D[28]^D[23]^D[21]^D[19]^D[18]^D[16]^D[14]^D[12]^D[8]^D[7]^D[6]^D[0] ;

CRC[1] =
D[70]^D[66]^D[65]^D[63]^D[61]^D[60]^D[57]^D[56]^D[55]^D[52]^D[51]^D[48]^D[46]^D[45]^D[44]^D[43]^D[41]^D[39]^D[36]^D[34]^D[32]^D[30]^D[29]^D[28]^D[24]^D[23]^D[22]^D[21]^D[20]^D[18]^D[17]^D[16]^D[15]^D[14]^D[13]^D[12]^D[9]^D[6]^D[1]^D[0];

CRC[2] =
D[71]^D[69]^D[68]^D[63]^D[62]^D[61]^D[60]^D[58]^D[57]^D[54]^D[50]^D[48]^D[47]^D[46]^D[44]^D[43]^D[42]^D[39]^D[37]^D[34]^D[33]^D[29]^D[28]^D[25]^D[24]^D[22]^D[17]^D[15]^D[13]^D[12]^D[10]^D[8]^D[6]^D[2]^D[1]^D[0];

CRC[3] =
D[70]^D[69]^D[64]^D[63]^D[62]^D[61]^D[59]^D[58]^D[55]^D[51]^D[49]^D[48]^D[47]^D[45]^D[44]^D[43]^D[40]^D[38]^D[35]^D[34]^D[30]^D[29]^D[26]^D[25]^D[23]^D[18]^D[16]^D[14]^D[13]^D[11]^D[9]^D[7]^D[3]^D[2]^D[1];

CRC[4] =
D[71]^D[70]^D[65]^D[64]^D[63]^D[62]^D[60]^D[59]^D[56]^D[52]^D[50]^D[49]^D[48]^D[46]^D[45]^D[44]^D[41]^D[39]^D[36]^D[35]^D[31]^D[30]^D[27]^D[26]^D[24]^D[19]^D[17]^D[15]^D[14]^D[12]^D[10]^D[8]^D[4]^D[3]^D[2];

CRC[5] =
D[71]^D[66]^D[65]^D[64]^D[63]^D[61]^D[60]^D[57]^D[53]^D[51]^D[50]^D[49]^D[47]^D[46]^D[45]^D[42]^D[40]^D[37]^D[36]^D[32]^D[31]^D[28]^D[27]^D[25]^D[20]^D[18]^D[16]^D[15]^D[13]^D[11]^D[9]^D[5]^D[4]^D[3];

CRC[6] =
D[67]^D[66]^D[65]^D[64]^D[62]^D[61]^D[58]^D[54]^D[52]^D[51]^D[50]^D[48]^D[47]^D[46]^D[43]^D[41]^D[38]^D[37]^D[33]^D[32]^D[29]^D[28]^D[26]^D[21]^D[19]^D[17]^D[16]^D[14]^D[12]^D[10]^D[6]^D[5]^D[4];

CRC[7] =
D[68]^D[67]^D[66]^D[65]^D[63]^D[62]^D[59]^D[55]^D[53]^D[52]^D[51]^D[49]^D[48]^D[47]^D[44]^D[42]^D[39]^D[38]^D[34]^D[33]^D[30]^D[29]^D[27]^D[22]^D[20]^D[18]^D[17]^D[15]^D[13]^D[11]^D[7]^D[6]^D[5];

nextCRC8_D72 = CRC;

Burst Ordering for BL8

DDR4 supports fixed WRITE burst ordering [A2:A1:A0 = 0:0:0] when write CRC is enabled in BL8 (fixed).

CRC Data Bit Mapping

The x16 die are treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].

Table 122: CRC Data Mapping for BL8

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
LDM_n/ LDBI_n	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
UDM_n/ UD_n	D136	D137	D138	D139	D140	D141	D142	D143	1	1

CRC Enabled With BC4

If CRC and BC4 are both enabled, then address bit A2 is used to transfer critical data first for BC4 writes.

CRC with BC4 Data Bit Mapping

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

When A2 = 0, input bits D[67:64] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[139:136] are 1s.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[143:140] are 1s.

Table 123: CRC Data Mapping for BC4

	Transfer									
Function	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
A2 = 0										
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
LDM_n/LDBI_n	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
UDM_n/UDBI_n	D136	D137	D138	D139	1	1	1	1	1	1
A2 = 1										
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D0	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
LDM_n/LDBI_n	D68	D69	D70	D71	1	1	1	1	1	1

TABLE 123: CRC DATA MAPPING FOR BC4 (CONTINUED)

Function	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
UDM_n/UDBI_n	D140	D141	D142	D143	1	1	1	1	1	1

CRC Equations for x8 Device in BC4 Mode with A2 = 0 and A2 = 1

The following example is of a CRC tree when x8 is used in BC4 mode (x4 and x16 CRC trees have similar differences).

CRC[0], A2=0 =
1^1^D[67]^D[66]^D[64]^1^1^D[56]^1^1^1^D[50]^D[49]^D[48]^1^D[43]^D[40]^1^D[35]^D[34]^1^1^1^1^1^D[19]^D[18]^D[16]^1^1^D[8] ^1^1^ D[0] ;
CRC[0], A2=1 =
1^1^D[71]^D[70]^D[68]^1^1^D[60]^1^1^1^D[54]^D[53]^D[52]^1^D[47]^D[44]^1^D[39]^D[38]^1^1^1^1^1^D[23]^D[22]^D[20]^1^1^D[12]^1^1^D[4] ;

CRC[1], A2=0 =
1^D[66]^D[65]^1^1^1^D[57]^D[56]^1^1^D[51]^D[48]^1^1^1^D[43]^D[41]^1^1^D[34]^D[32]^1^1^1^D[24]^1^1^1^D[18]^D[17]^D[16]^1^1^1^1^D[9] ^1^ D[1]^D[0];
CRC[1], A2=1 =
1^D[70]^D[69]^1^1^1^D[61]^D[60]^1^1^D[55]^D[52]^1^1^1^D[47]^D[45]^1^1^D[38]^D[36]^1^1^1^D[28]^1^1^1^1^D[22]^D[21]^D[20]^1^1^1^1^D[13]^1^D[5]^D[4];

CRC[2], A2=0 =
1^1^1^1^1^1^1^D[58]^D[57]^1^D[50]^D[48]^1^1^1^D[43]^D[42]^1^1^D[34]^D[33]^1^1^D[25]^D[24]^1^D[17]^1^1^1^D[10]^D[8] ^1^D[2]^D[1]^D[0];
CRC[2], A2=1 =
1^1^1^1^1^1^1^D[62]^D[61]^1^D[54]^D[52]^1^1^1^D[47]^D[46]^1^1^D[38]^D[37]^1^1^D[29]^D[28]^1^D[21]^1^1^1^D[14]^D12]^1^D[6]^D[5]^D[4];

CRC[3], A2=0 =
1^1^D[64]^1^1^1^D[59]^D[58]^1^D[51]^D[49]^D[48]^1^1^1^D[43]^D[40]^1^D[35]^D[34]^1^1^D[26]^D[25]^1^D[18]^D[16]^1^1^D[11]^D[9] ^1^D[3]^D[2]^D[1];
CRC[3], A2=1 =
1^1^D[68]^1^1^1^D[63]^D[62]^1^D[55]^D[53]^D[52]^1^1^1^D[47]^D[44]^1^D[39]^D[38]^1^1^D[30]^D[29]^1^D[22]^D[20]^1^1^D[15]^D[13]^1^D[7]^D[6]^D[5];

CRC[4], A2=0 =
1^1^D[65]^D[64]^1^1^1^D[59]^D[56]^1^D[50]^D[49]^D[48]^1^1^1^D[41]^1^1^D[35
]^1^1^D[27]^D[26]^D[24]^D[19]^D[17]^1^1^1^D[10]^D[8] ^1^D[3]^D[2];
CRC[4], A2=1 =
1^1^D[69]^D[68]^1^1^1^D[63]^D[60]^1^D[54]^D[53]^D[52]^1^1^1^D[45]^1^1^D[39
]^1^1^D[31]^D[30]^D[28]^D[23]^D[21]^1^1^1^D[14]^D[12]^1^D[7]^D[6];

CRC[5], A2=0 =
1^D[66]^D[65]^D[64]^1^1^1^D[57]^1^D[51]^D[50]^D[49]^1^1^1^D[42]^D[40]^1^1^
D[32]^1^1^D[27]^D[25]^1^D[18]^D[16]^1^1^D[11]^D[9] ^1^1^D[3];
CRC[5], A2=1 =
1^D[70]^D[69]^D[68]^1^1^1^D[61]^1^D[55]^D[54]^D[53]^1^1^1^D[46]^D[44]^1^1^
D[36]^1^1^D[31]^D[29]^1^D[22]^D[20]^1^1^D[15]^D[13]^1^1^D[7];

CRC[6], A2=0 =
D[67]^D[66]^D[65]^D[64]^1^1^D[58]^1^1^D[51]^D[50]^D[48]^1^1^D[43]^D[41]^1^1
^D[33]^D[32]^1^1^D[26]^1^D[19]^D[17]^D[16]^1^1^D[10]^1^1^1;
CRC[6], A2=1 =
D[71]^D[70]^D[69]^D[68]^1^1^D[62]^1^1^D[55]^D[54]^D[53]^1^1^D[47]^D[45]^1^1
^D[37]^D[36]^1^1^D[30]^1^D[23]^D[21]^D[20]^1^1^D[14]^1^1^1;

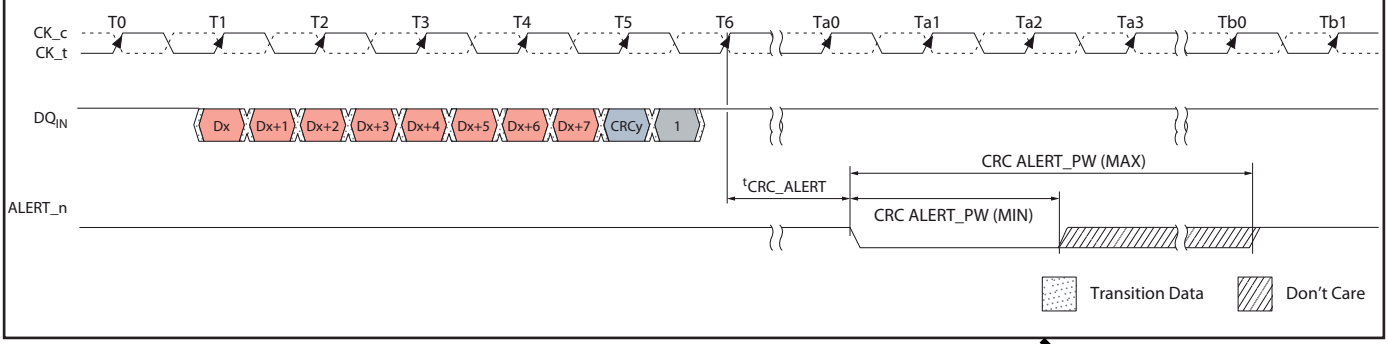
CRC[7], A2=0 =
1^D[67]^D[66]^D[65]^1^1^D[59]^1^1^1^D[51]^D[49]^D[48]^1^1^D[42]^1^1^D[34]^
D[33]^1^1^D[27]^1^1^D[18]^D[17]^1^1^D[11]^1^1^1;
CRC[7], A2=1 =
1^D[71]^D[70]^D[69]^1^1^D[63]^1^1^1^D[55]^D[53]^D[52]^1^1^D[46]^1^1^D[38]^
D[37]^1^1^D[31]^1^1^D[22]^D[21]^1^1^D[15]^1^1^1;

CRC Error Handling

The CRC error mechanism shares the same ALERT_n signal as CA parity for reporting write errors to the DRAM. The controller has two ways to distinguish between CRC errors and CA parity errors: 1) Read DRAM mode/MPR registers, and 2) Measure time ALERT_n is LOW. To speed up recovery for CRC errors, CRC errors are only sent back as a “short” pulse; the maximum pulse width is roughly ten clocks (unlike CA parity where ALERT_n is LOW longer than 45 clocks). The ALERT_n LOW could be longer than the maximum limit at the controller if there are multiple CRC errors as the ALERT_n signals are connected by a daisy chain bus. The latency to ALERT_n signal is defined as tCRC_ALERT in the following figure.

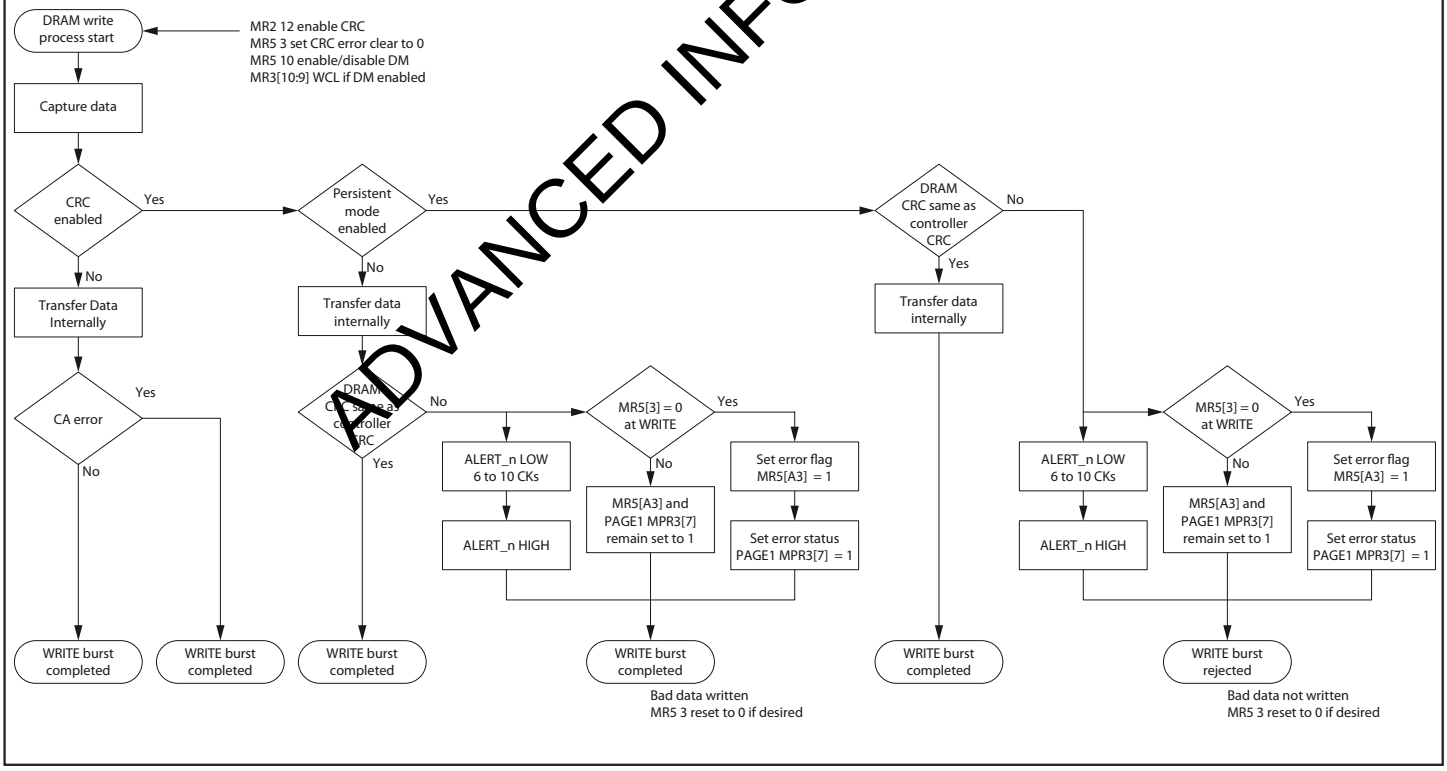
The DRAM will set the error status bit located at MR5[3] to a 1 upon detecting a CRC error, which will subsequently set the CRC error status flag in the MPR error log HIGH (MPR Page1, MPR3[7]). The CRC error status bit (and CRC error status flag) remains set at 1 until the DRAM controller clears the CRC error status bit using an MRS command to set MR5[3] to a 0. The DRAM controller, upon seeing an error as a pulse width, will retry the write transactions. The controller should consider the worst-case delay for ALERT_n (during initialization) and backup the transactions accordingly. The DRAM controller may also be made more intelligent and correlate the write CRC error to a specific rank or a transaction.

FIGURE 137: CRC ERROR REPORTING



Notes:
1. D[71:1] CRC computed by DRAM did not match CRC[7:0] at T5 and started error generating process at T6.
2. CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal LOW to the point where the DRAM driver releases and the controller starts to pull the signal up.

FIGURE 138: CA PARITY FLOW DIAGRAM



Data Bus Inversion

DATA BUS INVERSION (DBI) opportunistically inverts data bits, and in conjunction with the DBI_n I/O, less than half of the DQs will switch LOW for a given DQS strobe edge. The DBI function shares a common pin with the DATA MASK (DM) and TDQS functions. The DBI function applies to either or both READ and WRITE oper-ations: Write DBI cannot be enabled at the same time the DM function is enabled, and DBI is not allowed during MPR READ operation. Valid configurations for TDQS, DM, and DBI functions are shown below.

TABLE 124: DBI VS. DM VS. TDQS FUNCTION MATRIX

Read DBI	Write DBI	Data Mask (DM)	TDQS (x8 only)
Enabled (or Disabled)	Disabled	Disabled	Disabled
Enabled or Disabled	**Enabled**	Disabled	Disabled
Enabled or Disabled	Disabled	**Enabled**	Disabled
Disabled	Disabled	Disabled	**Enabled**

DBI During a WRITE Operation

If DBI_n is sampled LOW on a given byte lane during a WRITE operation, the DRAM inverts write data received on the DQ inputs prior to writing the internal memory array. If DBI_n is sampled HIGH on a given byte lane, the DRAM leaves the data received on the DQ inputs noninverted. The write DQ frame format is shown below for x8 and x16 configurations (the x4 configuration does not support the DBI function).

TABLE 125: DBI WRITE, DQ FRAME FORMAT

	Transfer, Lower (L) and Upper(U)							
Function	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDM_n or LDBI_n	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM_n or UDBI_n	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7

DBI During a READ Operation

If the number of 0 data bits within a given byte lane is greater than four during a READ operation, the DRAM inverts read data on its DQ outputs and drives the DBI_n pin LOW; otherwise, the DRAM does not invert the read data and drives the DBI_n pin HIGH.

TABLE 126: DBI READ, DQ FRAME FORMAT

	Transfer Byte, Lower (L) and Upper(U)							
Function	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDBI_n	LDBI0	LDBI1	LDBI2	LDBI3	LDBI4	LDBI5	LDBI6	LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDBI_n	UDBI0	UDBI1	UDBI2	UDBI3	UDBI4	UDBI5	UDBI6	UDBI7

Data Mask

The DATA MASK (DM) function is also described as PARTIAL WRITE. The DM function shares a common pin with the DBI_n and TDQS functions. The DM function applies only to WRITE operations and cannot be enabled at the same time the WRITE DBI function is enabled. The valid configurations for the TDQS, DM, and DBI functions are shown here.

TABLE 127: DM VS. TDQS VS. DBI FUNCTION MATRIX

Data Mask (DM)	TDQS (x8 only)	Write DBI	Read DBI
Enabled	Disabled	Disabled	Enabled or Disabled
Disabled	**Enabled**	Disabled	Disabled
	Disabled	**Enabled**	Enabled or Disabled
	Disabled	Disabled	**Enabled** (or Disabled)

When enabled, the DM function applies during a WRITE operation. If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs. If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core. The DQ frame format for x8 and x16 configuration is shown below. If both CRC write and DM are enabled (via MRS), the CRC will be checked and valid prior to the DRAM writing data into the DRAM core. If a CRC error occurs while the DM feature is enabled, CRC write persistent mode will be enabled and data will not be written into the DRAM core. In the case of CRC write enabled and DM disabled (via MRS), that is, CRC write nonpersistent mode, data is written to the DRAM core even if a CRC error occurs.

TABLE 128: DATA MASK, DQ FRAME FORMAT

	Transfer, Lower (L) and Upper (U)							
Function	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
LDM_n or LDBI_n	LDM0 or LDBI0	LDM1 or LDBI1	LDM2 or LDBI2	LDM3 or LDBI3	LDM4 or LDBI4	LDM5 or LDBI5	LDM6 or LDBI6	LDM7 or LDBI7
DQ[15:8]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
UDM_n or UDBI_n	UDM0 or UDBI0	UDM1 or UDBI1	UDM2 or UDBI2	UDM3 or UDBI3	UDM4 or UDBI4	UDM5 or UDBI5	UDM6 or UDBI6	UDM7 or UDBI7

Programmable Preamble Modes and DQS Postambles

The device supports programmable WRITE and READ preamble modes, either the normal 1tCK preamble mode or special 2tCK preamble mode. The 2tCK preamble mode places special timing constraints on many operational features as well as being supported for data rates of DDR4-2400 and faster. The WRITE preamble 1tCK or 2tCK mode can be selected independently from READ preamble 1tCK or 2tCK mode.

READ preamble training is also supported; this mode can be used by the DRAM controller to train or "read level" the DQS receivers.

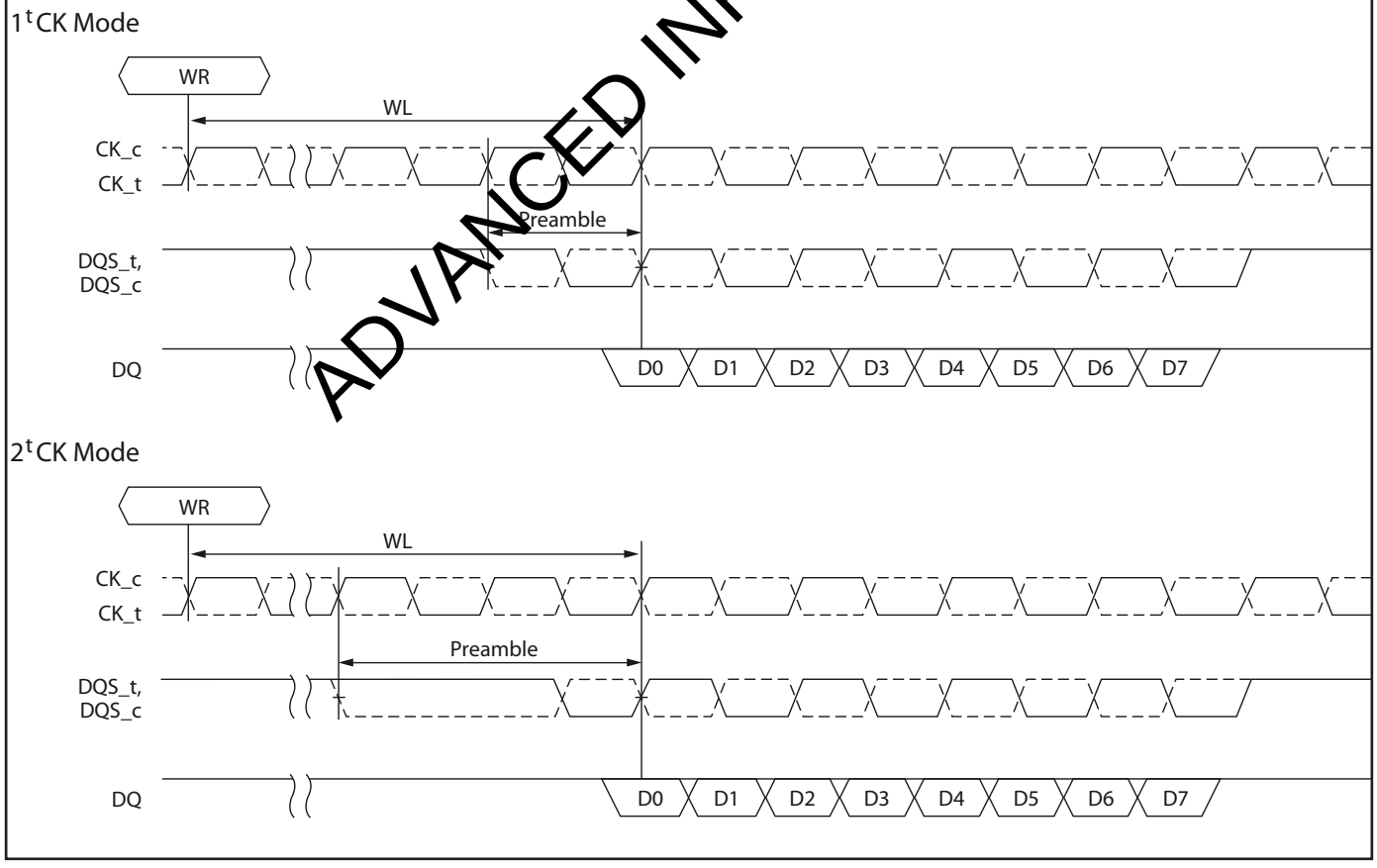
There are tCCD restrictions under some circumstances:

- When 2tCK READ preamble mode is enabled, a tCCD_S or tCCD_L of 5 clocks is not allowed.
- When 2tCK WRITE preamble mode is enabled and write CRC is not enabled, a tCCD_S or tCCD_L of 5 clocks is not allowed.
- When 2tCK WRITE preamble mode is enabled and write CRC is enabled, a tCCD_S or tCCD_L of 6 clocks is not allowed.

WRITE Preamble Mode

MR4[12] = 0 selects 1tCK WRITE preamble mode while MR4[12] = 1 selects 2tCK WRITE preamble mode. Examples are shown in the figures below.

Figure 139: 1TCK vs. 2TCK WRITE Preamble Mode



CWL has special considerations when in the 2tCK WRITE preamble mode. The CWL value selected in MR2[5:3], as seen in table below, requires at least one additional clock when the primary CWL value and 2tCK WRITE preamble mode are used; no additional clocks are required when the alternate CWL value and 2tCK WRITE preamble mode are used.

TABLE 129: CWL SELECTION

	CWL - Primary Choice		CWL - Alternate Choice	
Speed Bin	**1tCK Preamble**	**2tCK Preamble**	**1tCK Preamble**	**2tCK Preamble**
DDR4-1600	9	N/A	11	N/A
DDR4-1866	10	N/A	12	N/A
DDR4-2133	11	N/A	14	N/A
DDR4-2400	12	14	16	16
DDR4-2666	14	16	18	18
DDR4-2933	16	18	20	20
DDR4-3200	16	18	20	20

Note: 1. CWL programmable requirement for MR2[5:3].

When operating in 2tCK WRITE preamble mode, tWTR (command based) and tWR (MR0[11:9]) must be programmed to a value 1 clock greater than the tWTR and tWR setting normally required for the applicable speed bin to be JEDEC compliant; however, STACKED's DDR4 DRAMs do not require these additional tWTR and tWR clocks. The CAS_n-to-CAS_n command delay to either a different bank group (tCCD_S) or the same bank group (tCCD_L) have minimum timing requirements that must be satisfied between WRITE commands and are stated in the Timing Parameters by Speed Bin tables. When operating in 2tCK WRITE preamble mode, tCCD_S and tCCD_L must also be an even number of clocks. As an example, if the minimum timing specification requires only 5tCK, the 5tCK has to be rounded up to 6tCK when operating in 2tCK WRITE preamble mode, while 5tCK would be acceptable if operating in 1tCK WRITE preamble mode.

FIGURE 140: 1TCK VS. 2TCK WRITE PREAMBLE MODE, TCCD = 4

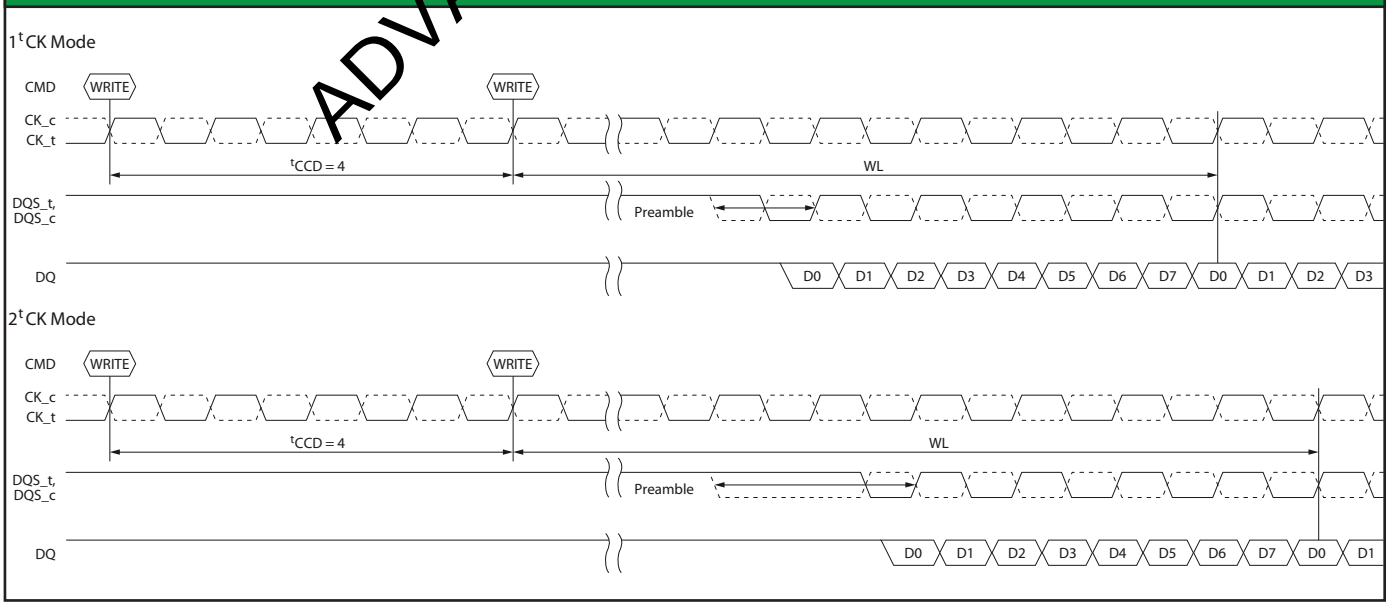
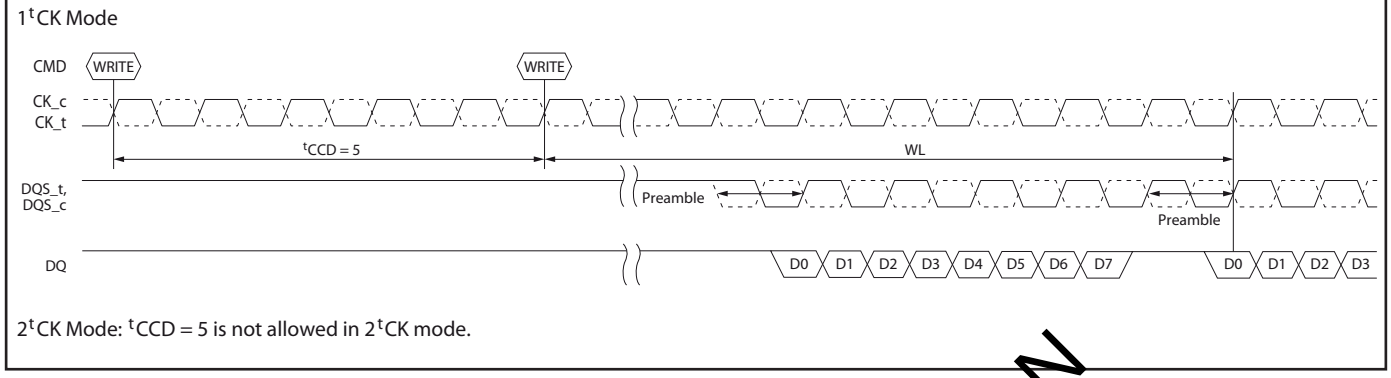
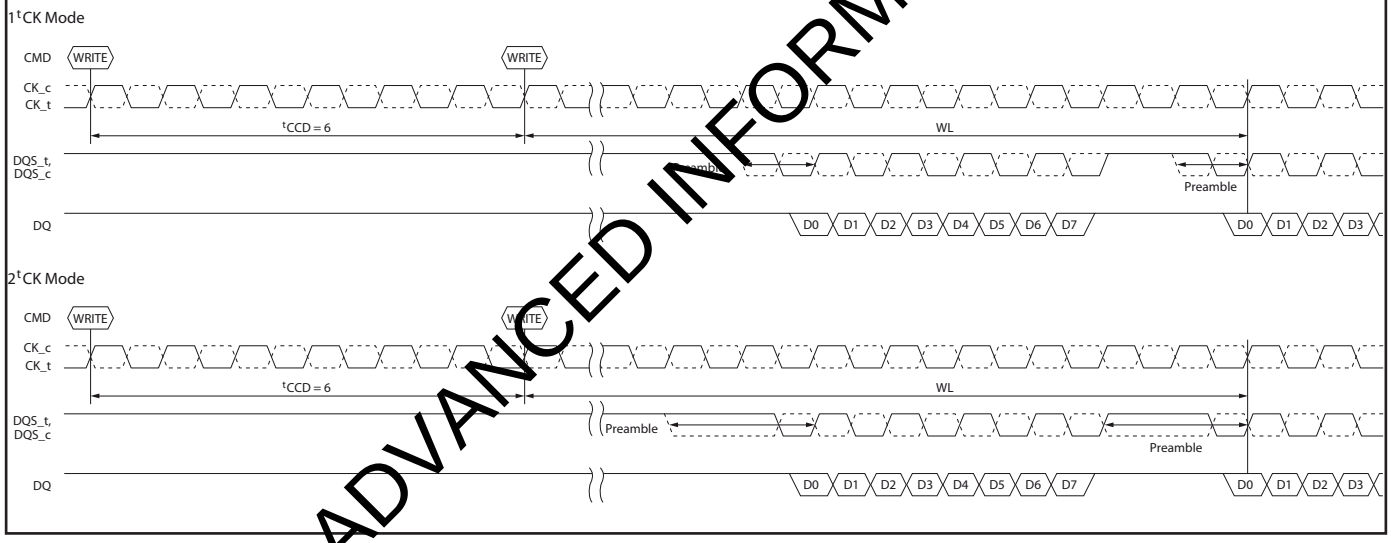


Figure 141: 1TCK vs. 2TCK WRITE Preamble Mode, TCCD = 5



Note: 1. tCCD_S and tCCD_L = 5 tCKs is not allowed when in 2tCK WRITE preamble mode.

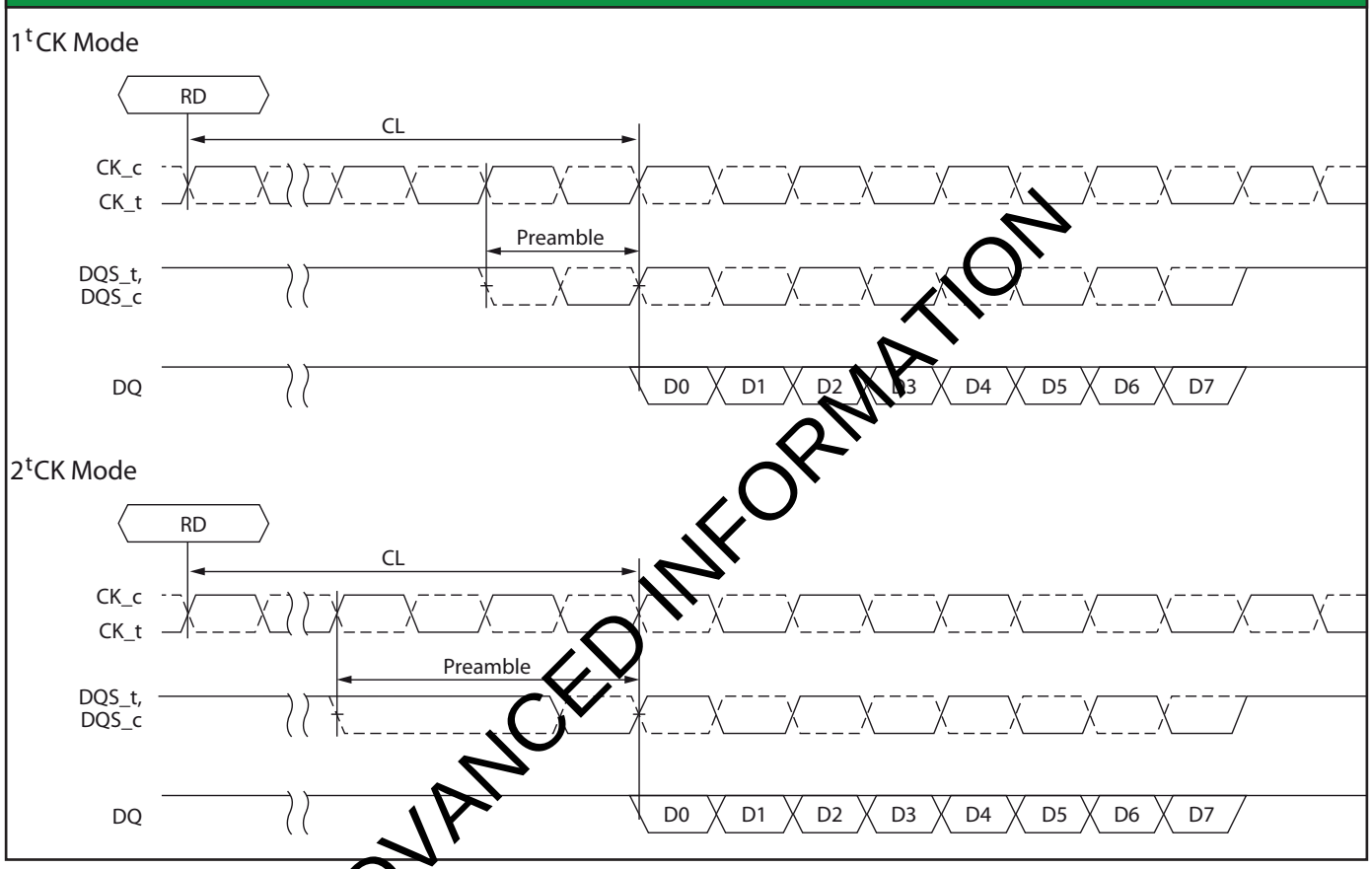
Figure 142: 1TCK vs. 2TCK WRITE Preamble Mode, TCCD = 6



READ Preamble Mode

MR4[11] = 0 selects 1tCK READ preamble mode and MR4[12] = 1 selects 2tCK READ preamble mode. Examples are shown in the following figure.

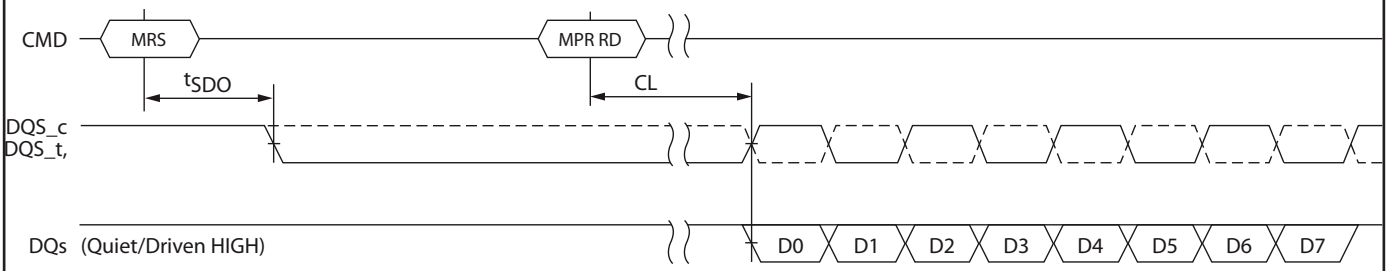
Figure 143: 1TCK vs. 2TCK READ Preamble Mode



READ Preamble Training

DDR4 supports READ preamble training via MPR reads; that is, READ preamble training is allowed only when the DRAM is in the MPR access mode. The READ preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers. READ preamble training is entered via an MRS command (MR4[10] = 1 is enabled and MR4[10] = 0 is disabled). After the MRS command is issued to enable READ preamble training, the DRAM DQS signals are driven to a valid level by the time tSDO is satisfied. During this time, the data bus DQ signals are held quiet, that is, driven HIGH. The DQS_t signal remains driven LOW and the DQS_c signal remains driven HIGH until an MPR Page0 READ command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit READ preamble training mode, an MRS command must be issued, MR4[10] = 0.

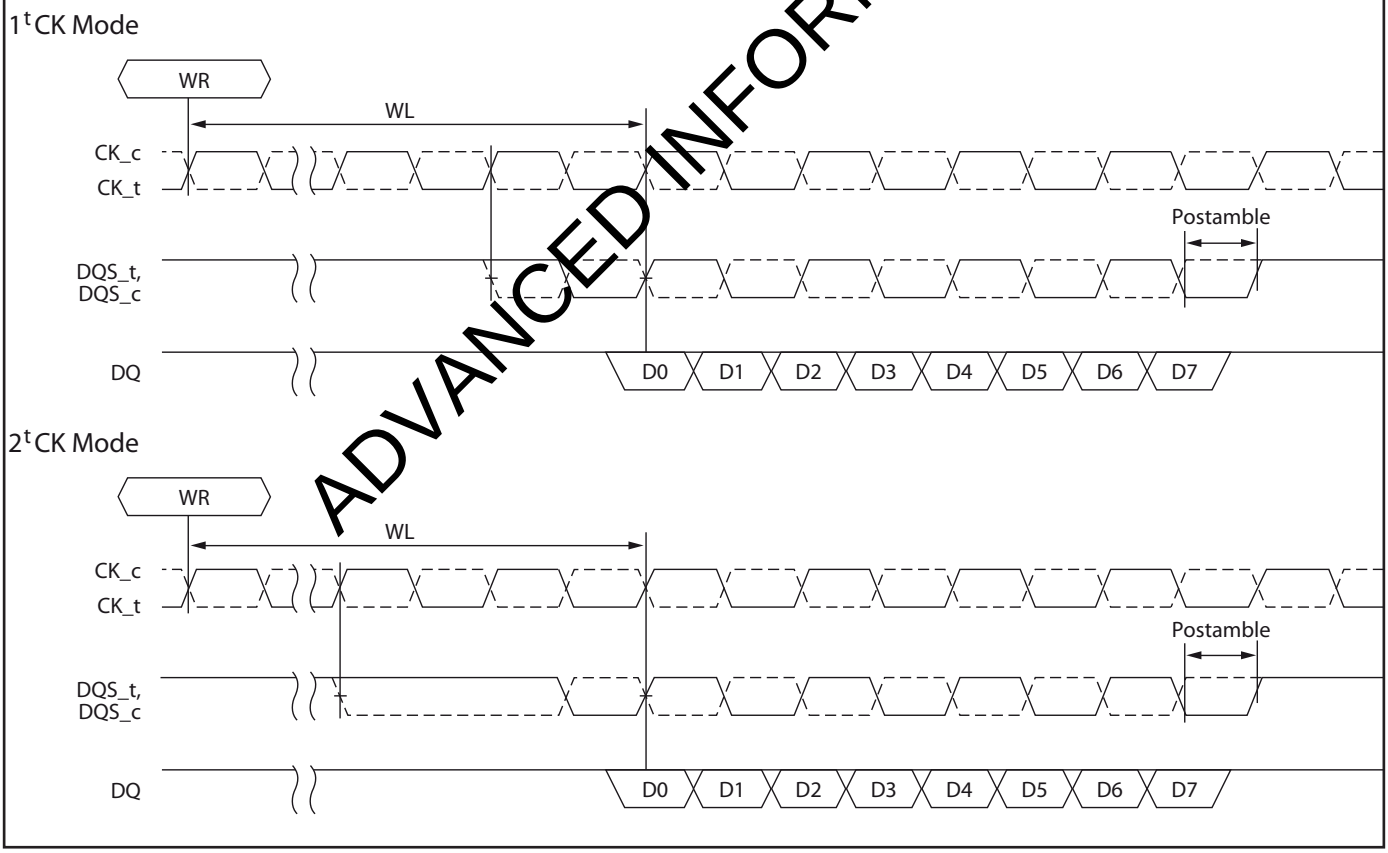
Figure 144: READ Preamble Training



WRITE Postamble

Whether the 1tCK or 2tCK WRITE preamble mode is selected, the WRITE postamble remains the same at ½tCK.

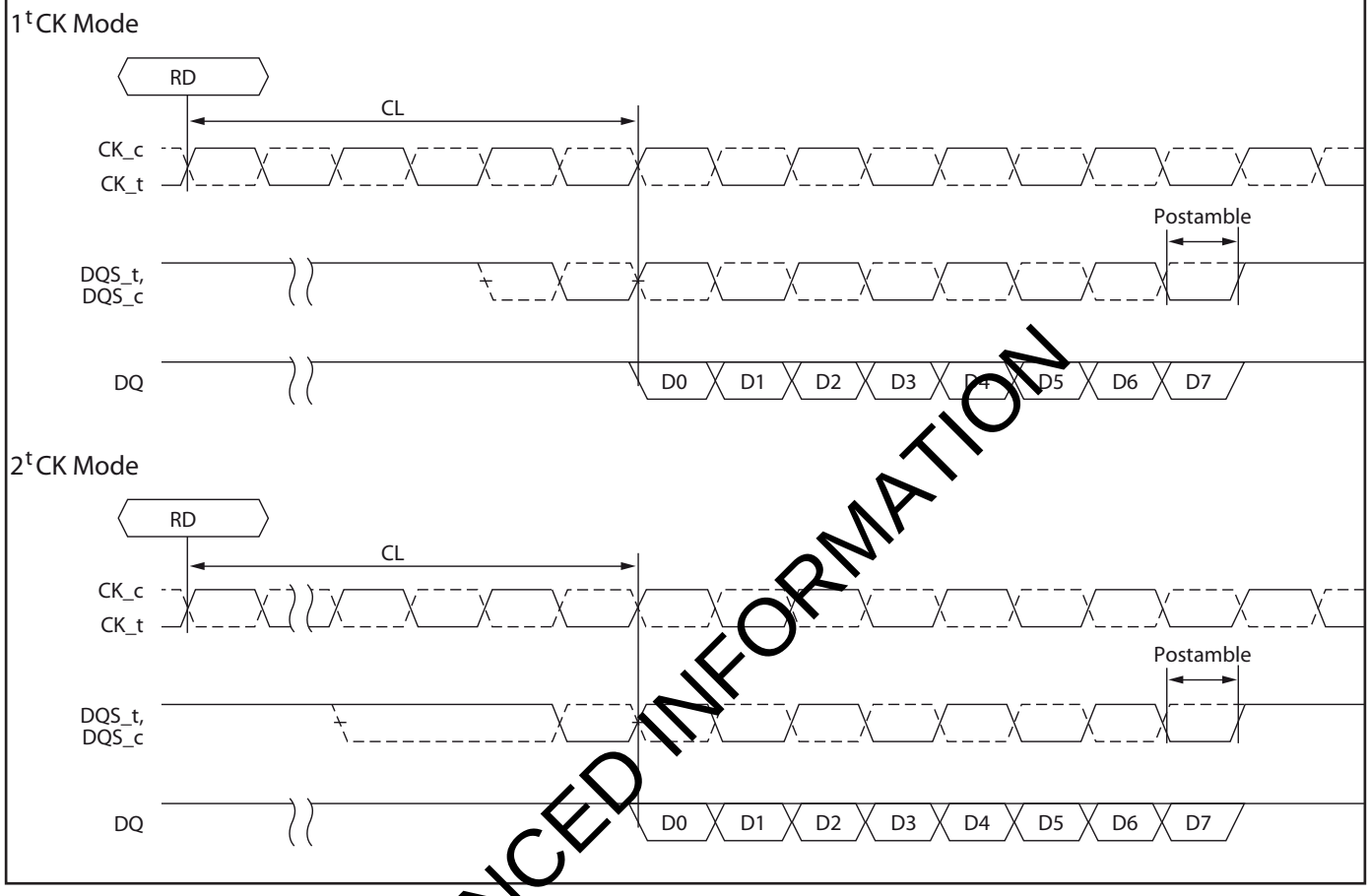
Figure 145: WRITE Postamble



READ Postamble

Whether the 1tCK or 2tCK READ preamble mode is selected, the READ postamble remains the same at ½tCK.

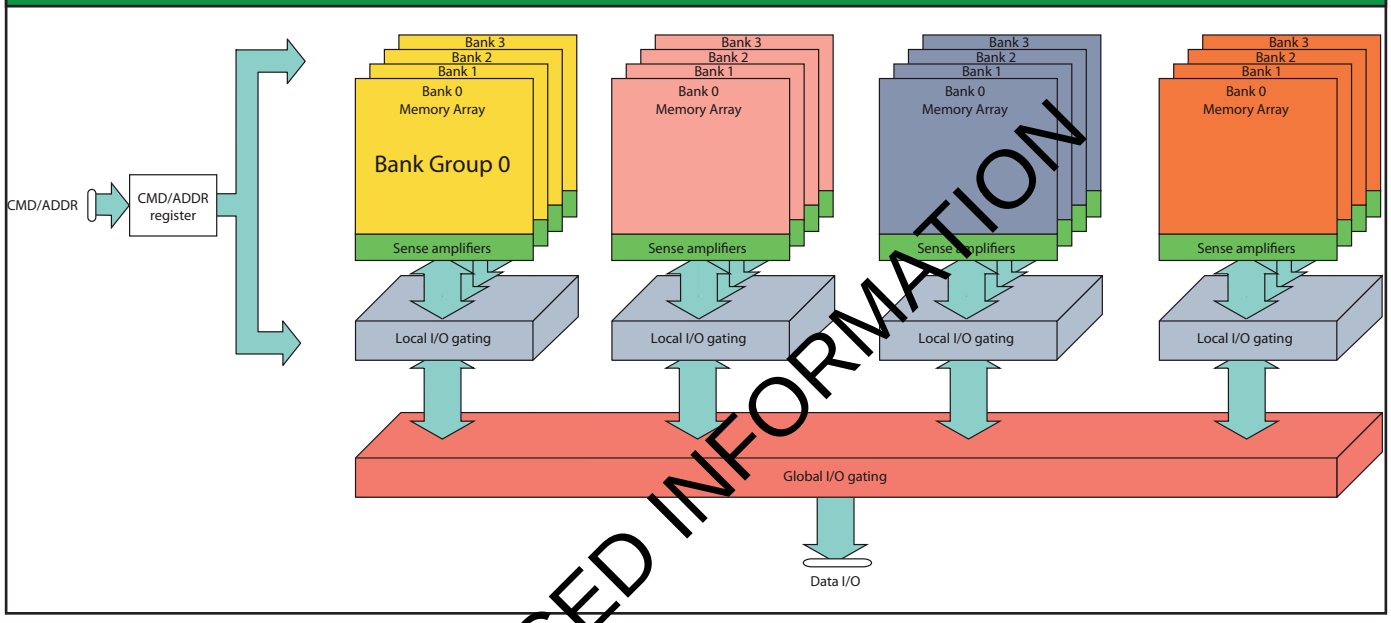
Figure 146: READ Postamble



Bank Access Operation

DDR4 supports bank grouping four subbanks (BA[1:0]); x16 DRAMs have two bank groups (BG[0]), and each bank group is comprised of four subbanks. Bank accesses to different banks' groups require less time delay between accesses than bank accesses to within the same bank's group. Bank accesses to different bank groups require ^{t}CCD_S (or short) delay between commands while bank accesses within the same bank group require ^{t}CCD_L (or long) delay between commands.

FIGURE 147: BANK GROUP X4/X8 BLOCK DIAGRAM



Notes: 1. Bank accesses to different bank groups require ^{t}CCD_S.
2. Bank accesses within the same bank group require ^{t}CCD_L.

TABLE 130: DDR4 BANK GROUP TIMING EXAMPLES

Parameter	DDR4-1600	DDR4-2133	DDR4-2400
^{t}CCD_S	4*n*CK	4*n*CK	4*n*CK
^{t}CCD_L	4*n*CK or 6.25ns	4*n*CK or 5.355ns	4*n*CK or 5ns
^{t}RRD_S (½K)	4*n*CK or 5ns	4*n*CK or 3.7ns	4*n*CK or 3.3ns
^{t}RRD_L (½K)	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 4.9ns
^{t}RRD_S (1K)	4*n*CK or 5ns	4*n*CK or 3.7ns	4*n*CK or 3.3ns
^{t}RRD_L (1K)	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 4.9ns
^{t}RRD_S (2K)	4*n*CK or 6ns	4*n*CK or 5.3ns	4*n*CK or 5.3ns
^{t}RRD_L (2K)	4*n*CK or 7.5ns	4*n*CK or 6.4ns	4*n*CK or 6.4ns

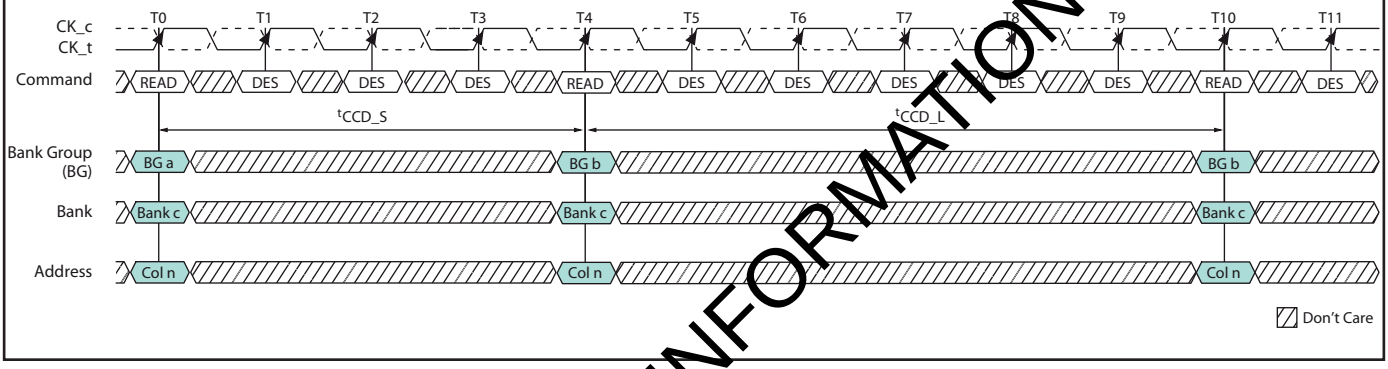
Bank Access Operation

TABLE 130: DDR4 BANK GROUP TIMING EXAMPLES (CONTINUED)

Parameter	DDR4-1600	DDR4-2133	DDR4-2400
^{t}WTR_S	2*n*CK or 2.5ns	2*n*CK or 2.5ns	2*n*CK or 2.5ns
^{t}WTR_L	4*n*CK or 7.5ns	4*n*CK or 7.5ns	4*n*CK or 7.5ns

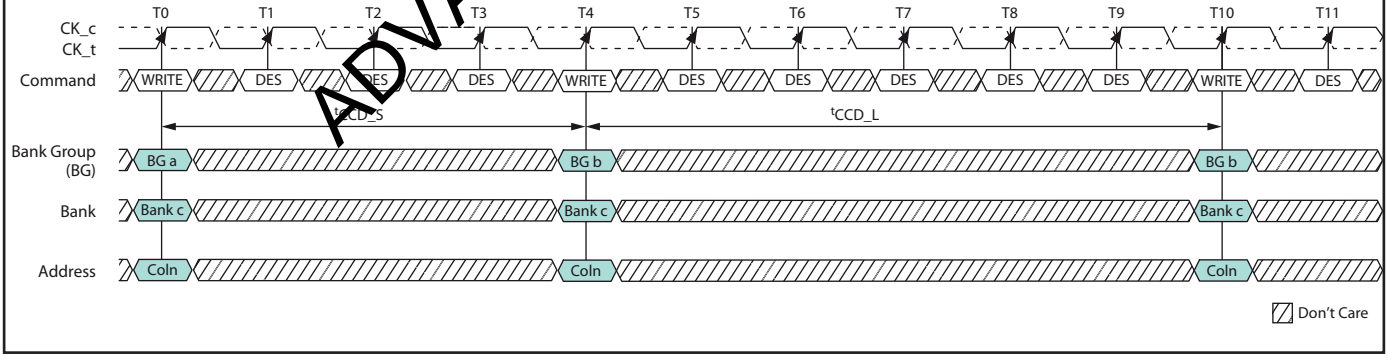
Notes:
1. Refer to Timing Tables for actual specification values, these values are shown for reference only and are not verified for accuracy.
2. Timings with both nCK and ns require both to be satisfied; that is, the larger time of the two cases must be satisfied.

FIGURE 148: READ BURST ^{t}CCD_S AND ^{t}CCD_L EXAMPLES



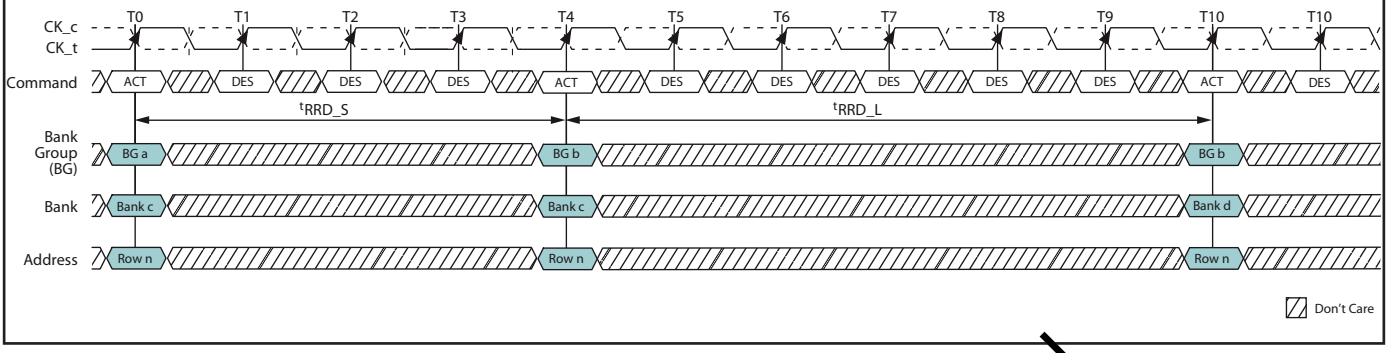
Notes:
1. ^{t}CCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).
2. ^{t}CCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10).

FIGURE 149: WRITE BURST ^{t}CCD_S AND ^{t}CCD_L EXAMPLES



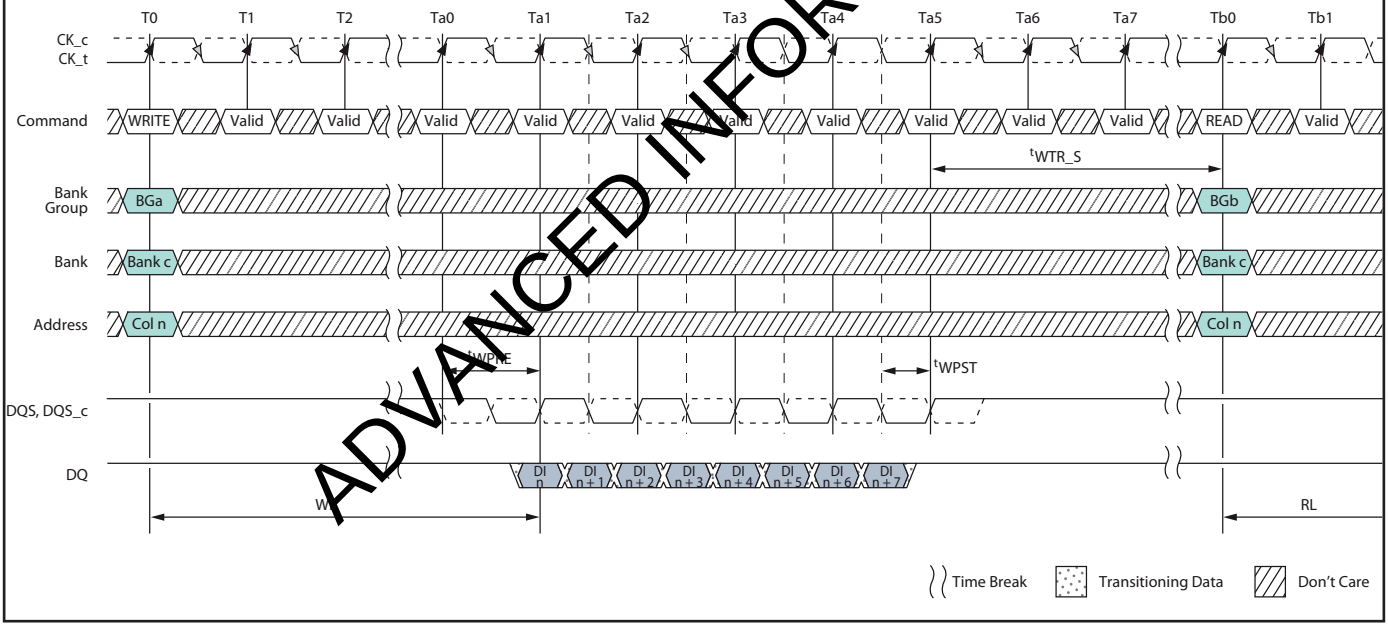
Notes:
1. ^{t}CCD_S; CAS_n-to-CAS_n delay (short). Applies to consecutive CAS_n to different bank groups (T0 to T4).
2. ^{t}CCD_L; CAS_n-to-CAS_n delay (long). Applies to consecutive CAS_n to the same bank group (T4 to T10).

FIGURE 150: TRRD TIMING



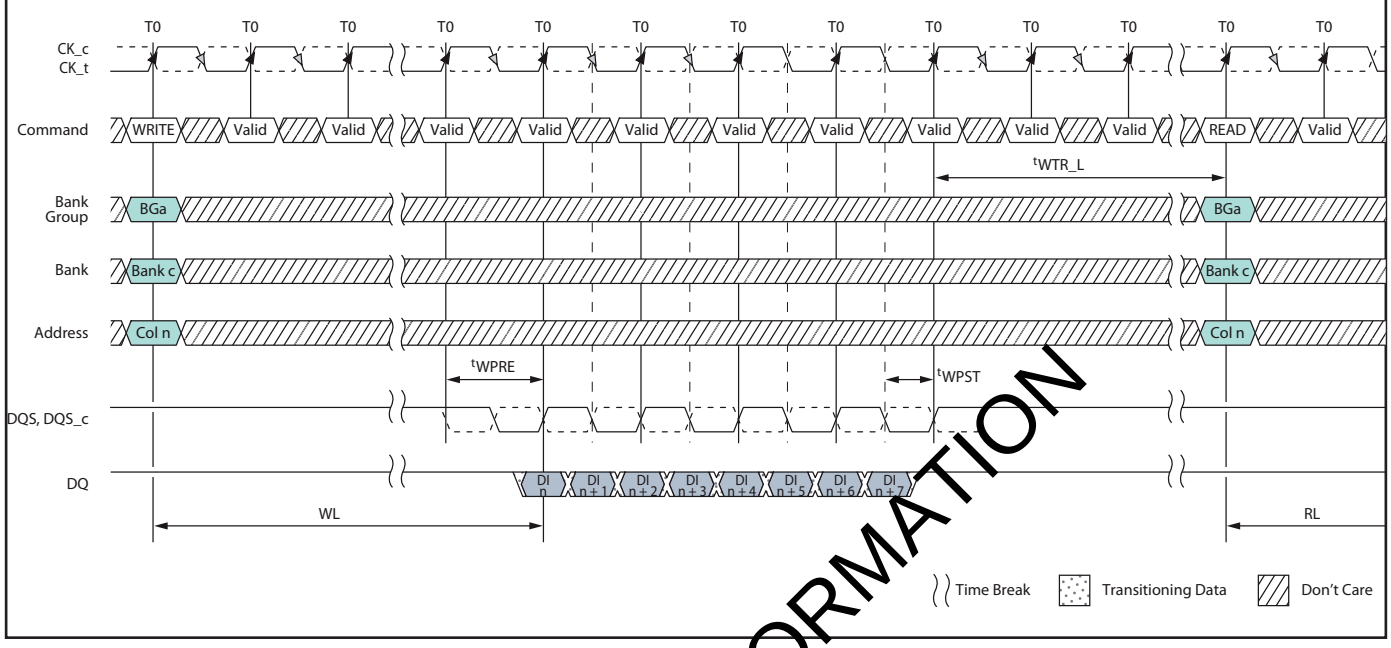
Notes:
1. tRRD_S; ACTIVATE-to-ACTIVATE command period (short), applies to consecutive ACTIVATE commands to different bank groups (T0 and T4).
2. tRRD_L; ACTIVATE-to-ACTIVATE command period (long), applies to consecutive ACTIVATE commands to the different banks in the same bank group (T4 and T10).

FIGURE 151: TWTR_S TIMING (WRITE-TO-READ, DIFFERENT BANK GROUP, CRC AND DM DISABLED)



Note:
1. tWTR_S: delay from start of internal write transaction to internal READ command to a different bank group.

Figure 152: tWTR_L Timing (WRITE-to-READ, Same Bank Group, CRC and DM Disabled)



Note: 1. tWTR_L: delay from start of internal write transaction to internal READ command to the same bank group.

READ Operation

Read Timing Definitions

The read timings shown below are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Note: ^{t}DQSQ = both rising/falling edges of DQS; no ^{t}AC defined.

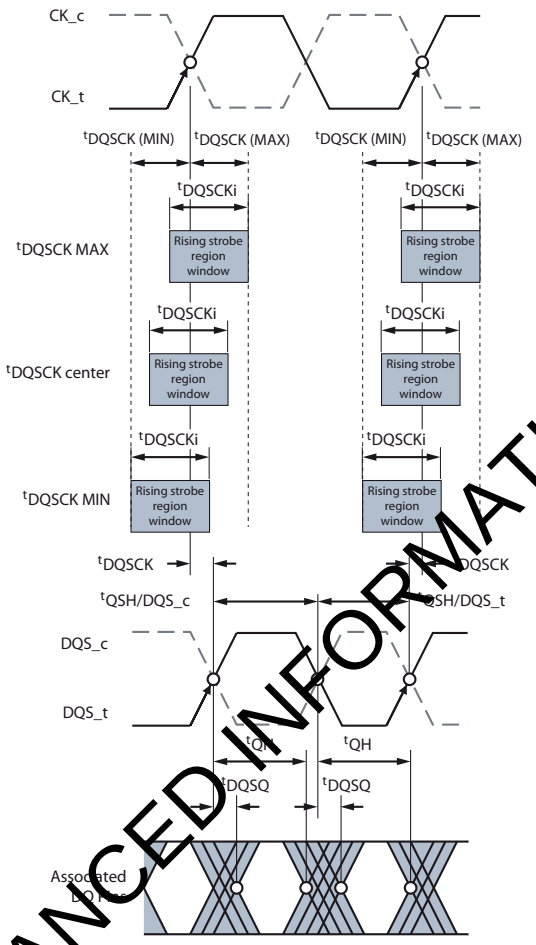
Rising data strobe edge parameters:

- ^{t}DQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSCK is the actual position of a rising strobe edge relative to CK.
- ^{t}QSH describes the DQS differential output HIGH time.
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- ^{t}QSL describes the DQS differential output LOW time.
- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Figure 153: Read Timing Definition



Read Timing - Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship shown below is applicable in normal operation mode, that is, when the DLL is enabled and locked.

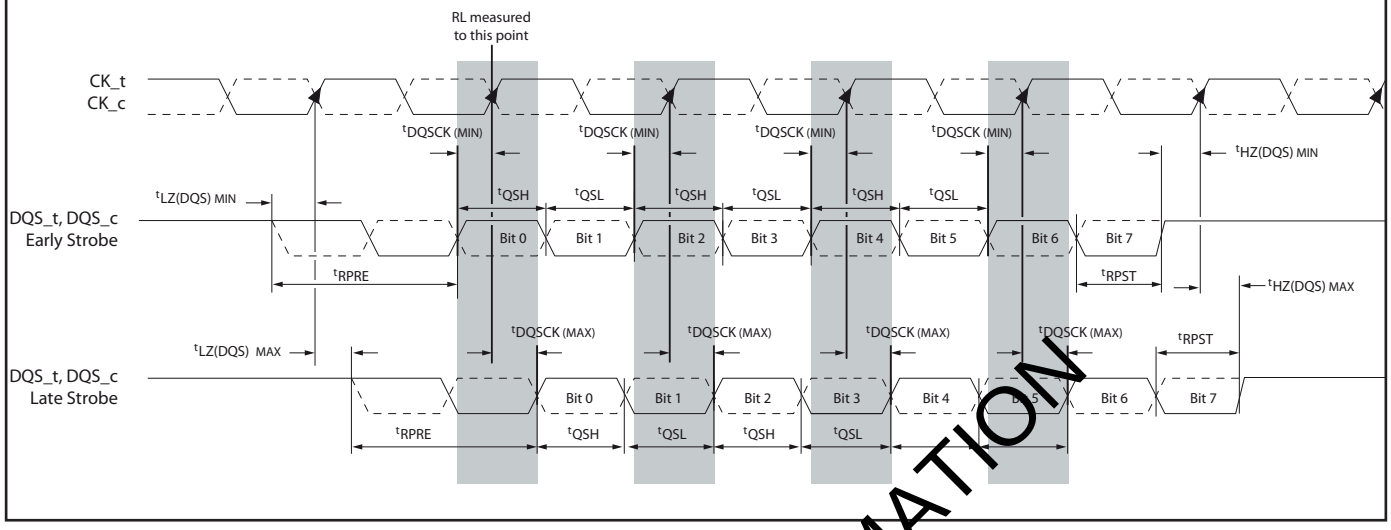
Rising data strobe edge parameters:

- ^{t}DQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSCK is the actual position of a rising strobe edge relative to CK.
- ^{t}QSH describes the data strobe high pulse width.
- ^{t}HZ(DQS) DQS strobe going to high, nondrive level (shown in the postamble section of the figure below).

Falling data strobe edge parameters:

- ^{t}QSL describes the data strobe low pulse width.
- ^{t}LZ(DQS) DQS strobe going to low, initial drive level (shown in the preamble section of the figure below).

Figure 154: Clock-to-Data Strobe Relationship



Notes:

1. Within a burst, the rising strobe edge will vary within ^{t}DQSCKj while at the same voltage and temperature. However, when the device, voltage, and temperature variations are incorporated, the rising strobe edge variance window can shift between ^{t}DQSCK (MIN) and ^{t}DQSCK (MAX).

   A timing of this window's right edge (latest) from rising CK_t, CK_c is limited by a device's actual ^{t}DQSCK (MAX). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by ^{t}DQSCK (MIN).
2. Notwithstanding Note 1, a rising strobe edge with ^{t}DQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with ^{t}DQSCK (MIN) at T(n + 1) because other timing relationships (^{t}QSH, ^{t}QSL) exist: if ^{t}DQSCK(n + 1) < 0: ^{t}DQSCK(n) < 1.0 ^{t}CK - (^{t}QSH (MIN) + ^{t}QSL (MIN)) - | ^{t}DQSCK(n + 1) |.
3. The DQS_t, DQS_c differential output HIGH time is defined by ^{t}QSH, and the DQS_t, DQS_c differential output LOW time is defined by tQSL.
4. ^{t}LZ(DQS) MIN and ^{t}HZ(DQS) MIN are not tied to ^{t}DQSCK (MIN) (early strobe case), and ^{t}LZ(DQS) MAX and ^{t}HZ(DQS) MAX are not tied to ^{t}DQSCK (MAX) (late strobe case).
5. The minimum pulse width of READ preamble is defined by ^{t}RPRE (MIN).
6. The maximum READ postamble is bound by ^{t}DQSCK (MIN) plus ^{t}QSH (MIN) on the left side and ^{t}HZDSQ (MAX) on the right side.
7. The minimum pulse width of READ postamble is defined by tRPST (MIN).
8. The maximum READ preamble is bound by ^{t}LZDQS (MIN) on the left side and ^{t}DQSCK (MAX) on the right side.

Read Timing - Data Strobe-to-Data Relationship

The data strobe-to-data relationship is shown below and is applied when the DLL is enabled and locked.

Note: tDQSQ: both rising/falling edges of DQS; no tAC defined.

Rising data strobe edge parameters:

- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

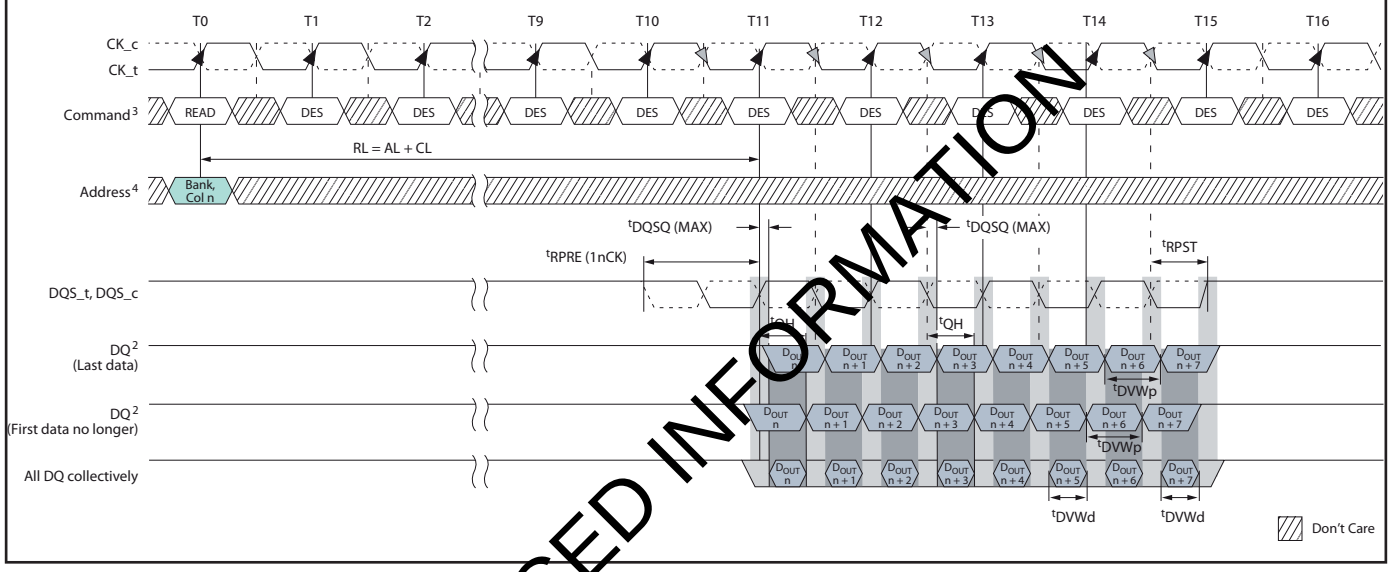
Falling data strobe edge parameters:

- ^{t}DQSQ describes the latest valid transition of the associated DQ pins.
- ^{t}QH describes the earliest invalid transition of the associated DQ pins.

Data valid window parameters:

- ^{t}DVWd is the Data Valid Window per device per UI and is derived from [tQH - tDQSQ] of each UI on a given DRAM
- ^{t}DVWp is the Data Valid Window per pin per UI and is derived [tQH - tDQSQ] of each UI on a pin of a given DRAM

Figure 155: Data Strobe-to-Data Relationship

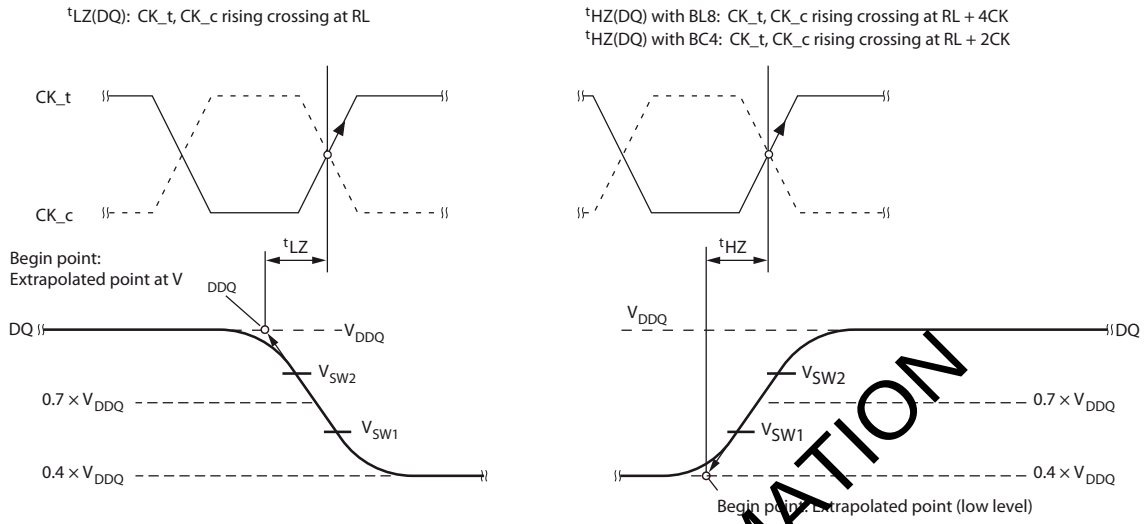


Notes:
1. BL = 8, RL = 11 (AL = 0, CL = 1) , Premable = 1^{t}CK.
2. DOUTn = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.
5. Output timings are referenced to VDDQ, and DLL on for locking.
6. ^{t}DQSQ defines the skew between DQS to data and does not define DQS to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) Calculations

^{t}HZ and ^{t}LZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving ^{t}HZ(DQS) and ^{t}HZ(DQ), or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ). The figure below shows a method to calculate the point when the device is no longer driving ^{t}HZ(DQS) and tHZ(DQ), or begins driving ^{t}LZ(DQS) and ^{t}LZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. ^{t}LZ(DQS), ^{t}LZ(DQ), ^{t}HZ(DQS), and ^{t}HZ(DQ) are defined as singled-ended parameters.

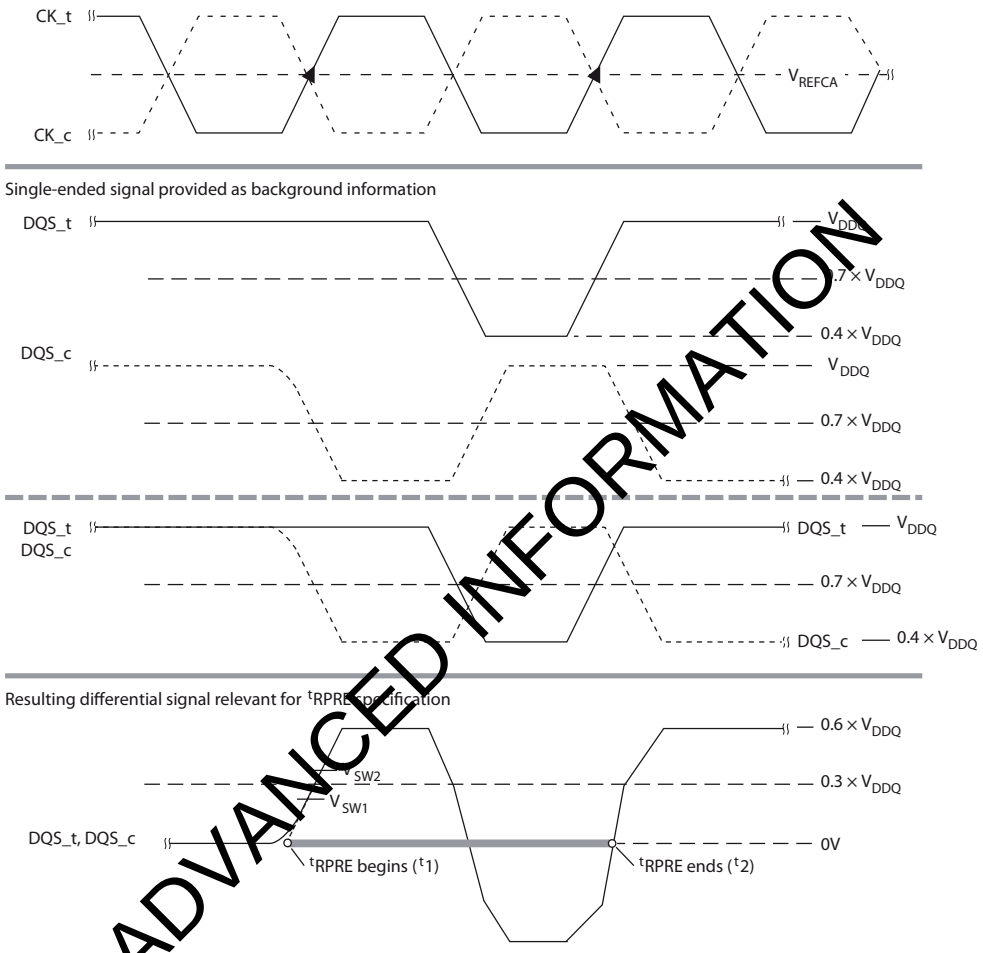
FIGURE 156: TLZ AND THZ METHOD FOR CALCULATING TRANSITIONS AND ENDPOINTS



Notes:
1. $V_{sw1} = (0.70 - 0.04) \times V_{DDQ}$ for both tLZ and tHZ.
2. $V_{sw2} = (0.70 + 0.04) \times V_{DDQ}$ for both tLZ and tHZ.
3. Extrapolated point (low level) = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$
   Driver impedance = RZQ/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

tRPRE Calculation

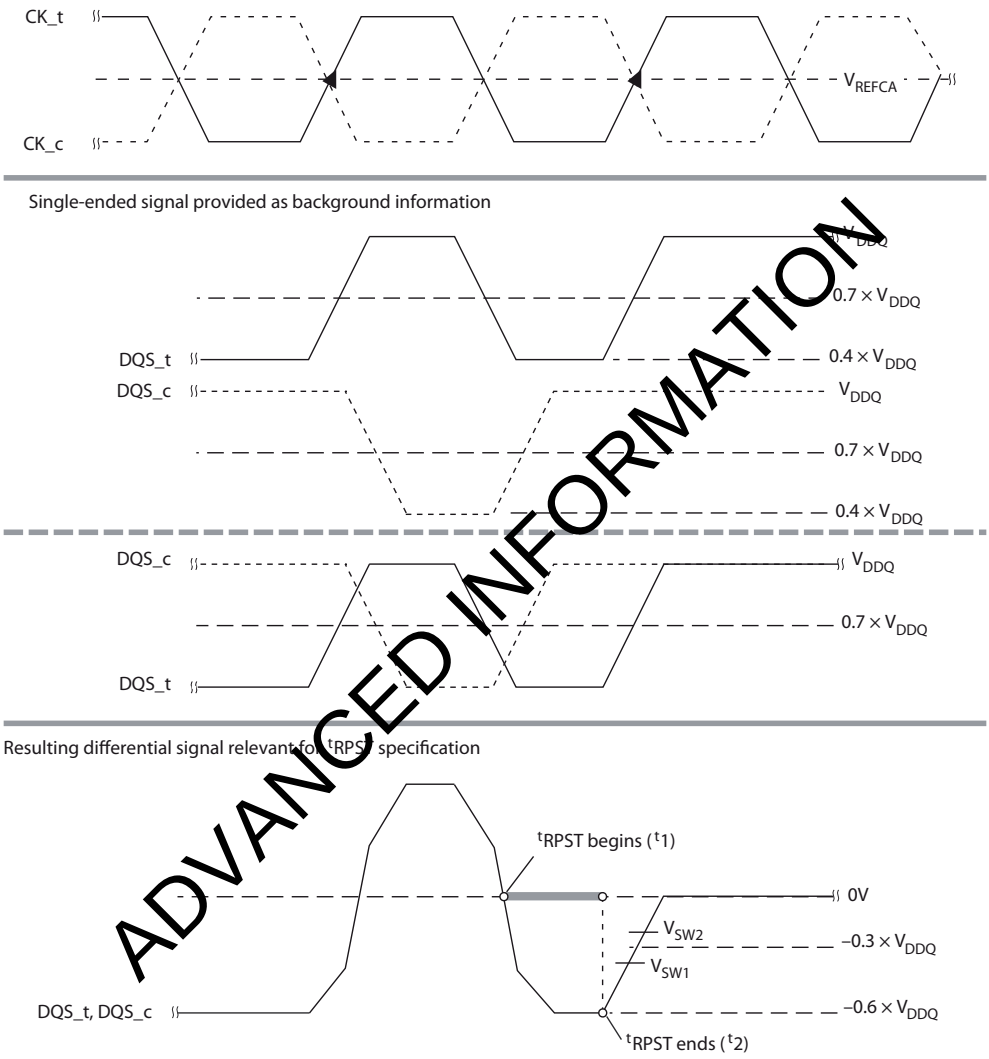
Figure 157: tRPRE Method for Calculating Transitions and Endpoints



Notes:
1. V_{sw1} = (0.3 - 0.04) × VDDQ.
2. V_{sw2} = (0.30 + 0.04) × VDDQ.
3. DQS_t and DQS_c low level = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$
   Driver impedance = RZQ/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

tRPST Calculation

Figure 158: tRPST Method for Calculating Transitions and Endpoints



Notes:
1. $V_{sw1} = (-0.3 - 0.04) \times V_{DDQ}$.
2. 2. $V_{sw2} = (-0.30 + 0.04) \times V_{DDQ}$.
3. 3. DQS_t and DQS_c low level = $V_{DDQ}/(50 + 34) \times 34 = 0.4 \times V_{DDQ}$
   Driver impedance = RZQ/7 = 34Ω
   V_{TT} test load = 50Ω to V_{DDQ}.

READ Burst Operation

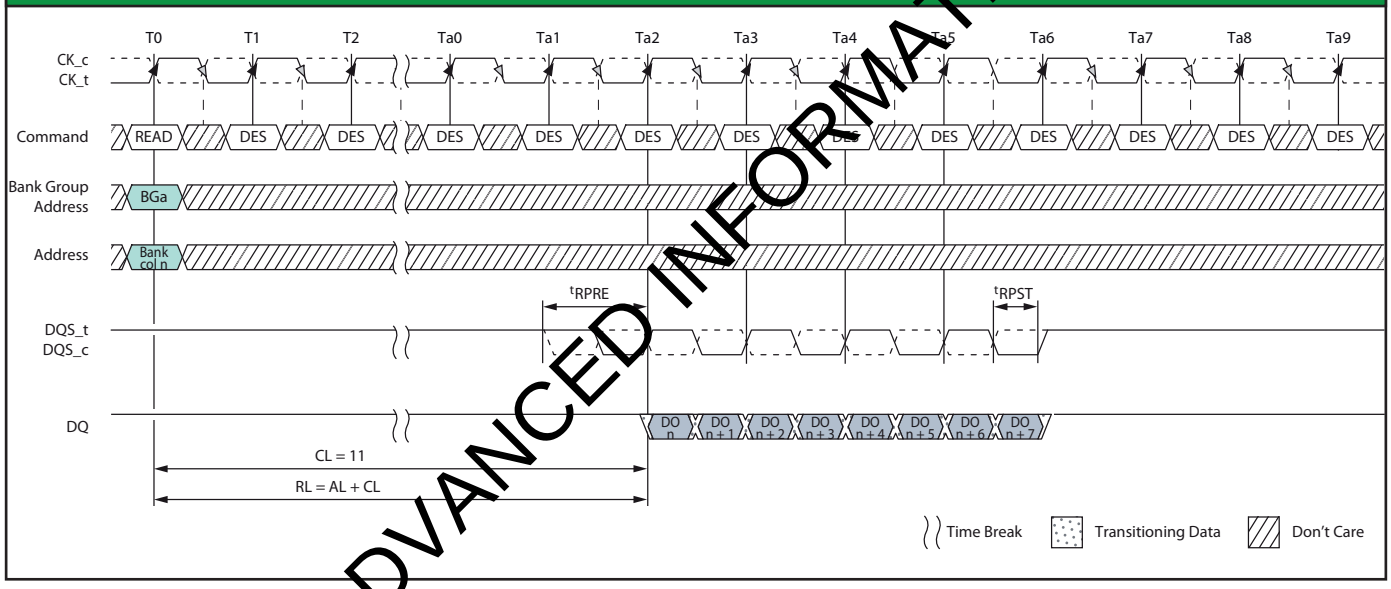
DDR4 READ commands support bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

READ commands can issue precharge automatically with a READ with auto precharge command (RDA), and is enabled by A10 HIGH:

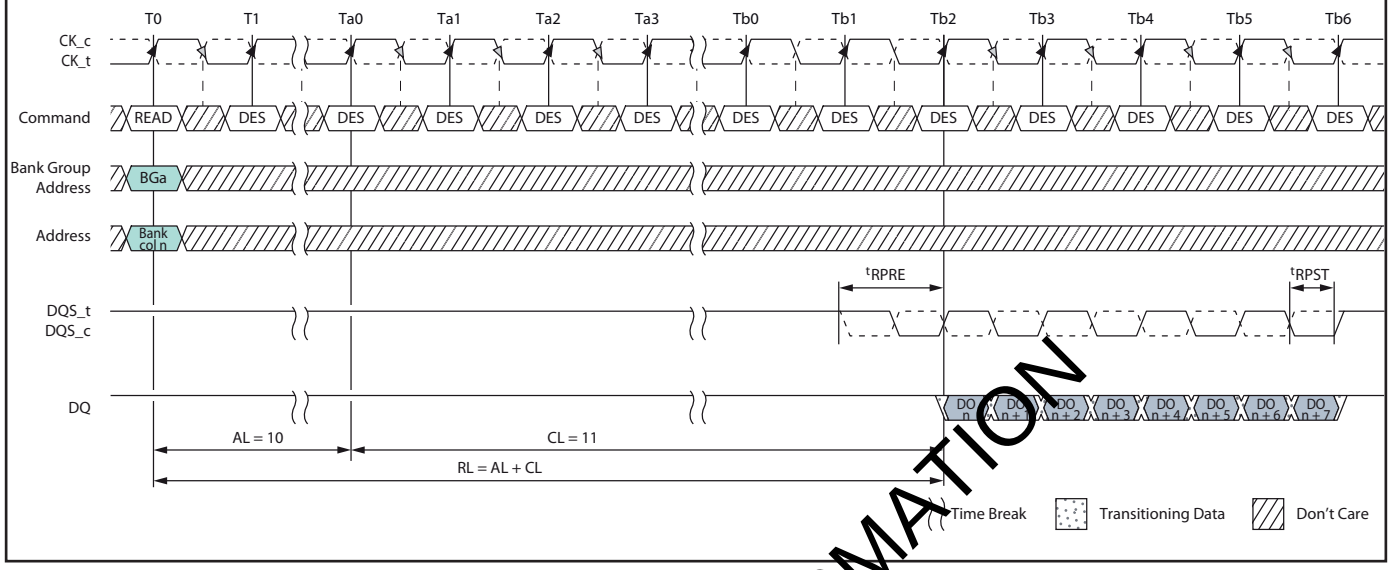
- READ command with A10 = 0 (RD) performs standard read, bank remains active after READ burst.
- READ command with A10 = 1 (RDA) performs read with auto precharge, bank goes in to precharge after READ burst.

FIGURE 159: READ BURST OPERATION, RL = 11 (AL = 0, CL = 11, BL8)



Notes:
1. BL8, RL = 0, AL = 0, CL = 11, Preamble = 1tCK.
2. DO n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

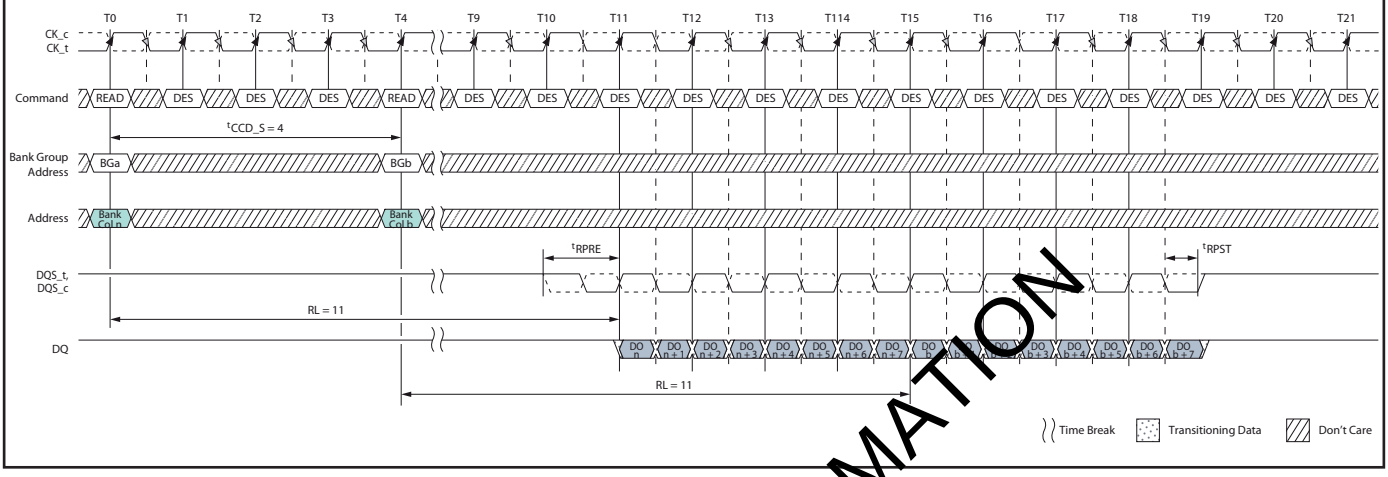
FIGURE 160: READ BURST OPERATION, RL = 21 (AL = 10, CL = 11, BL8)



Notes:
1. BL8, RL = 21, AL = (CL - 1), CL = 11, Preamble = 1tCK.
2. DO n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

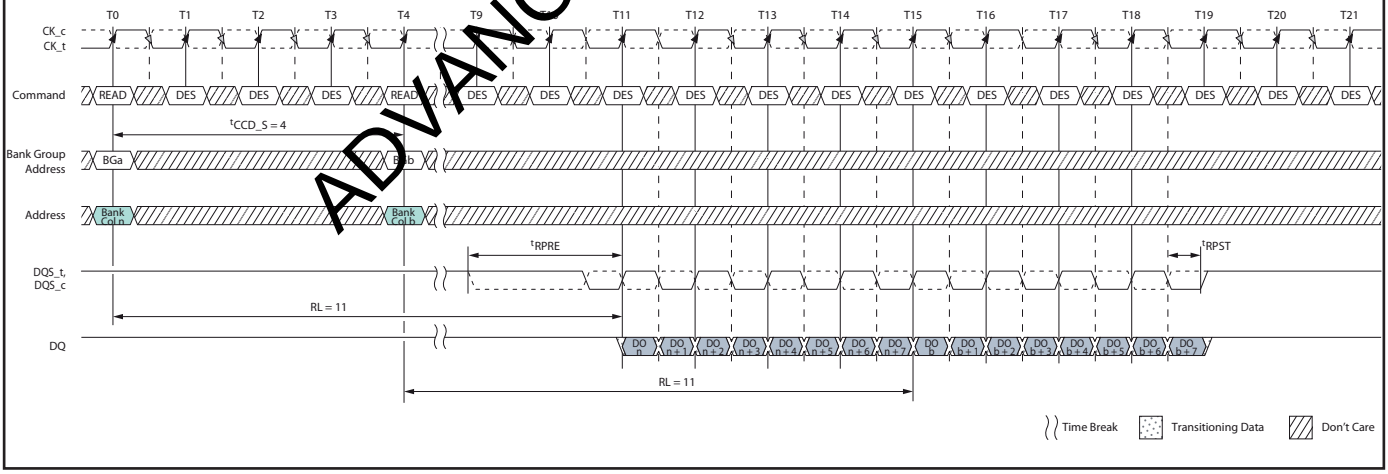
READ Operation Followed by Another READ Operation

Figure 161: Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



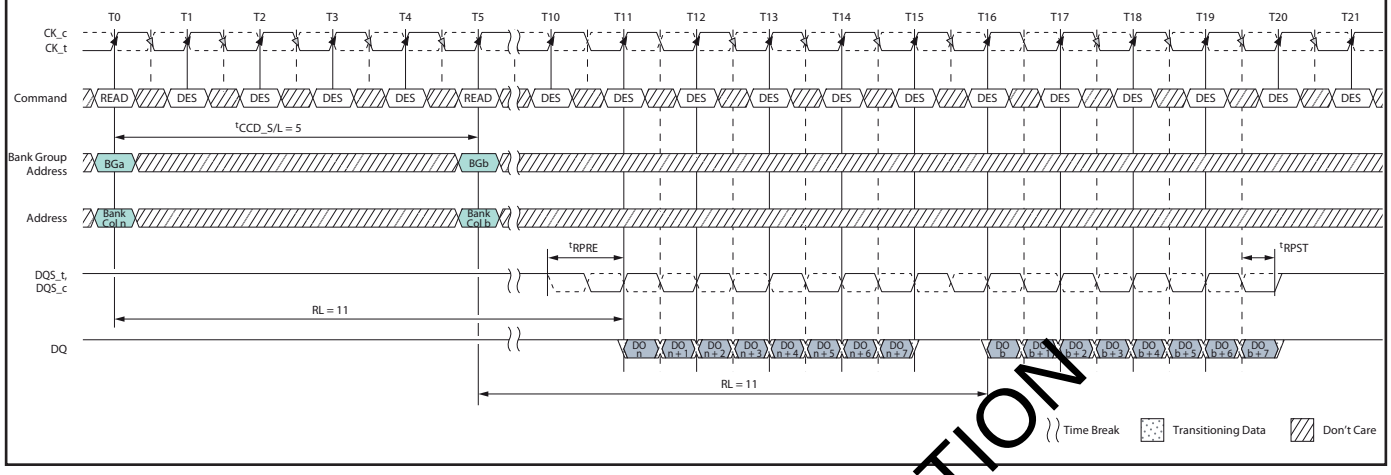
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 162: Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



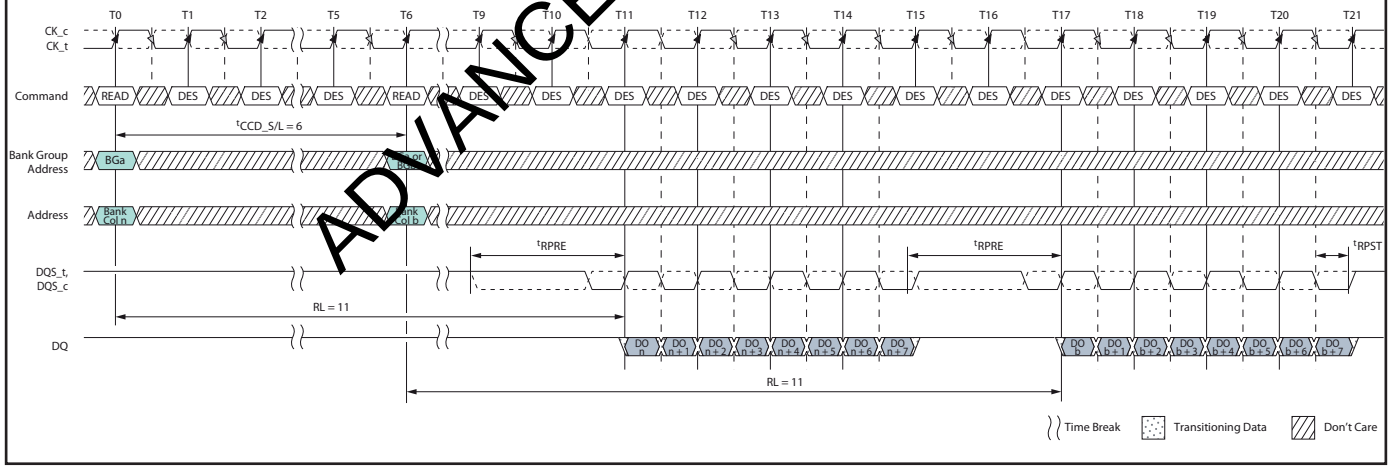
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 163: Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank



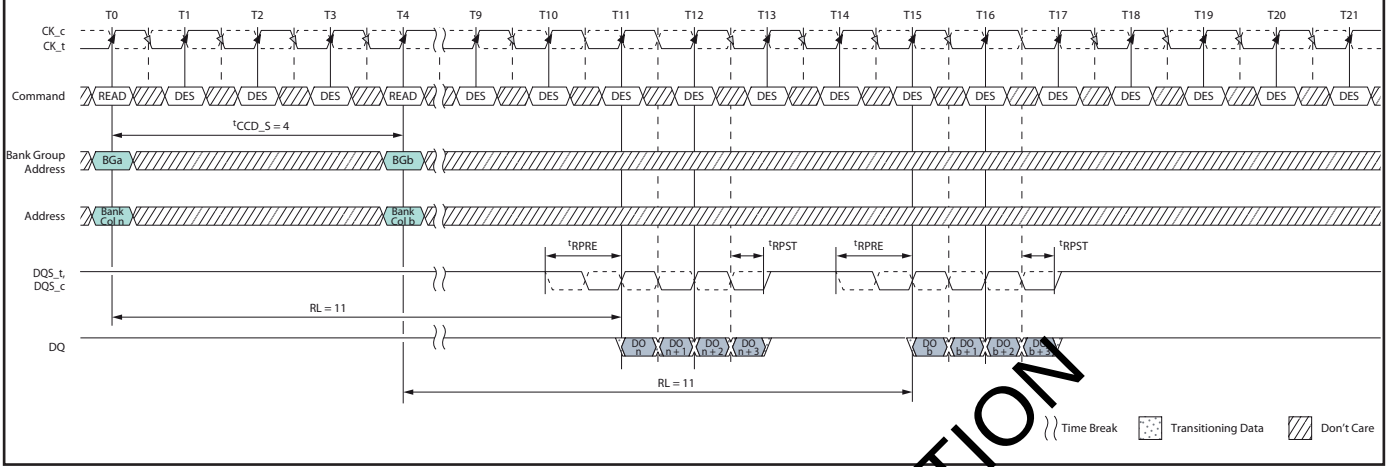
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

Figure 164: Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



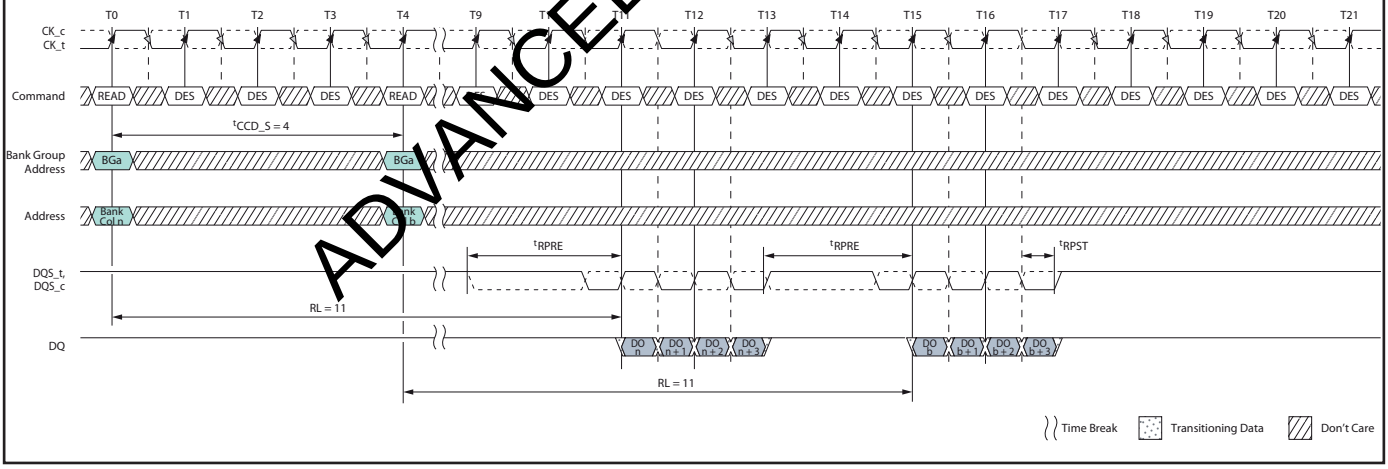
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.
6. 6 tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

FIGURE 165: READ (BC4) TO READ (BC4) WITH 1TCK PREAMBLE IN DIFFERENT BANK GROUP



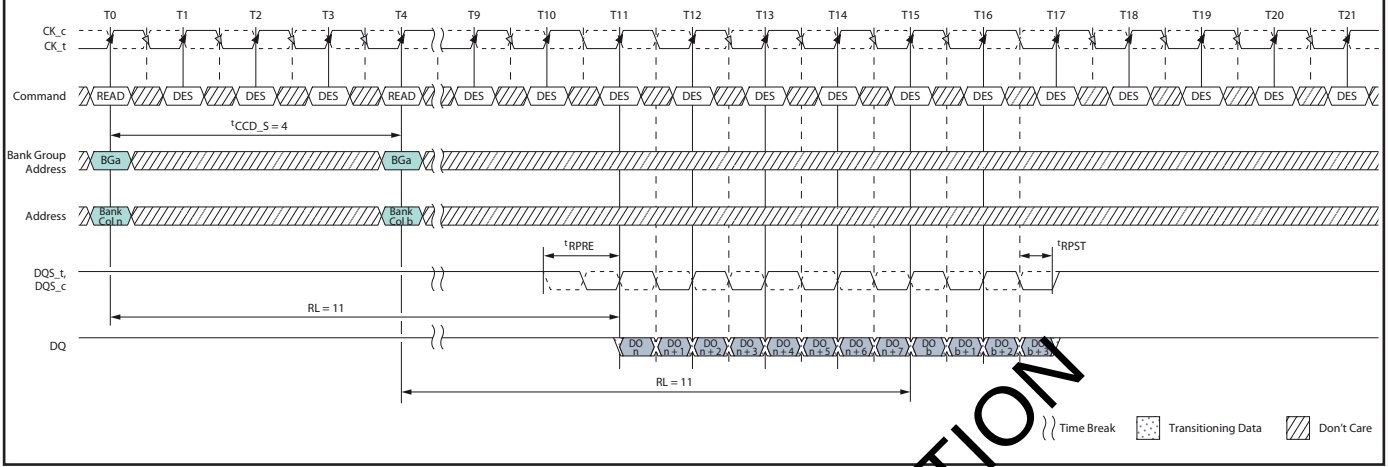
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 166: READ (BC4) TO READ (BC4) WITH 2TCK PREAMBLE IN DIFFERENT BANK GROUP



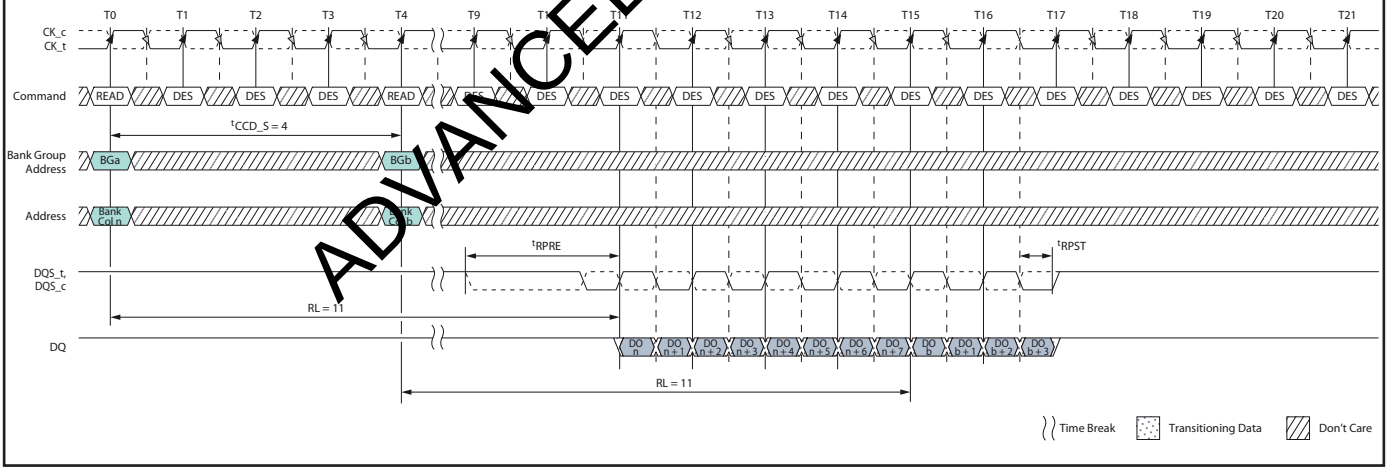
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 167: READ (BL8) TO READ (BC4) OTF WITH 1TCK PREAMBLE IN DIFFERENT BANK GROUP



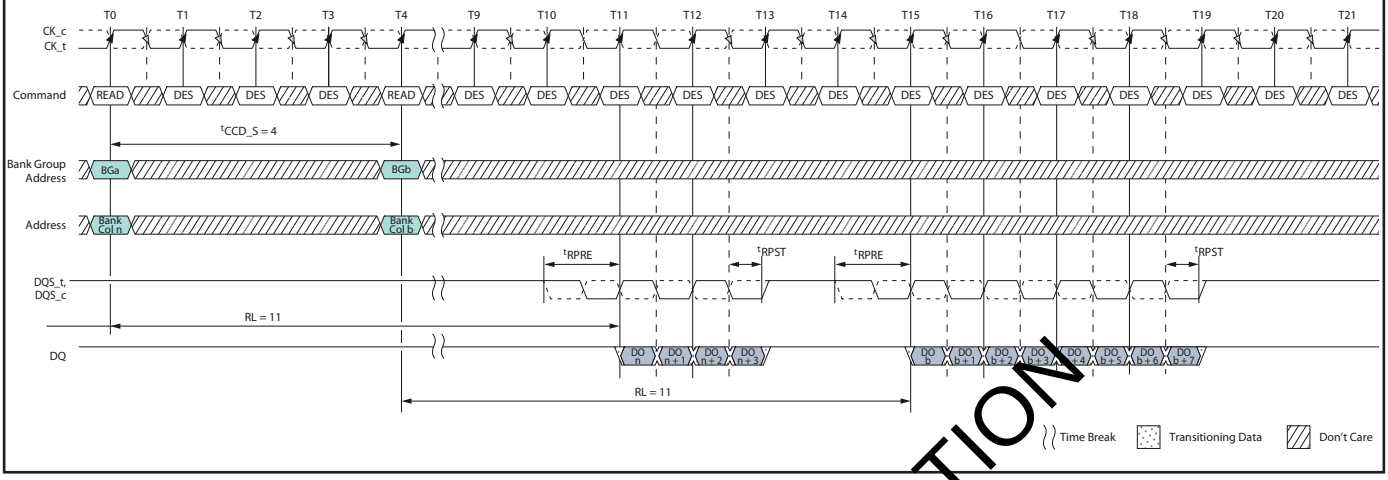
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 168: READ (BL8) TO READ (BC4) OTF WITH 2TCK PREAMBLE IN DIFFERENT BANK GROUP



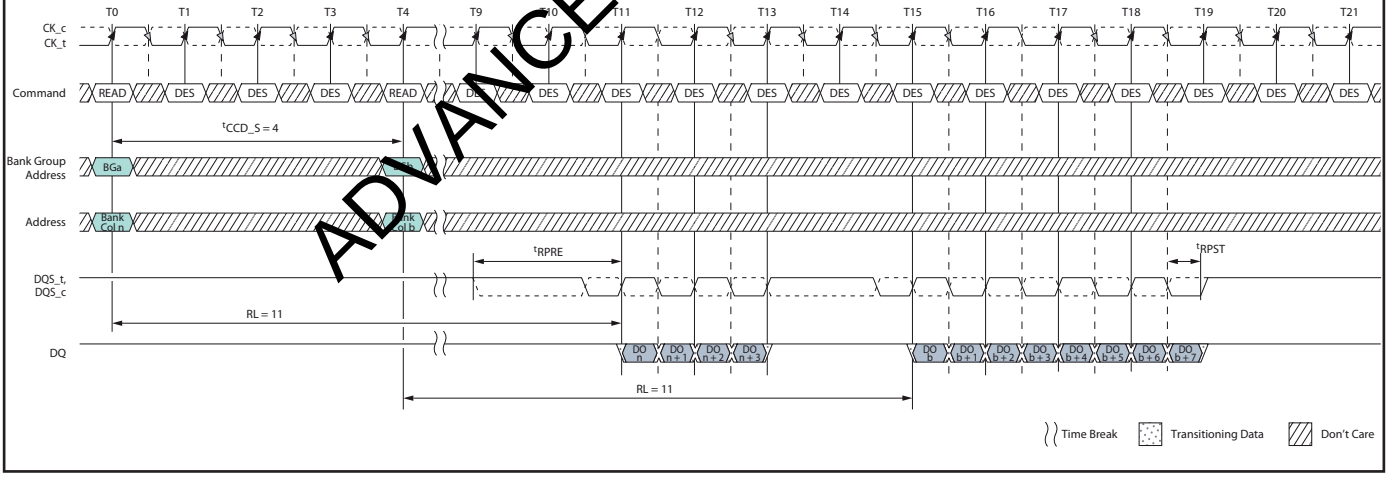
Notes:
1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 169: READ (BC4) TO READ (BL8) OTF WITH 1TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BL = 8, AL =0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

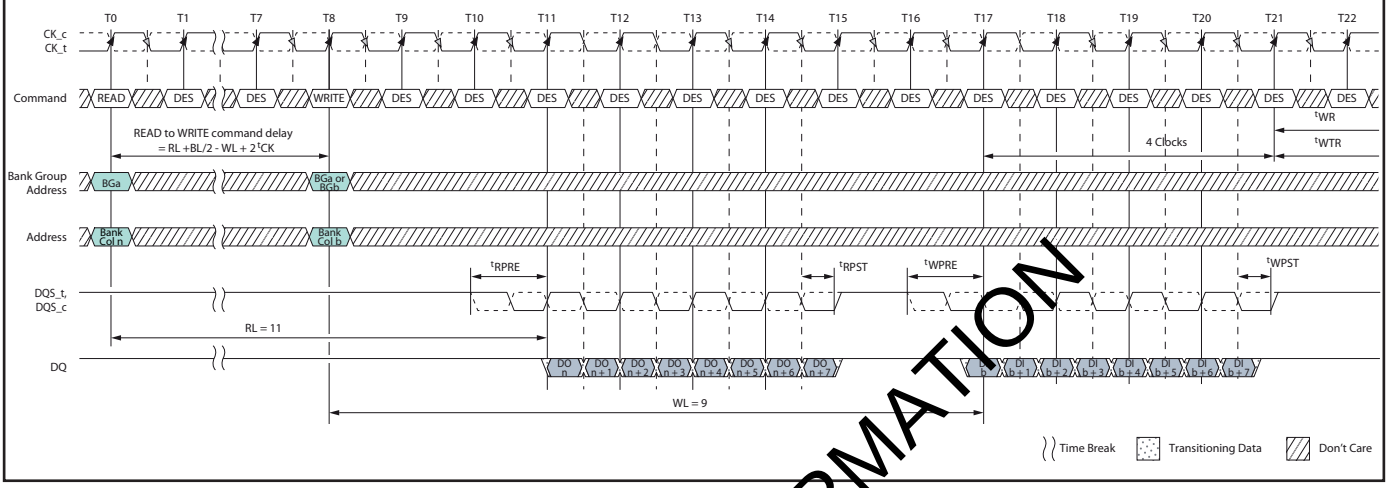
FIGURE 170: READ (BC4) TO READ (BL8) OTF WITH 2TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

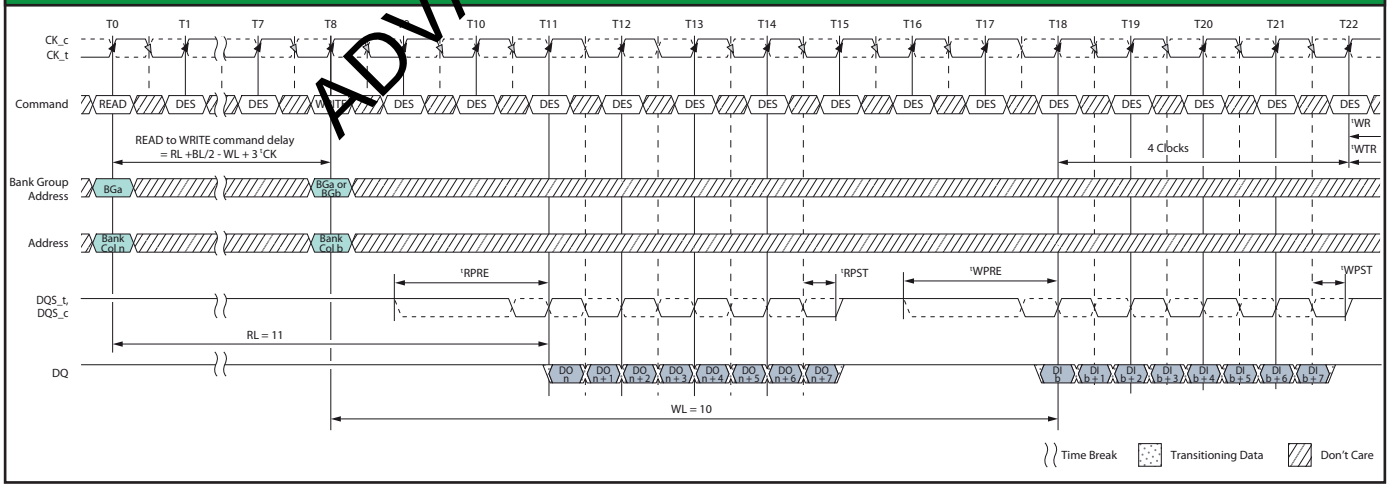
READ Operation Followed by WRITE Operation

FIGURE 171: READ (BL8) TO WRITE (BL8) WITH 1^TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1^tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1^tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

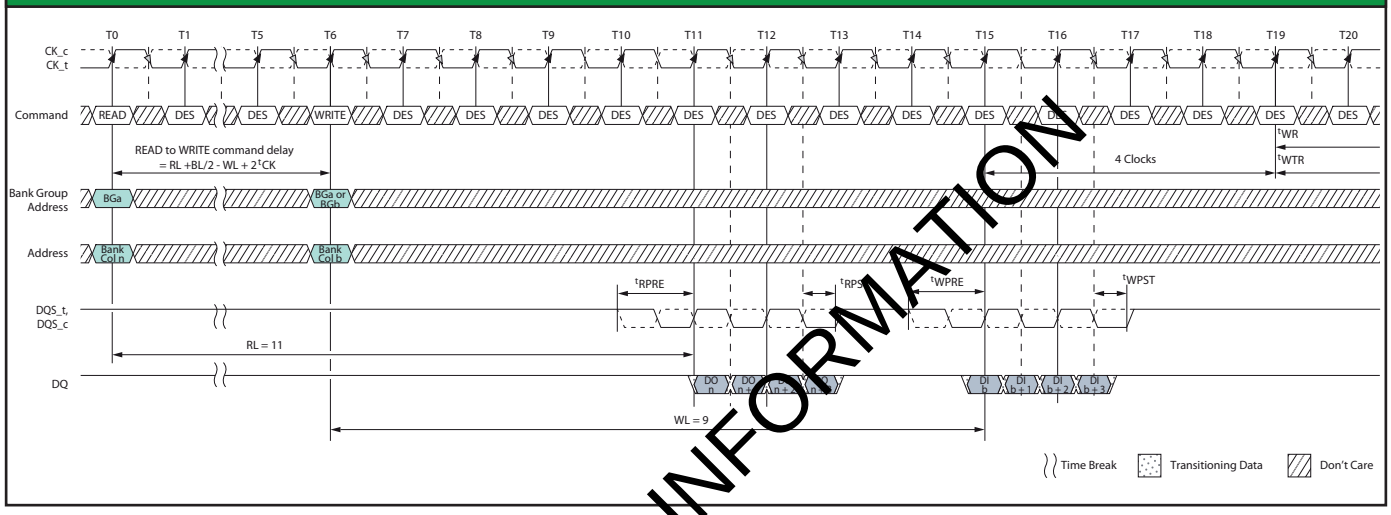
FIGURE 172: READ (BL8) TO WRITE (BL8) WITH 2^TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2^tCK, WL = 10 (CWL = 9+1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

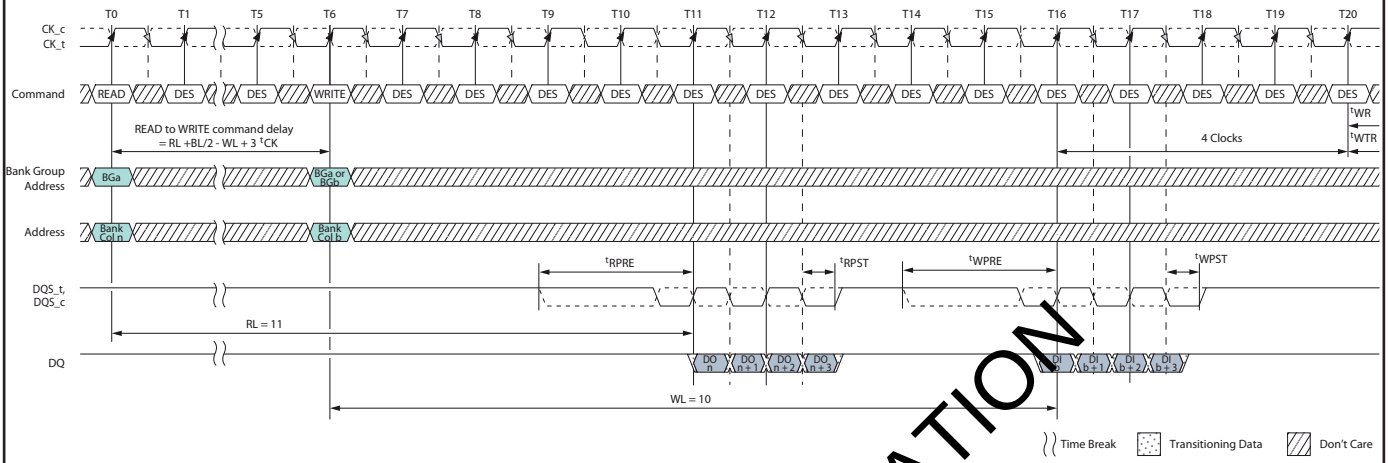
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 173: READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



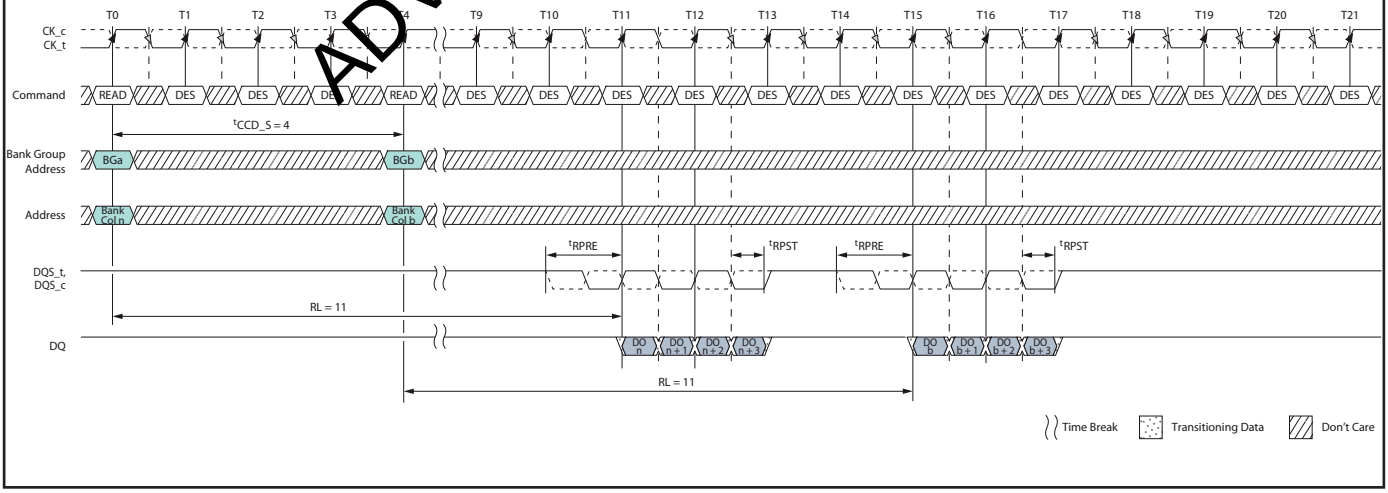
Notes:
1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

FIGURE 174: READ (BC4) OTF TO WRITE (BC4) OTF WITH 2TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (OTF) setting activated by MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and WRITE commands at T6.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

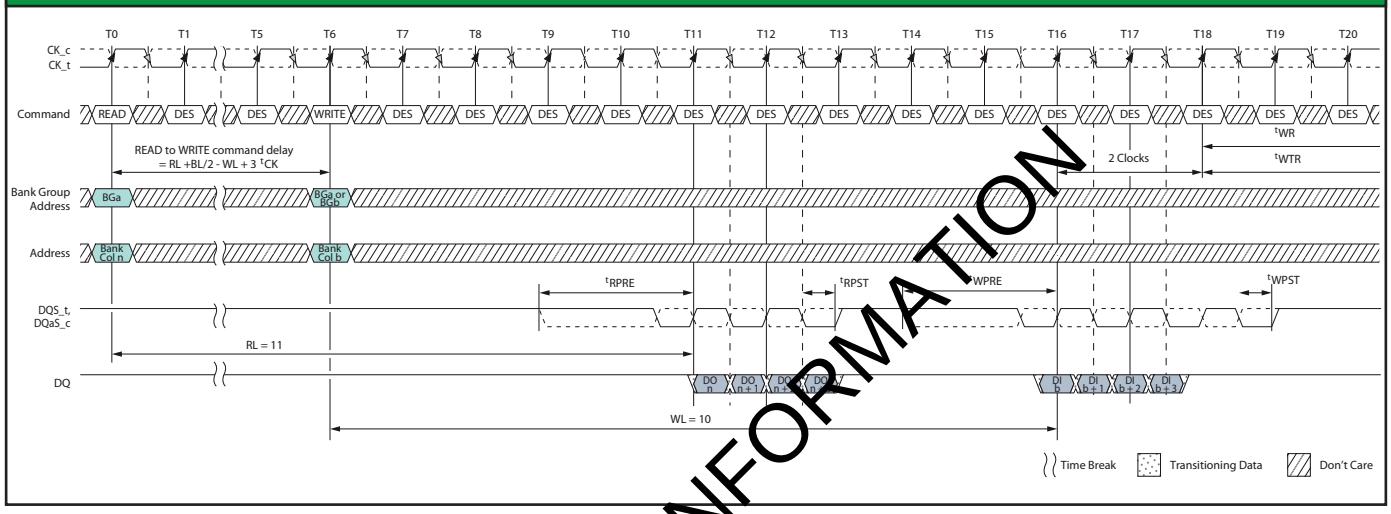
FIGURE 175: READ (BC4) FIXED TO WRITE (BC4) FIXED WITH 1TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.

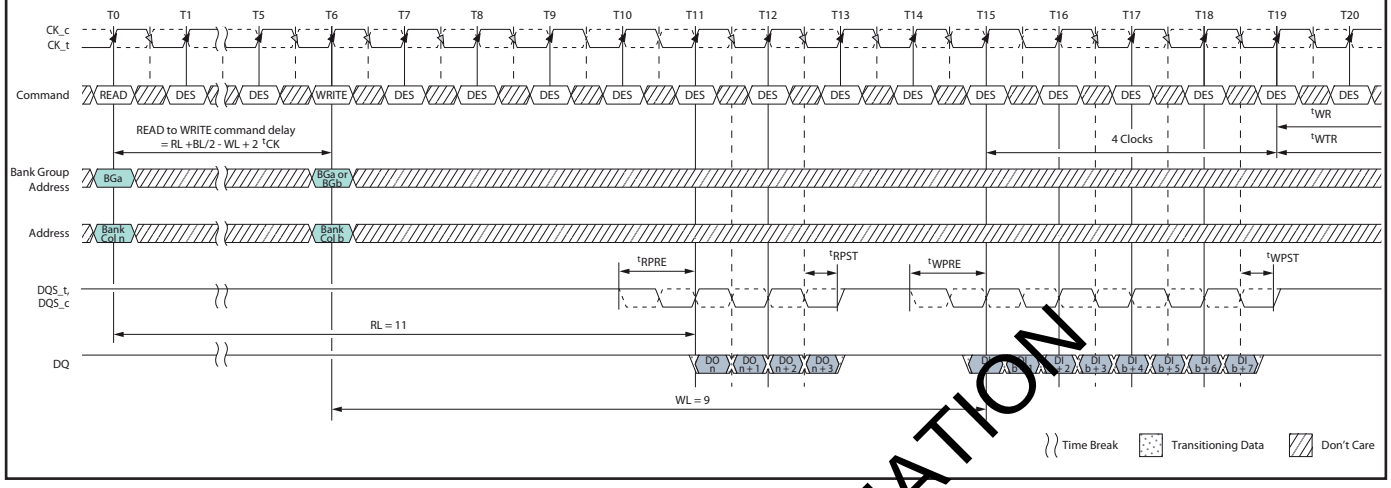
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 01.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 176: READ (BC4) Fixed to WRITE (BC4) Fixed with 2TCK Preamble in Same or Different Bank Group



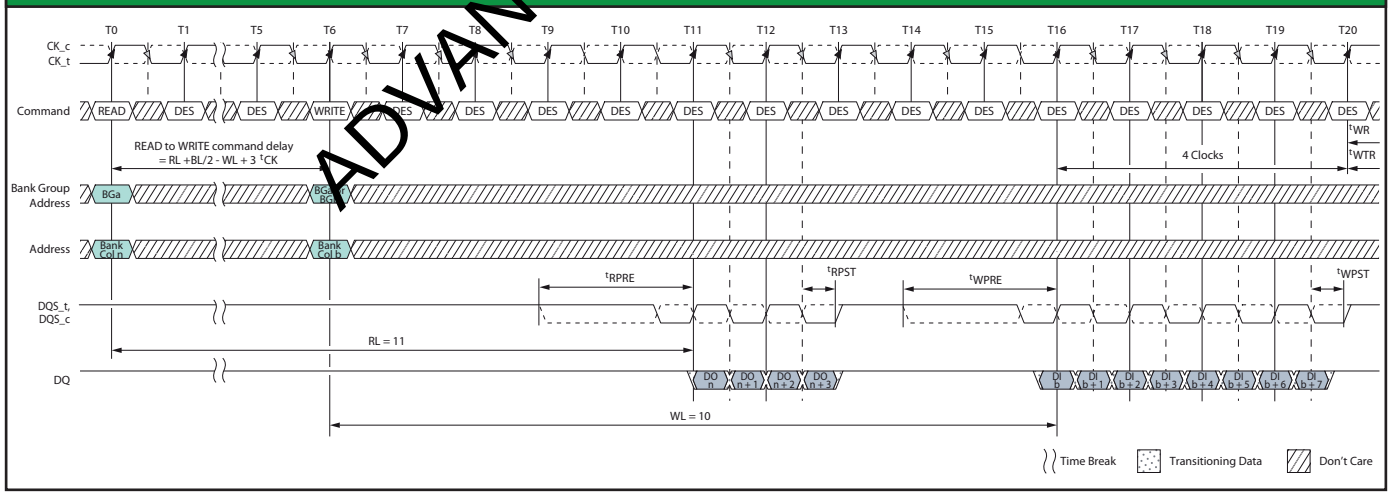
Notes:
1. BC = 4, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 9 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 10.
5. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

FIGURE 177: READ (BC4) TO WRITE (BL8) OTF WITH 1TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

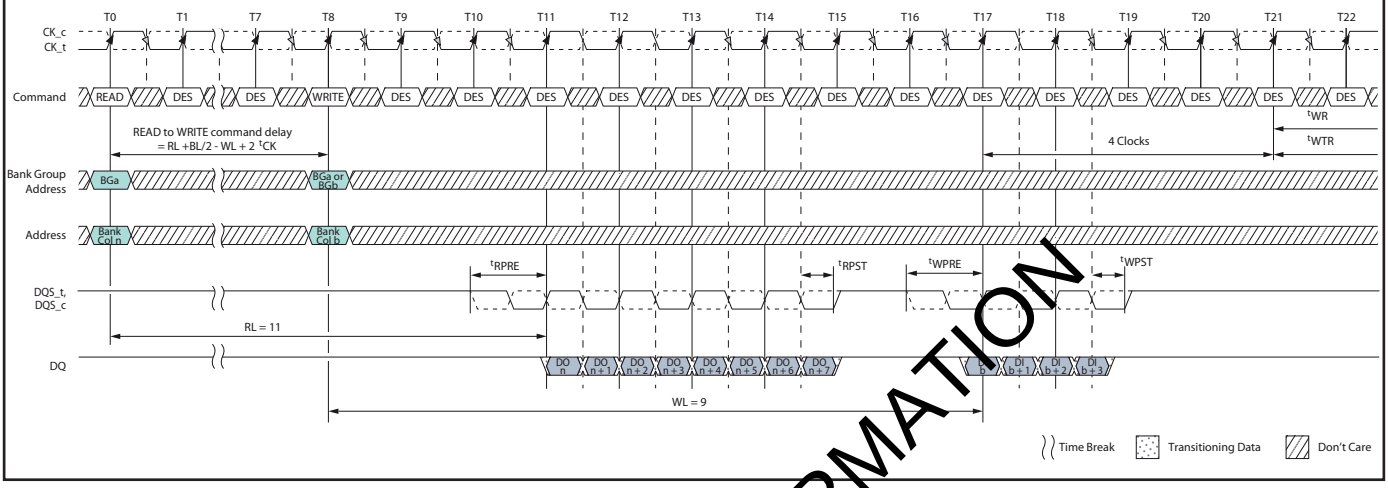
FIGURE 178: READ (BC4) TO WRITE (BL8) OTF WITH 2TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO n = data-out from column n; DI b = data-in from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T6.

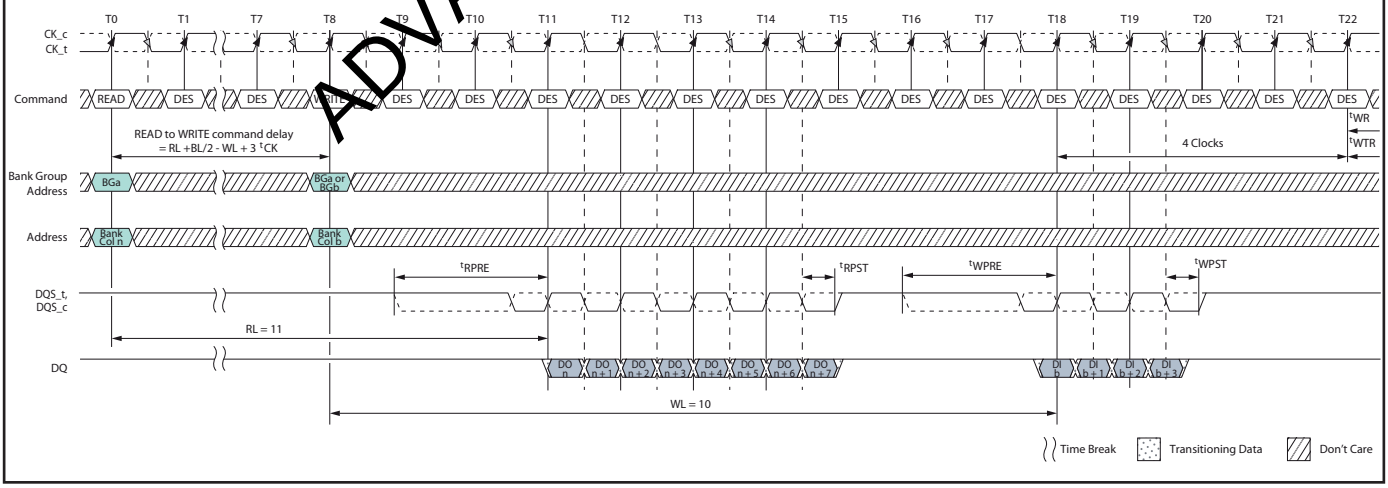
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

FIGURE 179: READ (BL8) TO WRITE (BC4) OTF WITH 1TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

FIGURE 180: READ (BL8) TO WRITE (BC4) OTF WITH 2TCK PREAMBLE IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 2tCK, WL = 10 (CWL = 9 + 1 [see Note 5], AL = 0), WRITE preamble = 2tCK.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

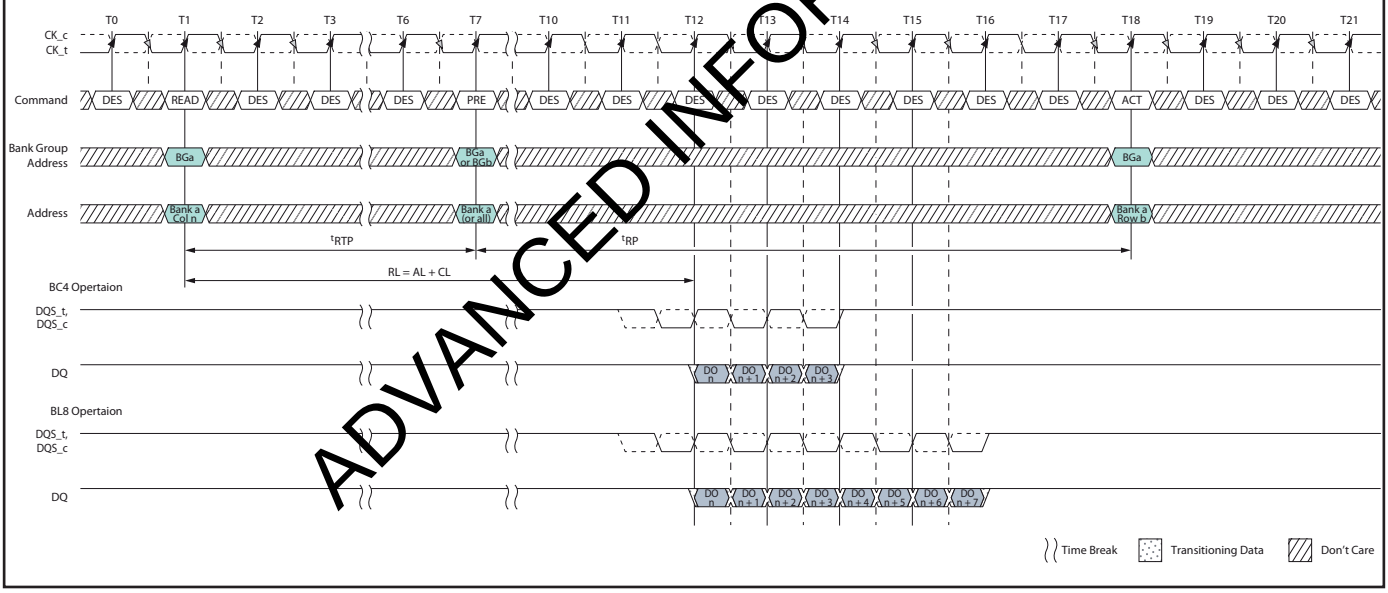
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during READ commands at T0. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
5. 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ Operation Followed by PRECHARGE Operation

The minimum external READ command to PRECHARGE command spacing to the same bank is equal to AL + ^{t}RTP with ^{t}RTP being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, ^{t}RAS, must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by ^{t}RTP (MIN) = MAX (4 × *n*CK, 7.5ns). A new bank ACTIVATE command may be issued to the same bank if the following two conditions are satisfied simultaneously:

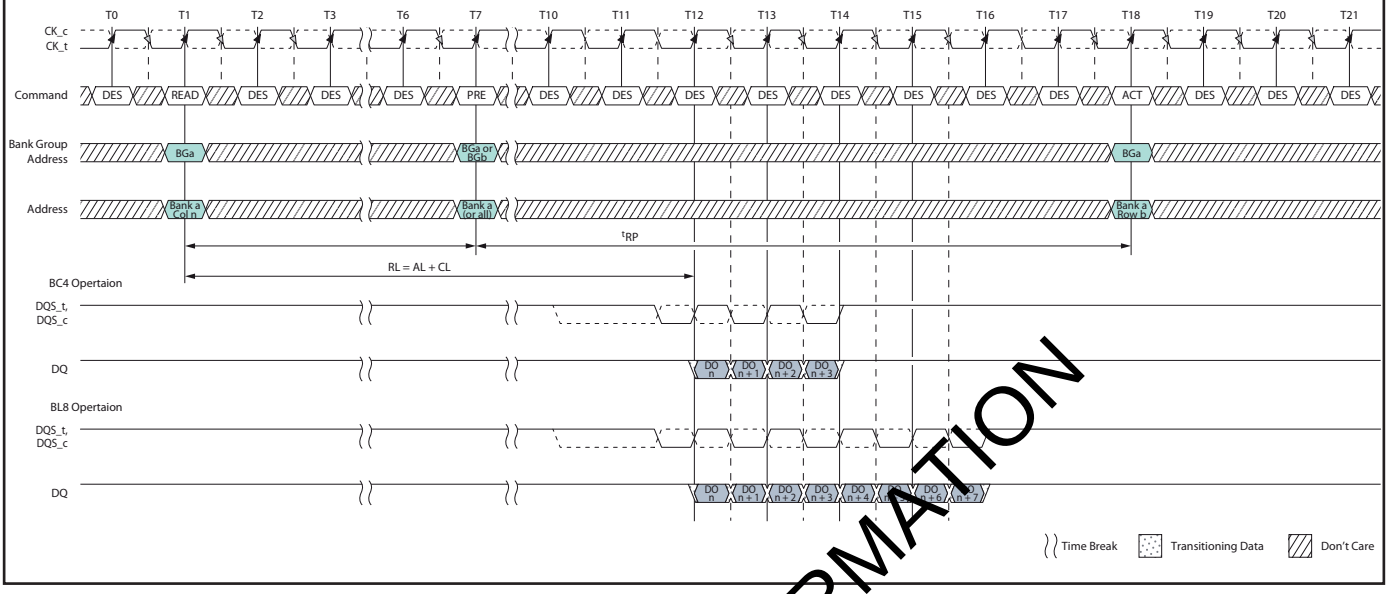
- The minimum RAS precharge time (^{t}RP [MIN]) has been satisfied from the clock at which the precharge begins.
- The minimum RAS cycle time (^{t}RC [MIN]) from the previous bank activation has been satisfied.

Figure 181: READ to PRECHARGE with 1^{T}CK Preamble



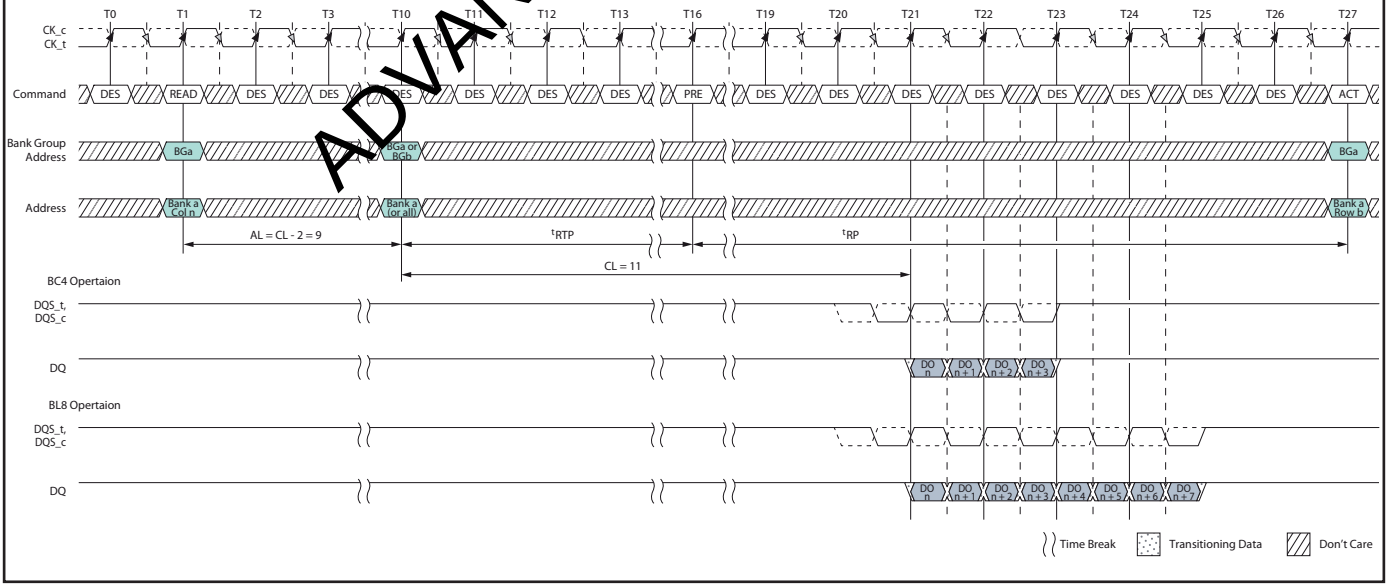
Notes:
1. RL = 11 (CL = 11, AL = 0), Preamble = 1^{t}CK, ^{t}RTP = 6, tRP = 11.
2. 2. DO *n* = data-out from column *n*.
3. 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. 4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T7) and that ^{t}RC (MIN) is satisfied at the next ACTIVATE command time (T18).
5. 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 182: READ TO PRECHARGE WITH 2TCK PREAMBLE



Notes:
1. RL = 11 (CL = 11, AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11.
2. DO n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T7) and that tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

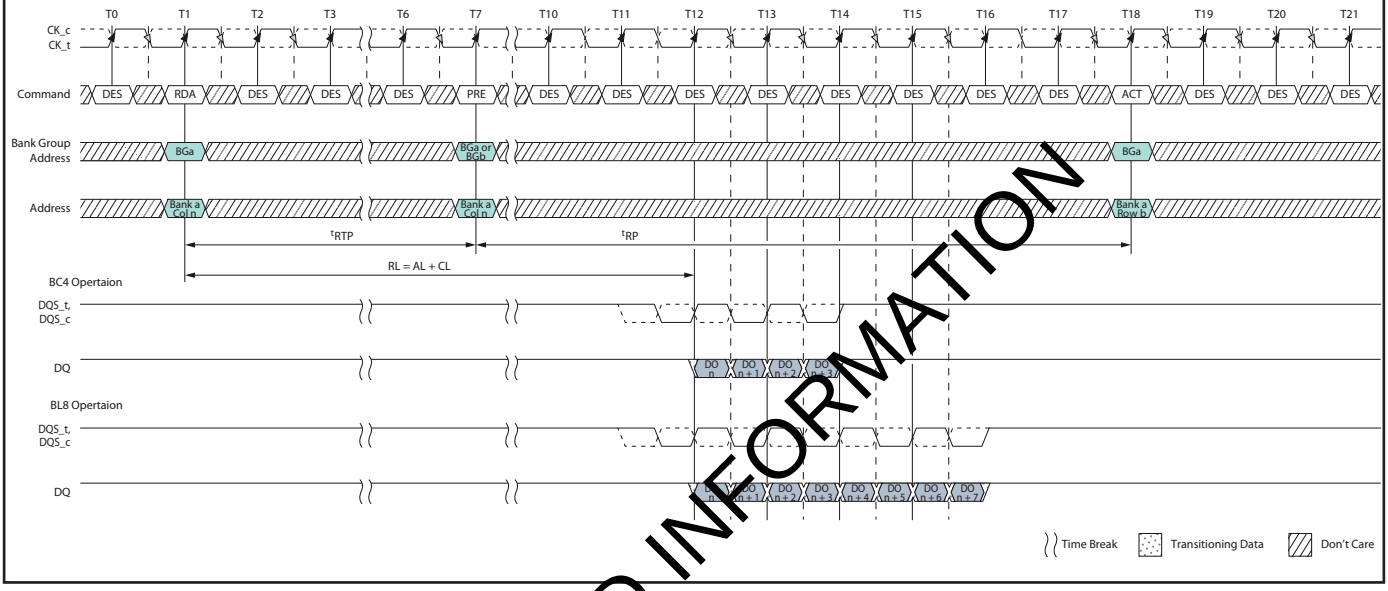
FIGURE 183: READ TO PRECHARGE WITH ADDITIVE LATENCY AND 1TCK PREAMBLE



Notes:
1. RL =20 (CL = 11, AL = CL - 2), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.

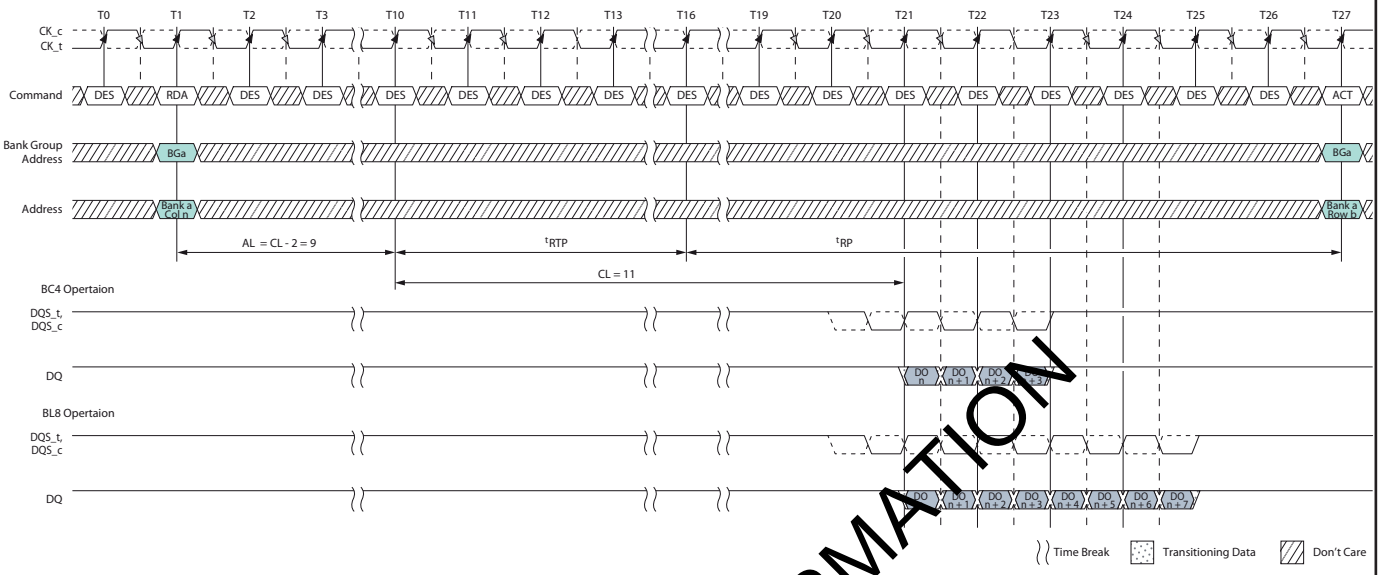
4. DES commands are shown for ease of illustration; other commands may be valid at these times.
5. 4. The example assumes that tRAS (MIN) is satisfied at the PRECHARGE command time (T16) and that tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
5. 5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

FIGURE 184: READ WITH AUTO PRECHARGE AND 1TCK PREAMBLE



Notes:
1. RL = 11 (CL = 11, AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001].
5. The example assumes that tRC (MIN) is satisfied at the next ACTIVATE command time (T18).
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

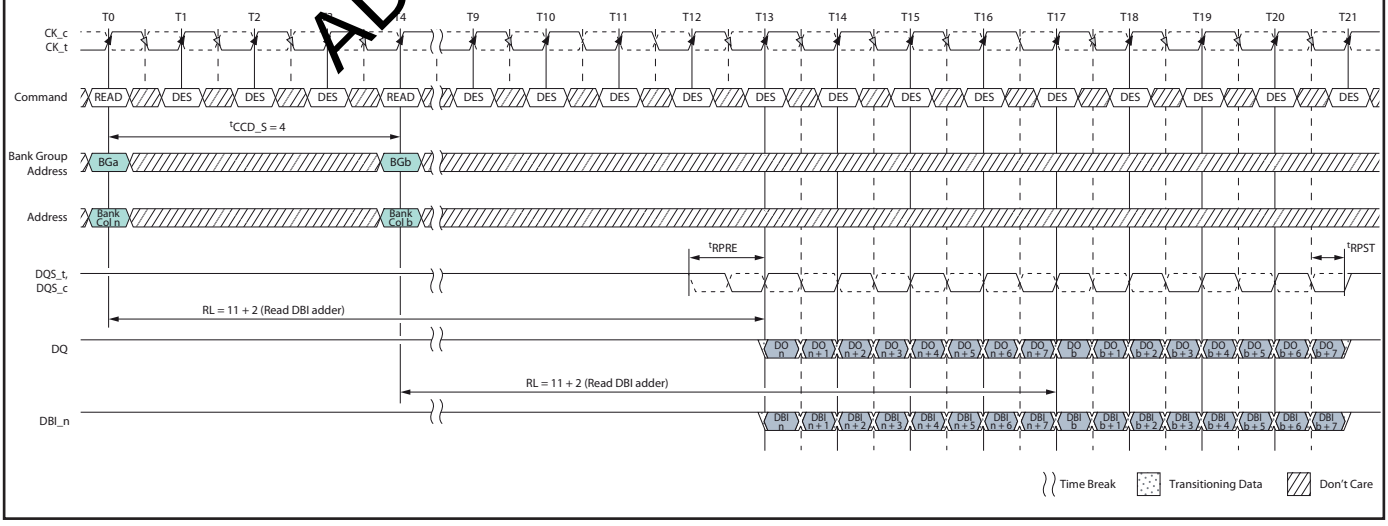
FIGURE 185: READ WITH AUTO PRECHARGE, ADDITIVE LATENCY, AND 1TCK PREAMBLE



Notes:
1. RL = 20 (CL = 11, AL = CL - 2), Preamble = 1tCK, tRTP = 6, tRP = 11.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[11:9] = 001.
5. The example assumes that tRC (MIN) is satisfied at the next ACTIVATE command time (T27).
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Operation with Read Data Bus Inversion (DBI)

FIGURE 186: CONSECUTIVE READ (BL8) WITH 1TCK PREAMBLE AND DBI IN DIFFERENT BANK GROUP

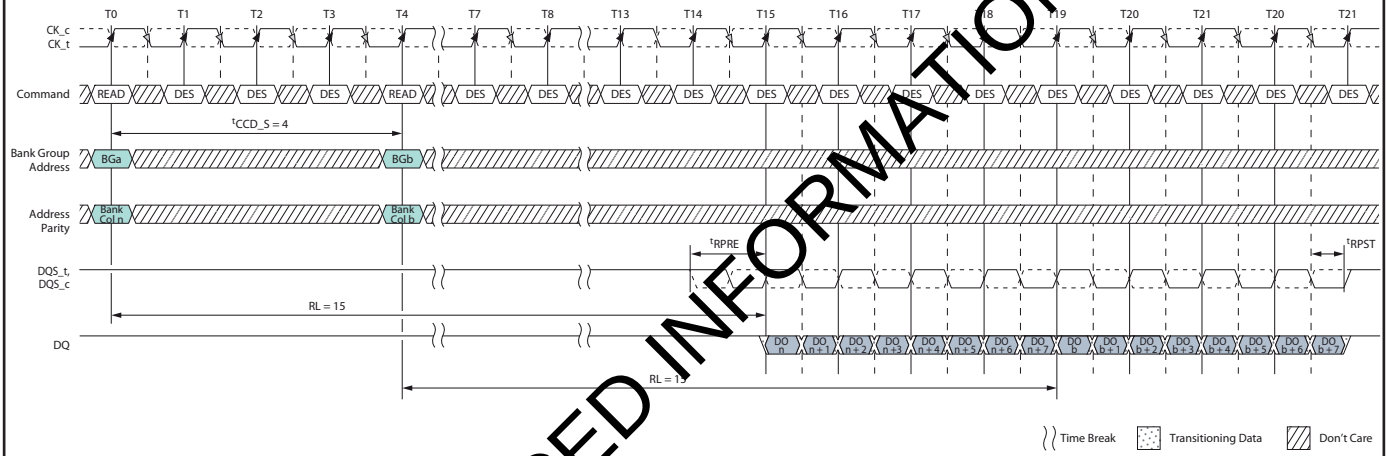


Notes:
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, RL = 11 + 2 (Read DBI adder).

2. DO *n* (or *b*) = data-out from column *n* (or b); DBI *n* (or *b*) = data bus inversion from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Enable.

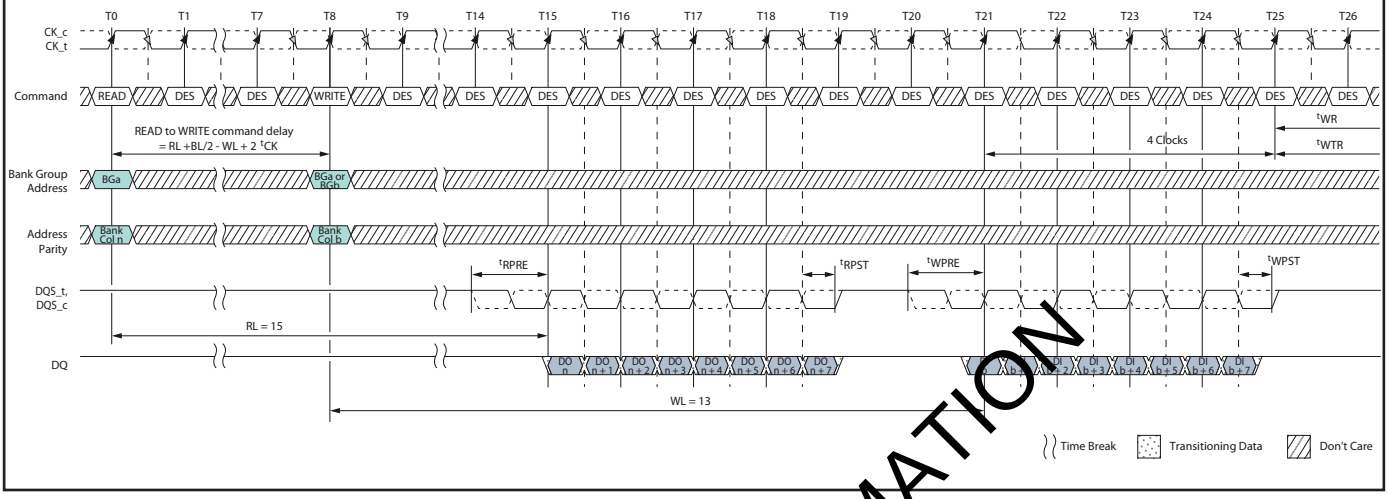
READ Operation with Read Data Bus Inversion (DBI)

FIGURE 187: CONSECUTIVE READ (BL8) WITH 1TCK PREAMBLE AND CA PARITY IN DIFFERENT BANK GROUP



Notes:
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 01] and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable.

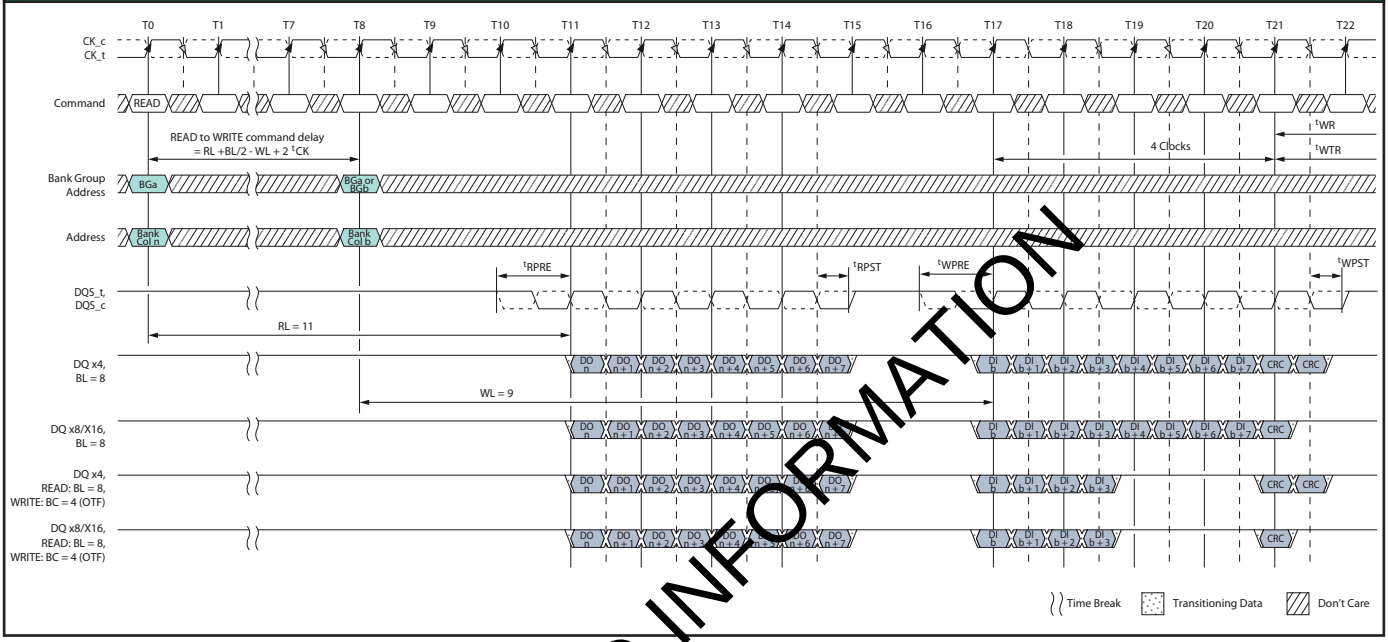
Figure 188: READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA Parity in Same or Different Bank Group



Notes:
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), READ preamble = 1tCK, CWL = 9, AL = 0, PL = 4, (WL = CL + AL + PL = 13), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE command at T8.
5. CA parity = Enable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

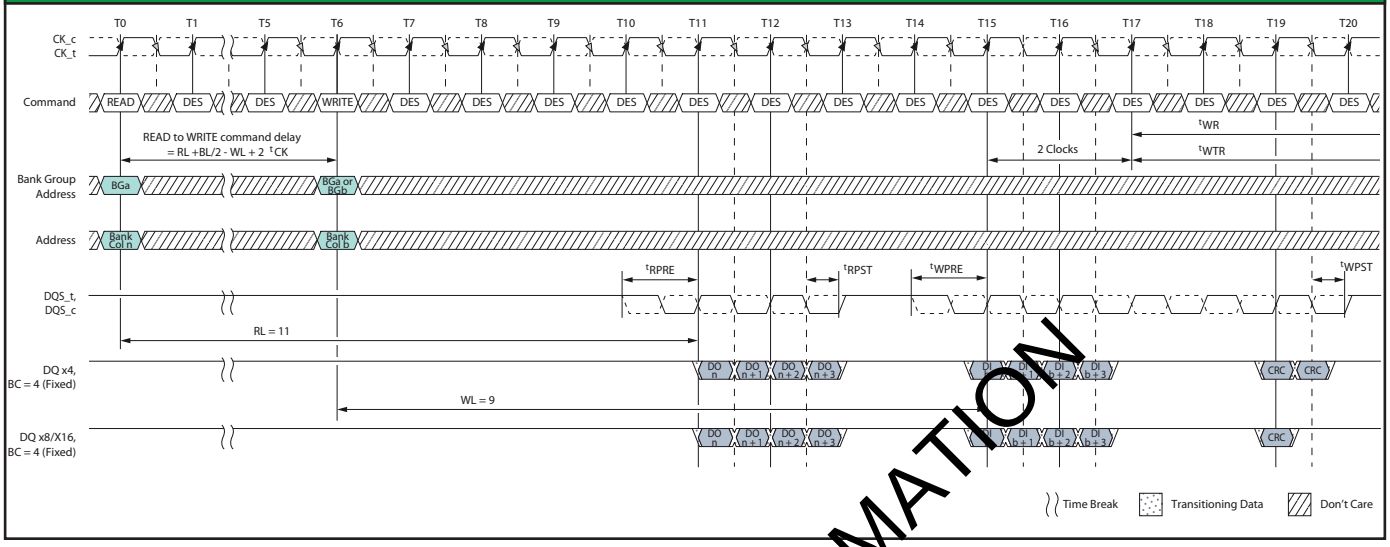
READ Followed by WRITE with CRC Enabled

FIGURE 189: READ (BL8) TO WRITE (BL8 OR BC4: OTF) WITH 1TCK PREAMBLE AND WRITE CRC IN SAME OR DIFFERENT BANK GROUP



Notes:
1. BL = 8 (or BC = 4: OTF for Write), RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and WRITE commands at T8.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T8.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

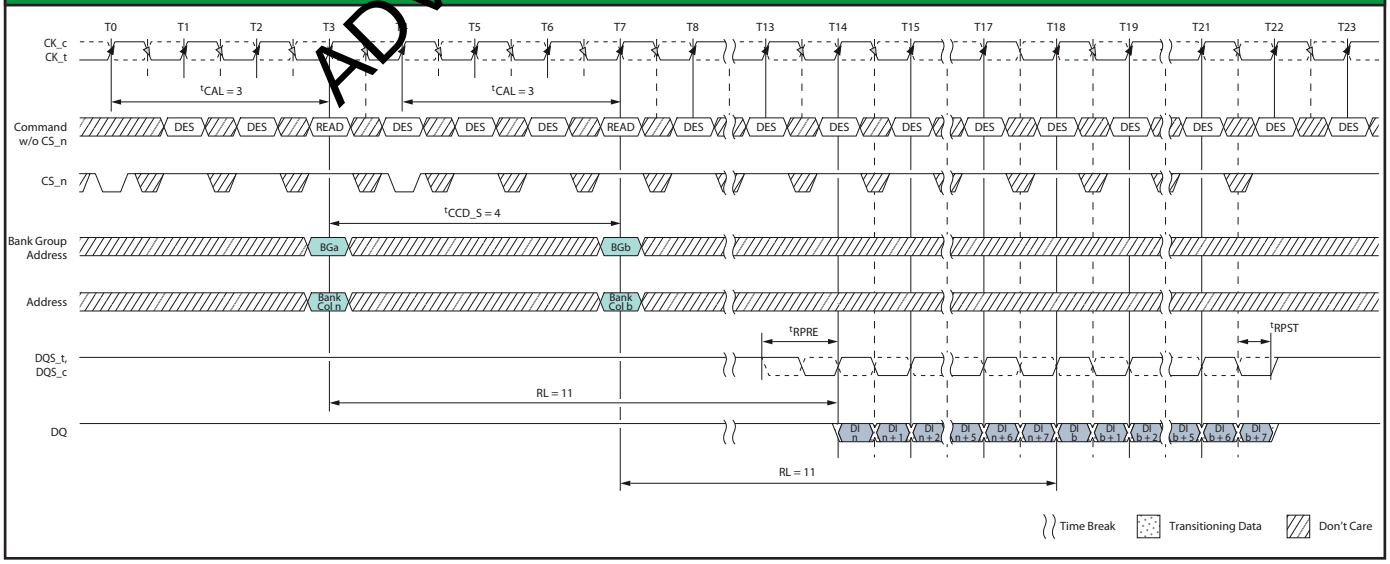
Figure 190: READ (BC4: Fixed) to WRITE (BC4: Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Notes:
1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), WRITE preamble = 1tCK.
2. DO *n* = data-out from column *n*, DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

READ Operation with Command/Address Latency (CAL) Enabled

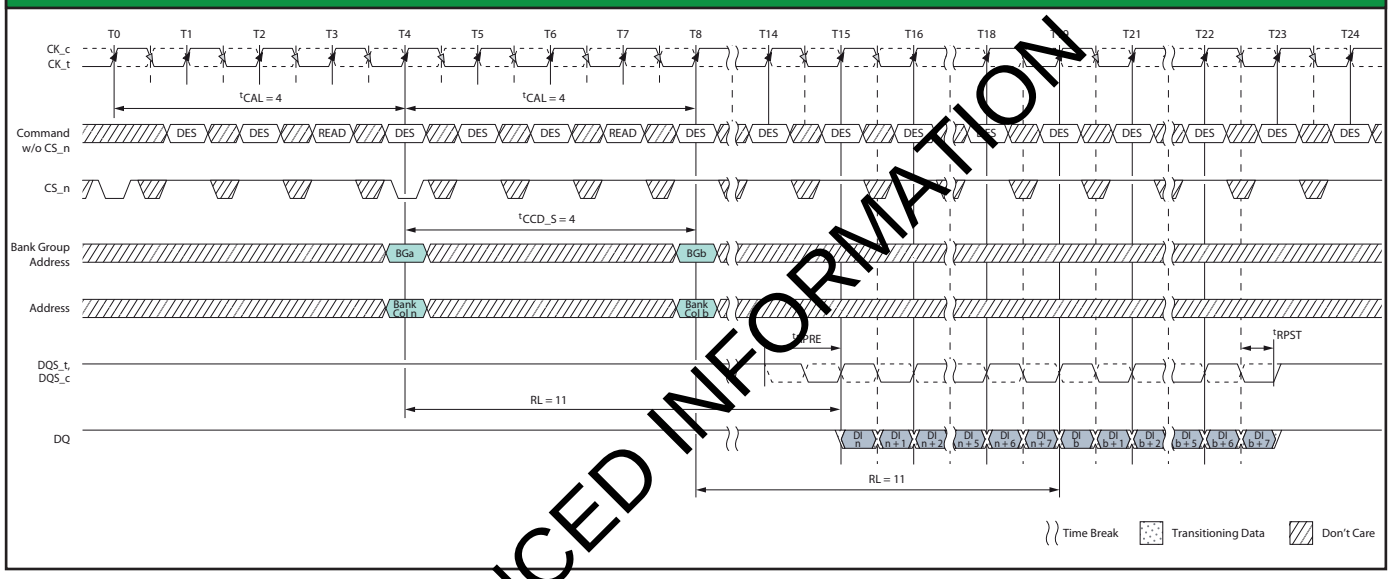
Figure 191: Consecutive READ (BL8) with CAL (3tCK) and 1tCK Preamble in Different Bank Group



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.

2. DI n (or b) = data-in from column n (or b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T7.
5. CA parity = Enable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

Figure 192: Consecutive READ (BL8) with CAL (4tCK) and 1tCK Preamble in Different Bank Group



Notes:
1. BL = 8, RL = 11 (CL = 11, AL = 0), READ preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T3 and T8.
5. CA parity = Enable, CS to CA latency = Enable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. Enabling CAL mode does not impact ODT control timings. The same timing relationship relative to the command/address bus as when CAL is disabled should be maintained.

WRITE Operation

Write Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is, when the DLL is enabled and locked.

Write Timing – Clock-to-Data Strobe Relationship

The clock-to-data strobe relationship is shown below and is applicable in normal oper-ation mode, that is, when the DLL is enabled and locked.

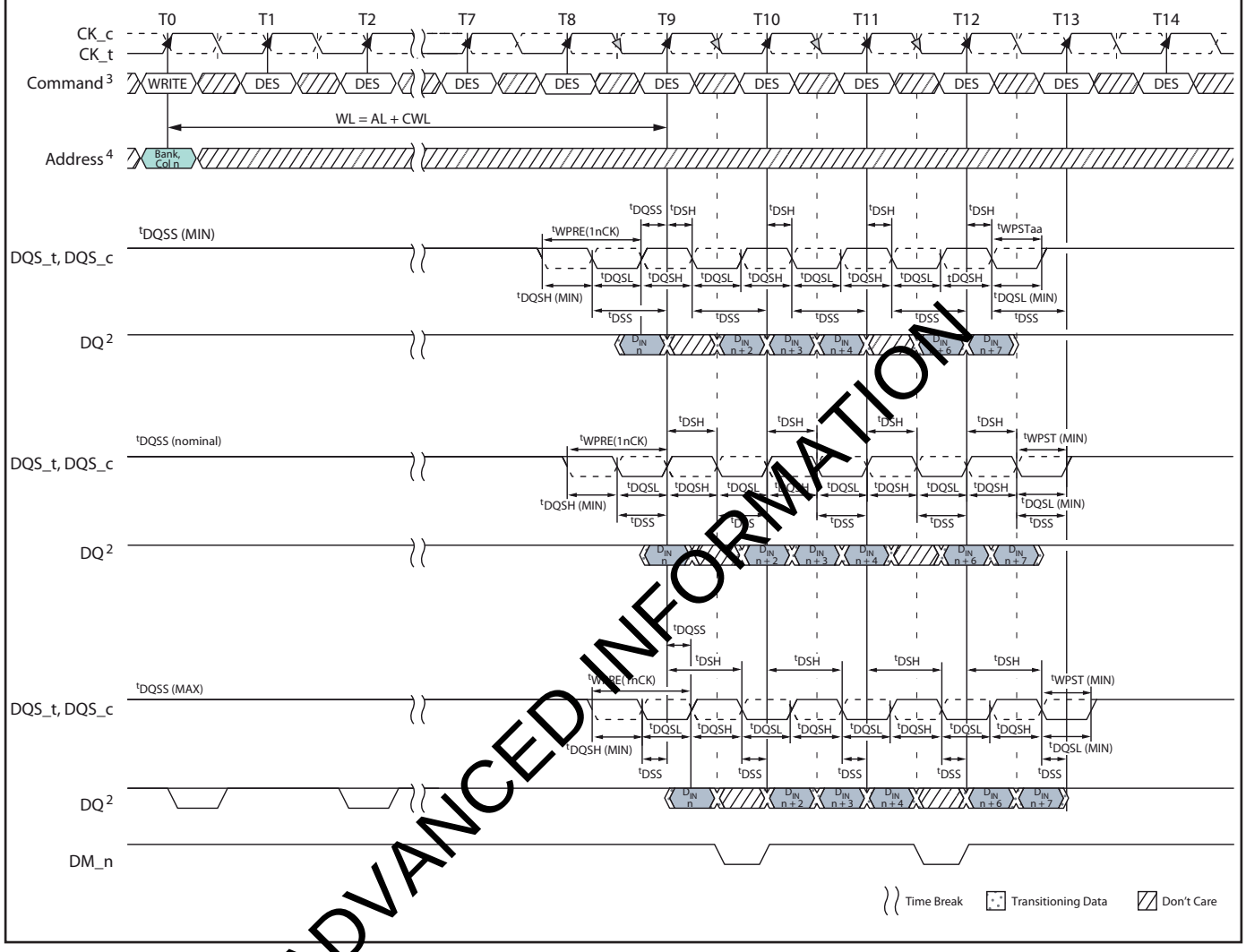
Rising data strobe edge parameters:

- ^{t}DQSS (MIN) to ^{t}DQSS (MAX) describes the allowed range for a rising data strobe edge relative to CK.
- ^{t}DQSS is the actual position of a rising strobe edge relative to CK.
- ^{t}DQSH describes the data strobe high pulse width.
- ^{t}WPST strobe going to HIGH, nondrive level (shown in the postamble section of the graphic below).

Falling data strobe edge parameters:

- ^{t}DQSL describes the data strobe low pulse width.
- ^{t}WPRE strobe going to LOW, initial drive level (shown in the preamble section of the graphic below).

Figure 193: Write Timing Definition

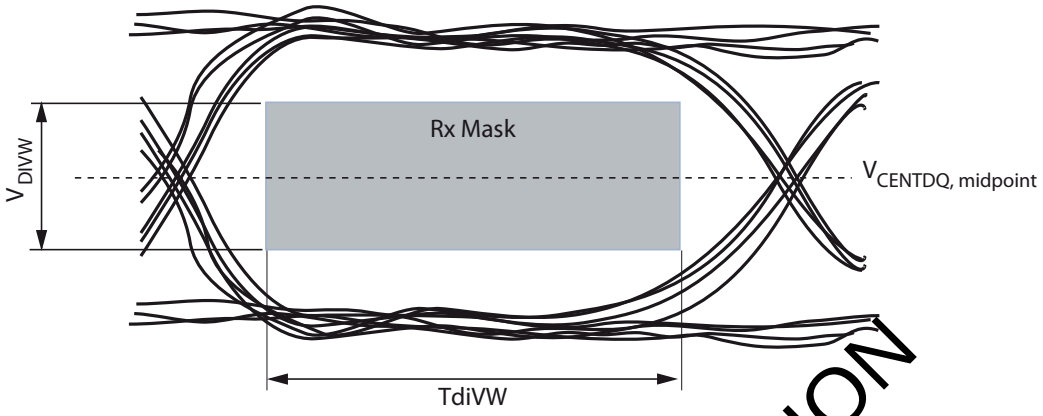


Notes:
1. BL8, WL = 9 (AL = 0, CWL = 9).
2. $D_{IN}n$ = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. ^{t}DQSS must be met at each rising clock edge.

Write Timing – Data Strobe-to-Data Relationship

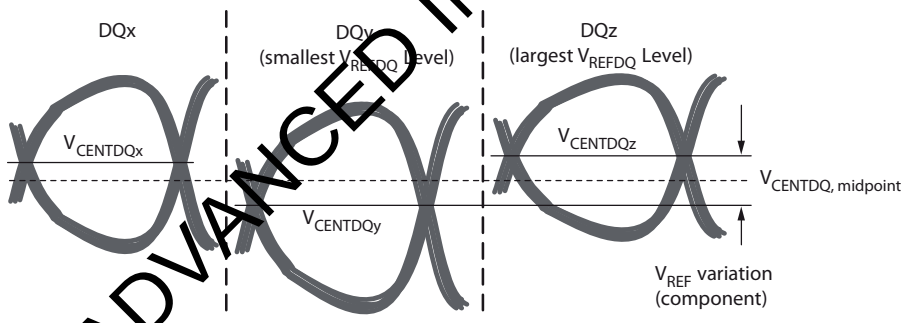
The DQ input receiver uses a compliance mask (Rx) for voltage and timing as shown in the figure below. The receiver mask (Rx mask) defines the area where the input signal must not encroach in order for the DRAM input receiver to be able to successfully capture a valid input signal. The Rx mask is not the valid data-eye. T_{diVW} and V_{diVW} define the absolute maximum Rx mask.

Figure 194: Rx Compliance Mask



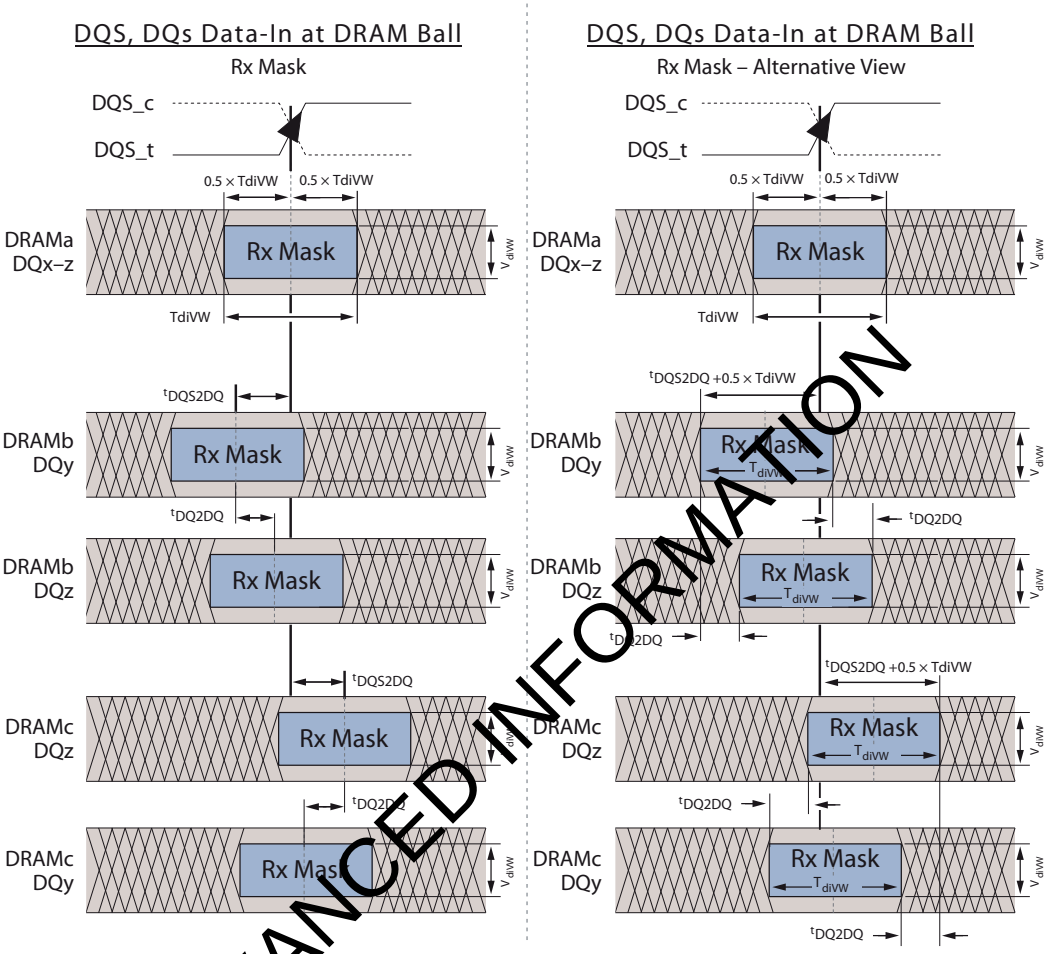
$V_{CENTDQ,midpoint}$ is defined as the midpoint between the largest V_{REFDQ} voltage level and the smallest V_{REFDQ} voltage level across all DQ pins for a given DRAM. Each DQ pin's V_{REFDQ} is defined by the center (widest opening) of the cumulative data input eye as depicted in the following figure. This means a DRAM's level variation is accounted for within the DRAM Rx mask. The DRAM V_{REFDQ} level will be set by the system to account for RON and ODT settings.

Figure 195: V_{CENT_DQ} V_{REFDQ} Voltage Variation



The following figure shows the Rx mask requirements both from a midpoint-to-midpoint reference (left side) and from an edge-to-edge reference. The intent is not to add any new requirement or specification between the two but rather how to convert the relationship between the two methodologies. The minimum data-eye shown in the composite view is not actually obtainable due to the minimum pulse width requirement.

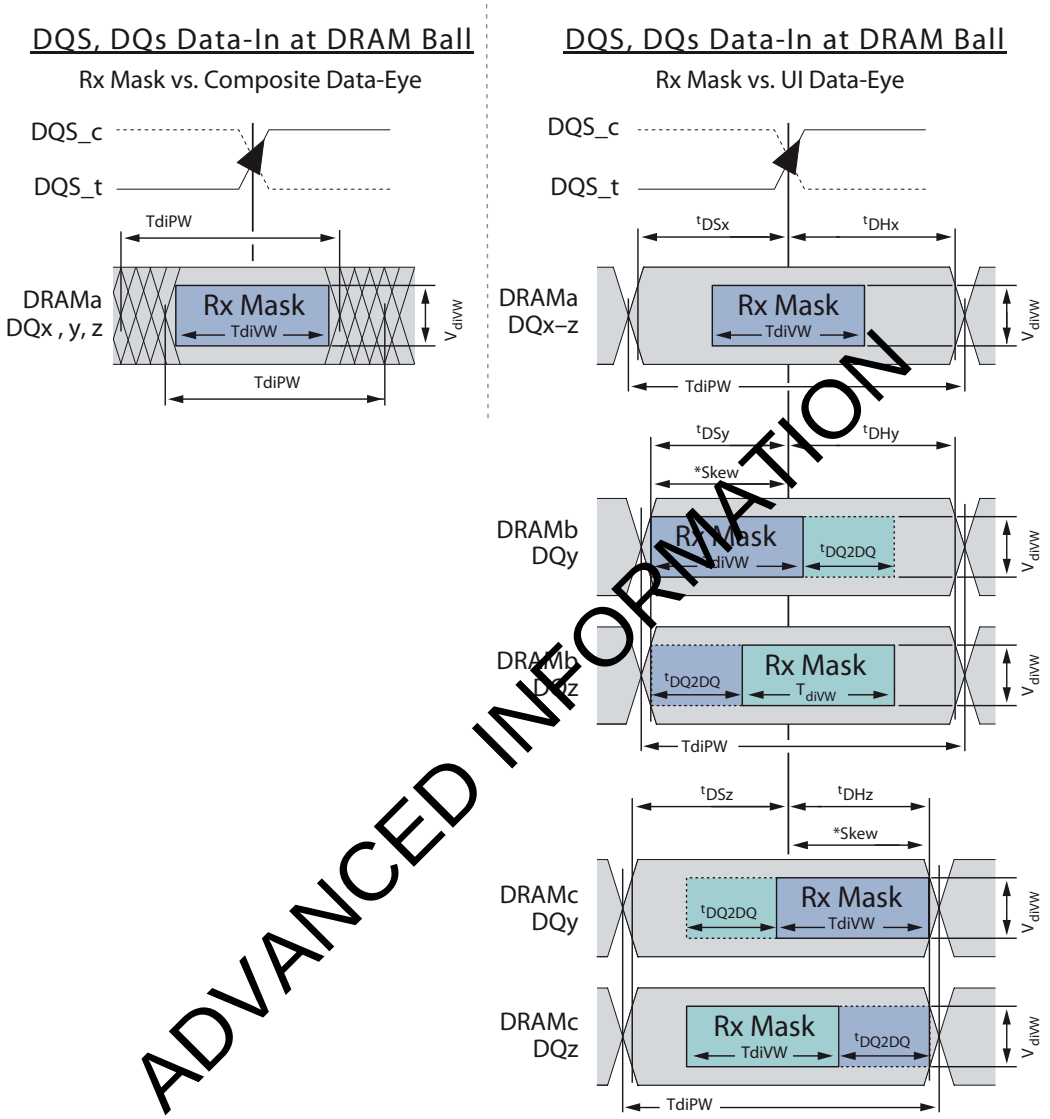
FIGURE 196: RX MASK DQ-TO-DQS TIMINGS



Notes:
1. DQx represents an optimally centered mask.
   DQy represents earliest valid mask.
   DQz represents latest valid mask.
2. DRAMa represents a DRAM without any DQS/DQ skews.
   DRAMb represents a DRAM with early skews (negative ^{t}DQS2DQ).
   DRAMc represents a DRAM with delayed skews (positive ^{t}DQS2DQ).
3. This figure shows the skew allowed between DRAM-to-DRAM and between DQ-to-DQ for a DRAM. Signals assume data is center-aligned at DRAM latch.
   TdiPW is not shown; composite data-eyes shown would violate T_{diPW}.
   $V_{CENTDQ,midpoint}$ is not shown but is assumed to be midpoint of V_{diVW}.

The previous figure shows the basic Rx mask requirements. Converting the Rx mask requirements to a classical DQ-to-DQS relationship is shown in the following figure. It should become apparent that DRAM write training is required to take full advantage of the Rx mask.

FIGURE 197: RX MASK DQ-TO-DQS DRAM-BASED TIMINGS

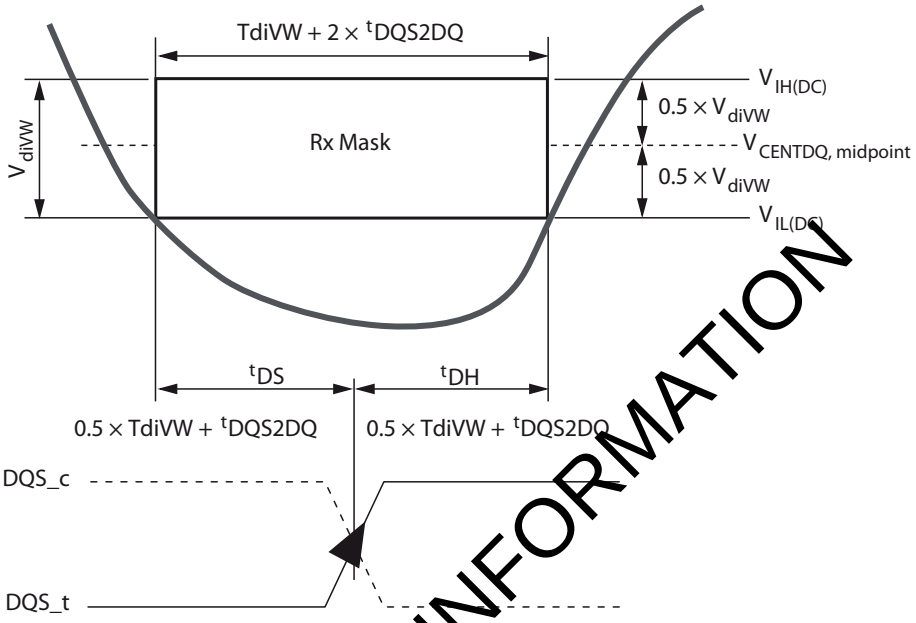


Notes:
1. DQx represents an optimally centered mask.
   DQy represents earliest valid mask.
   DQz represents latest valid mask.
2. *Skew = ^{t}DQS2DQ + 0.5 × TdiVW
   DRAMa represents a DRAM without any DQS/DQ skews.
   DRAMb represents a DRAM with the earliest skews (negative ^{t}DQS2DQ, ^{t}DQSy > *Skew).
   DRAMc represents a DRAM with the latest skews (positive ^{t}DQS2DQ, ^{t}DQHz > *Skew).
3. ^{t}DS/tDH are traditional data-eye setup/hold edges at DC levels.
   ^{t}DS and tDH are not specified; ^{t}DH and ^{t}DS may be any value provided the pulse width and Rx mask limits are not violated.
   ^{t}DH (MIN) > TdiVW + ^{t}DS (MIN) + ^{t}DQ2DQ.

The DDR4 SDRAM's input receivers are expected to capture the input data with an Rx mask of TdiVW provided the minimum pulse width is satisfied. The DRAM controller will have to train the data input buffer to utilize the Rx mask specifications to this maximum benefit.

If the DRAM controller does not train the data input buffers, then the worst case limits have to be used for the Rx mask (TdiVW + 2 × ^{t}DQS2DQ), which will generally be the classical minimum (^{t}DS and ^{t}DH) and is required as well.

FIGURE 198: EXAMPLE OF DATA INPUT REQUIREMENTS WITHOUT TRAINING



WRITE Burst Operation

The following write timing diagrams are intended to help understand each write parameter's meaning and are only examples. Each parameter will be defined in detail separately. In these write timing diagrams, CK and DQS are shown aligned, and DQS and DQ are shown center-aligned for the purpose of illustration.

DDR4 WRITE command supports bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when MR0 is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

WRITE commands can issue precharge automatically with a WRITE with auto precharge (WRA) command, which is enabled by A10 HIGH.

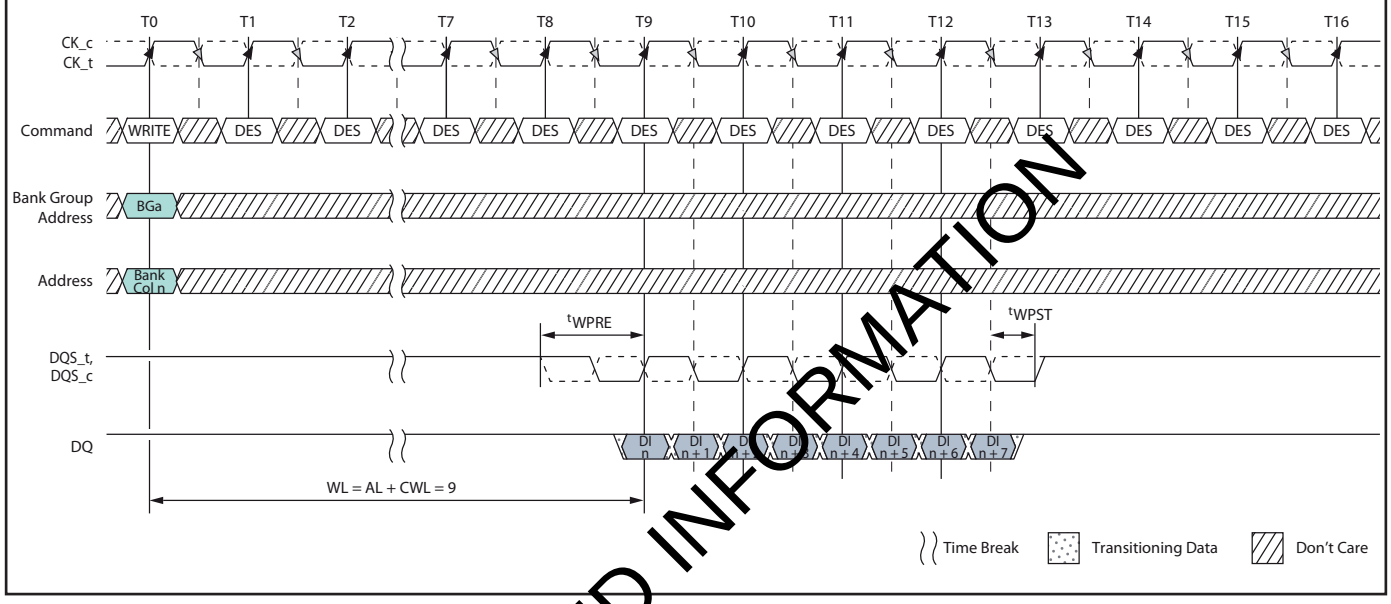
- WRITE command with A10 = 0 (WR) performs standard write, bank remains active after WRITE burst
- WRITE command with A10 = 1 (WRA) performs write with auto precharge, bank goes into precharge after WRITE burst

The DATA MASK (DM) function is supported for the x8 and x16 configurations only (the DM function is not supported on x4 devices). The DM function shares a common pin with the DBI_n and TDQS functions. The DM function only applies to WRITE operations and cannot be enabled at the same time the DBI function is enabled.

- If DM_n is sampled LOW on a given byte lane, the DRAM masks the write data received on the DQ inputs.

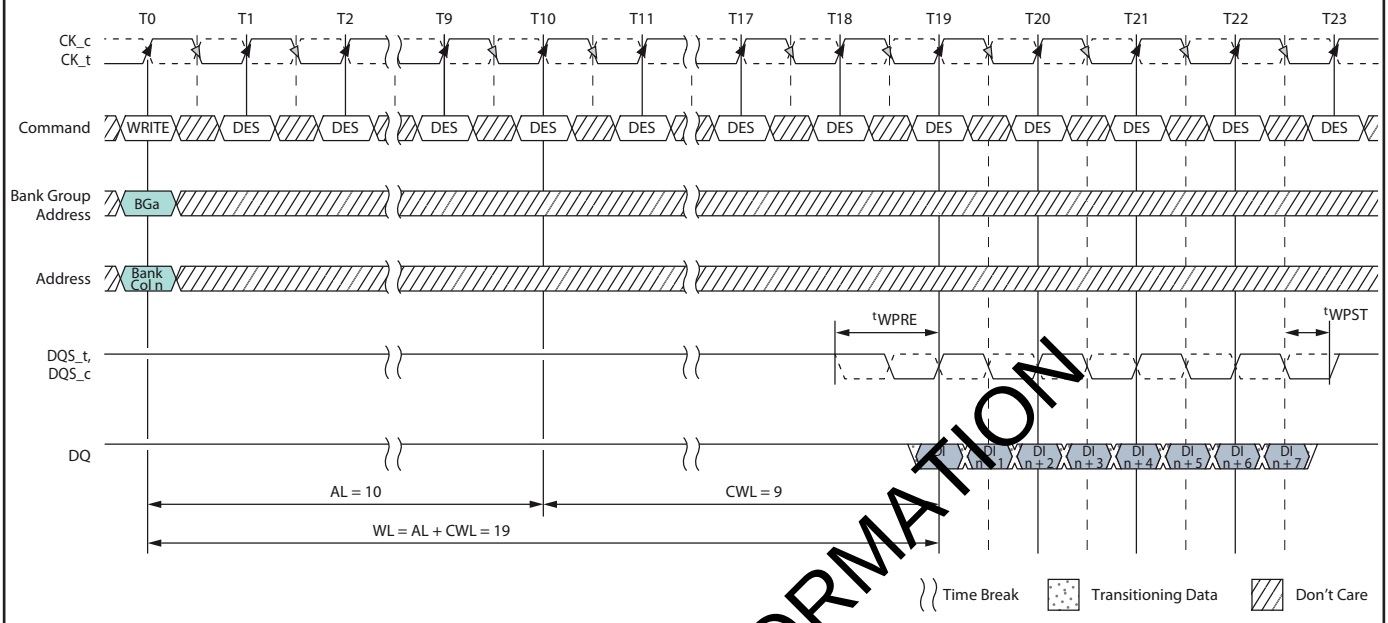
- If DM_n is sampled HIGH on a given byte lane, the DRAM does not mask the data and writes this data into the DRAM core.
- If CRC write is enabled, then DM enabled (via MRS) will be selected between write CRC nonpersistent mode (DM disabled) and write CRC persistent mode (DM enabled).

FIGURE 199: WRITE BURST OPERATION, WL = 9 (AL = 0, CWL = 9, BL8)



Notes:
1. BL8, WL = 0, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* = Data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA atency = Disable, Read DBI = Disable.

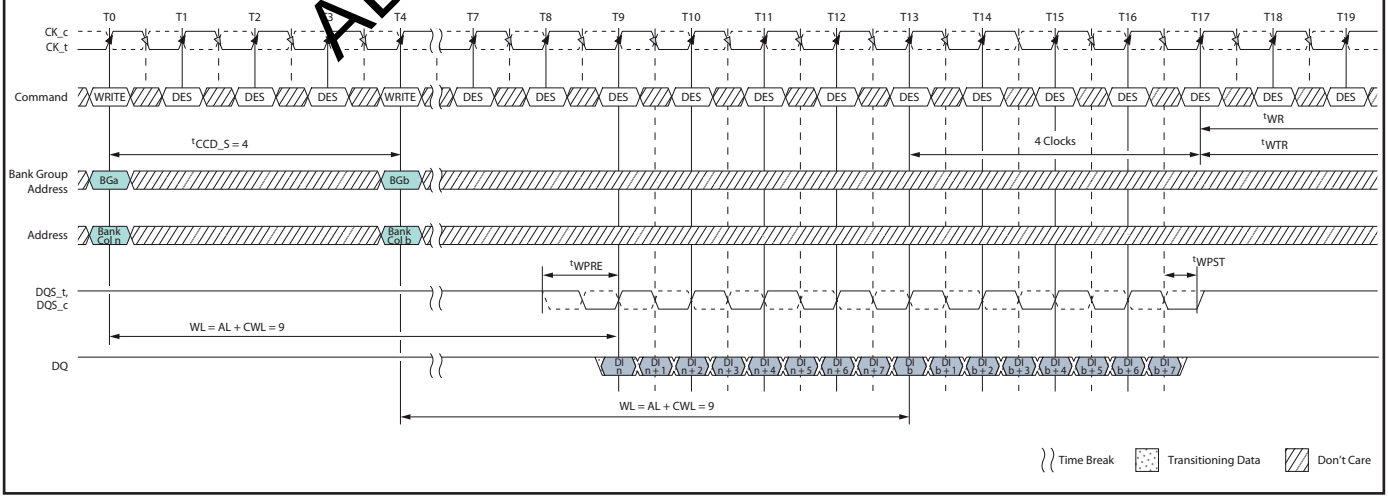
Figure 200: WRITE Burst Operation, WL = 19 (AL = 10, CWL = 9, BL8)



Notes:
1. BL8, WL = 19, AL = 10 (CL - 1), CWL = 9, Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

WRITE Operation Followed by Another WRITE Operation

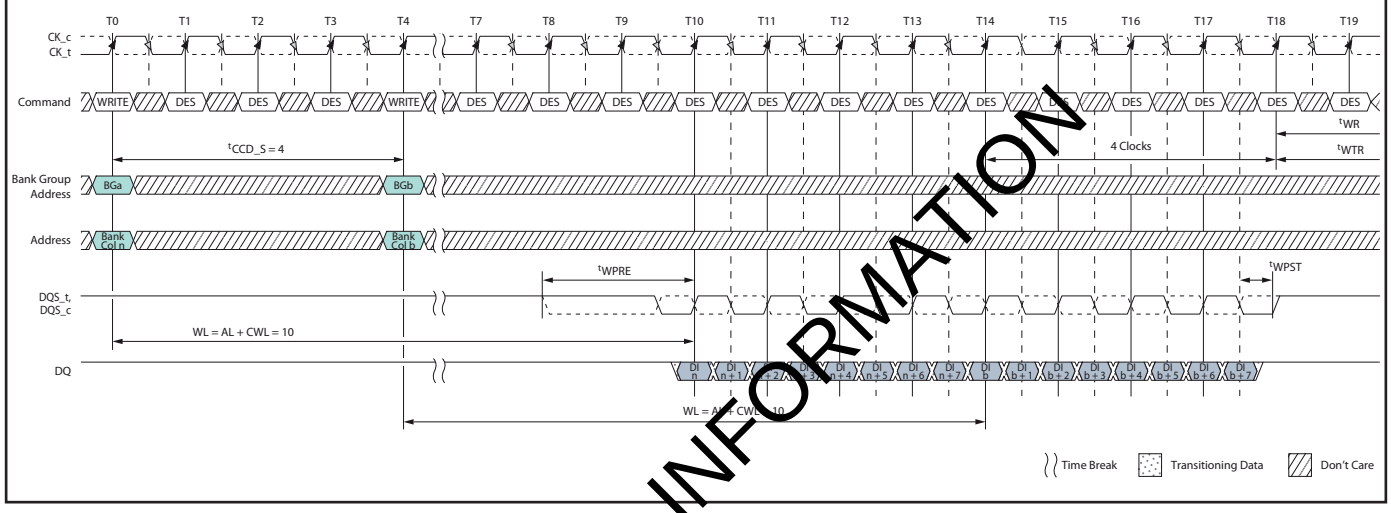
Figure 201: Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



Notes:
1. BL8, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).

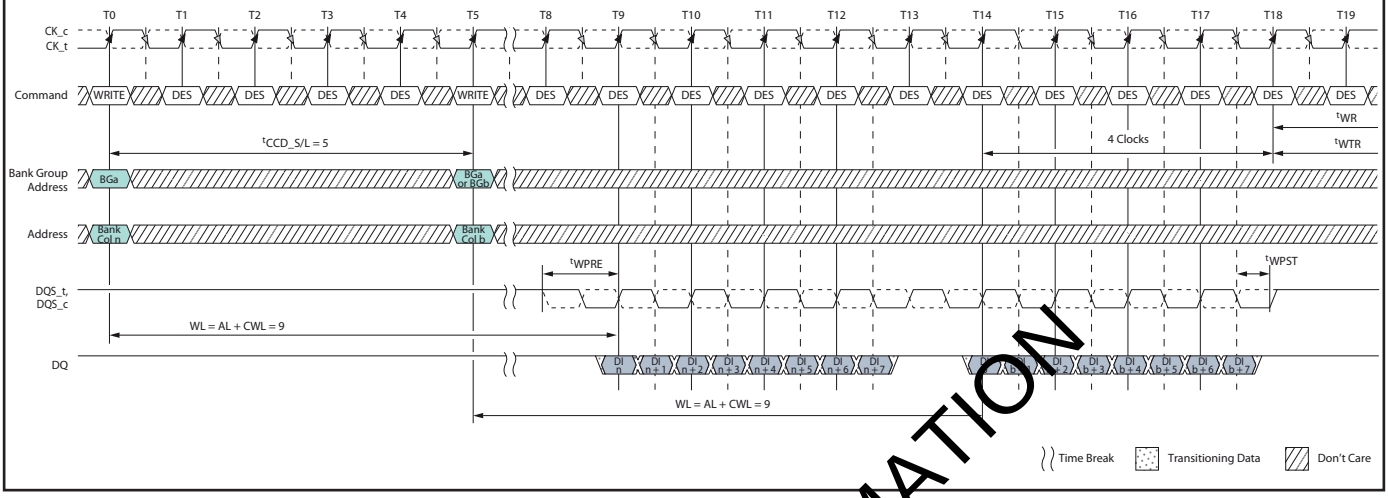
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.

FIGURE 202: CONSECUTIVE WRITE (BL8) WITH 2^{T}CK PREAMBLE IN DIFFERENT BANK GROUP



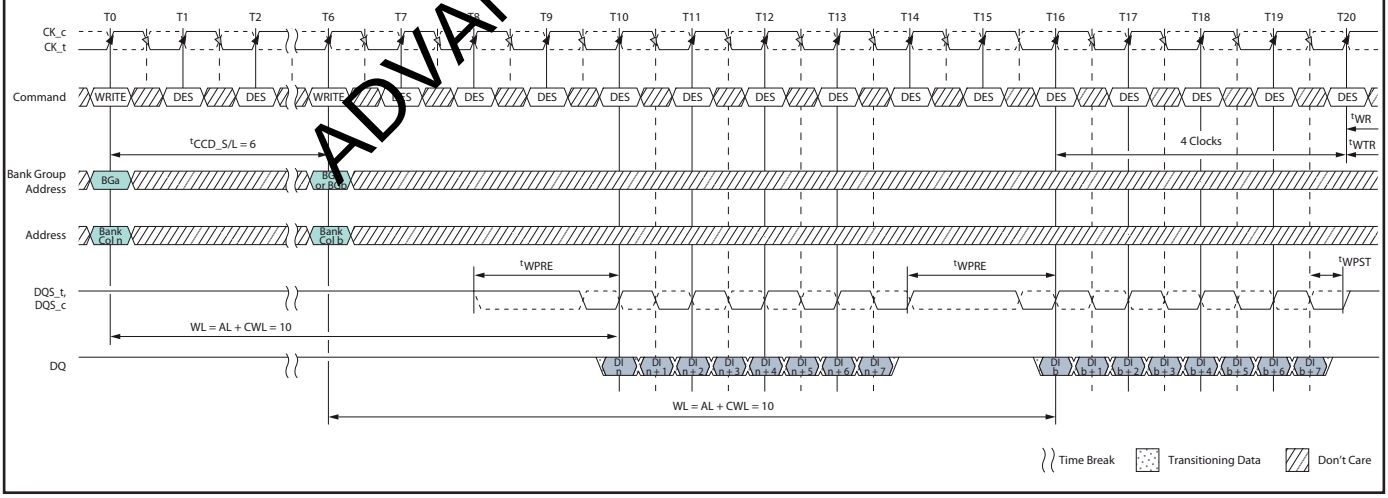
Notes:
1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2^{t}CK.
2. DI n (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.
7. When operating in 2^{t}CK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range, which means CWL = 9 is not allowed when operating in 2^{t}CK WRITE preamble mode.

Figure 203: Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



Notes:
1. BL8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

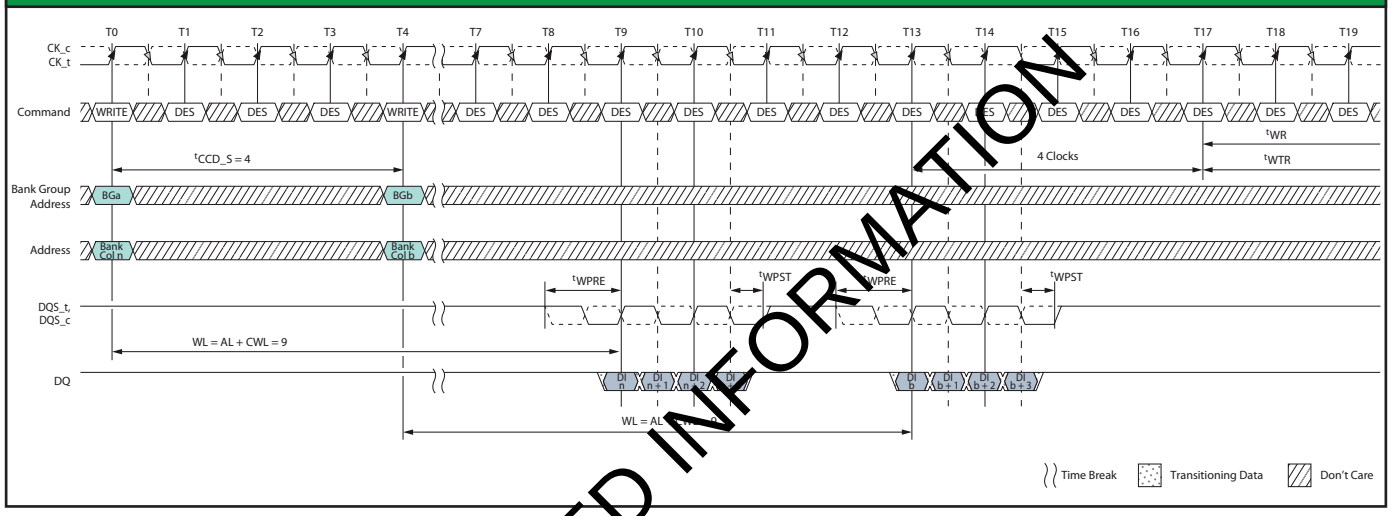
Figure 204: Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



Notes:
1. BL8, AL = 0, CWL = 9 + 1 = 10 (see Note 8), Preamble = 2tCK, tCCD_S/L = 6tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.

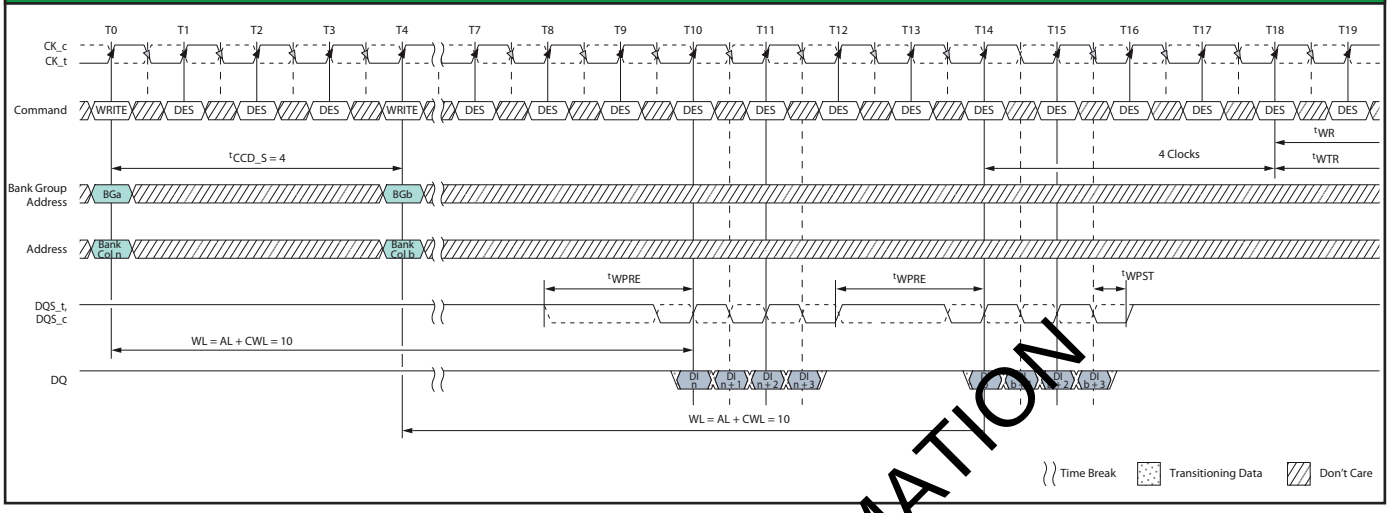
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. ^{t}CCD_S/L = 5 isn't allowed in 2^{t}CK preamble mode.
7. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2^{t}CK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range, which means CWL = 9 is not allowed when operating in 2^{t}CK WRITE preamble mode.

FIGURE 205: WRITE (BC4) OTF TO WRITE (BC4) OTF WITH 1^{T}CK PREAMBLE IN DIFFERENT BANK GROUP



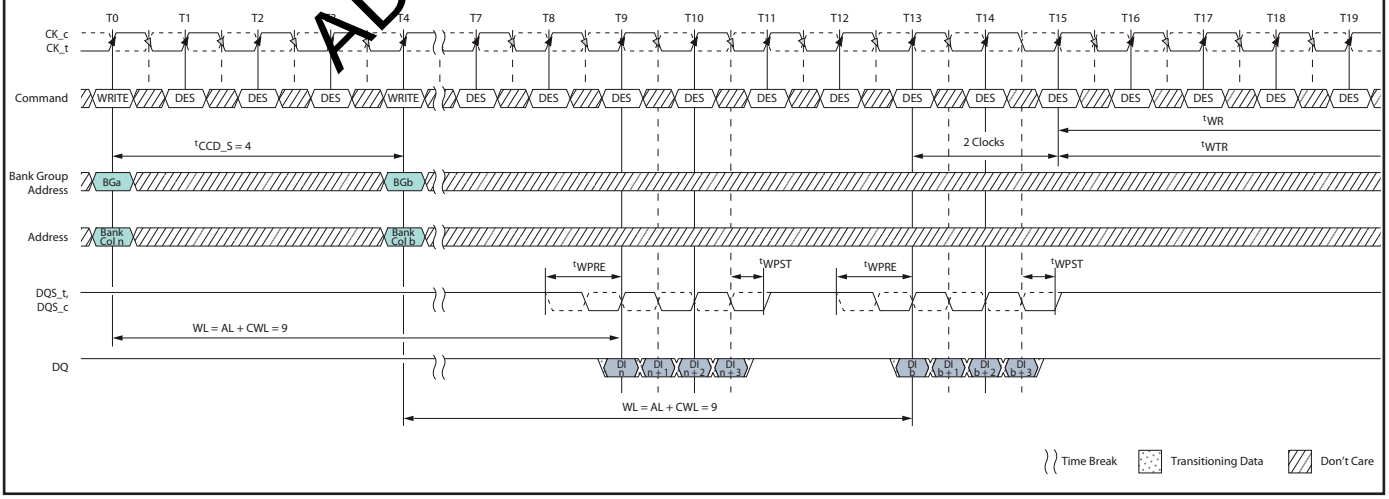
Notes:
1. BC4, AL = 0, CWL = 9, Preamble = 1^{t}CK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (^{t}WR) and write timing parameter (^{t}WTR) are referenced from the first rising clock edge after the last write data shown at T17.

FIGURE 206: WRITE (BC4) OTF TO WRITE (BC4) OTF WITH 2TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BC4, AL = 0, CWL = 9 + 1 = 10 (see Note 7), Preamble = 2tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range, which means CWL = 9 is not allowed when operating in 2tCK WRITE preamble mode.

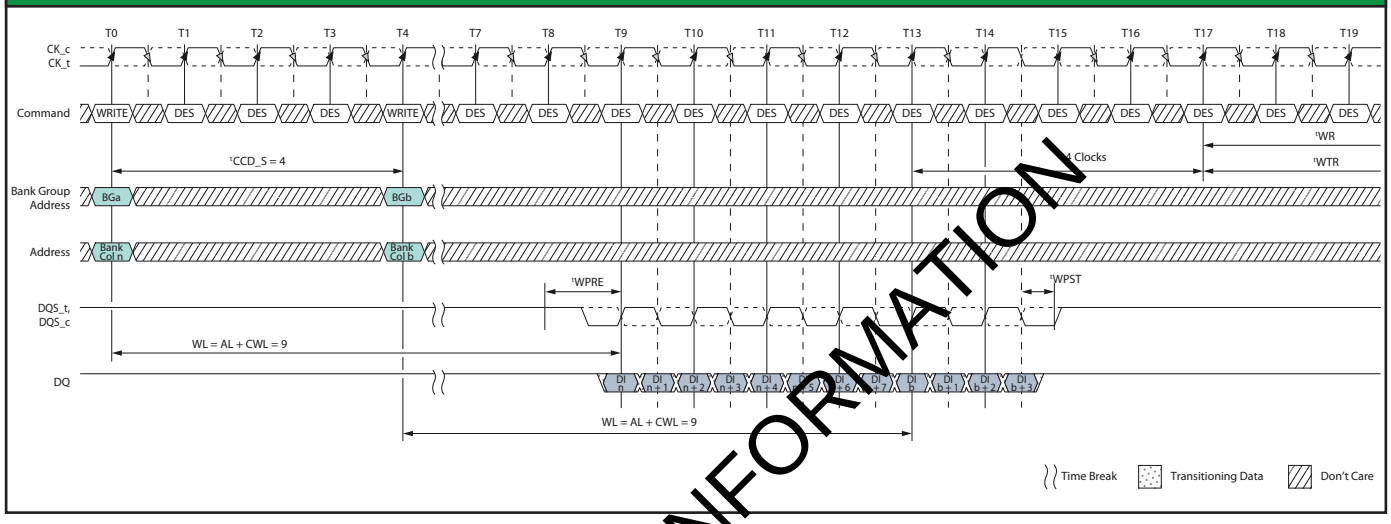
FIGURE 207: WRITE (BC4) FIXED TO WRITE (BC4) FIXED WITH 1TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).

3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 (fixed) setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

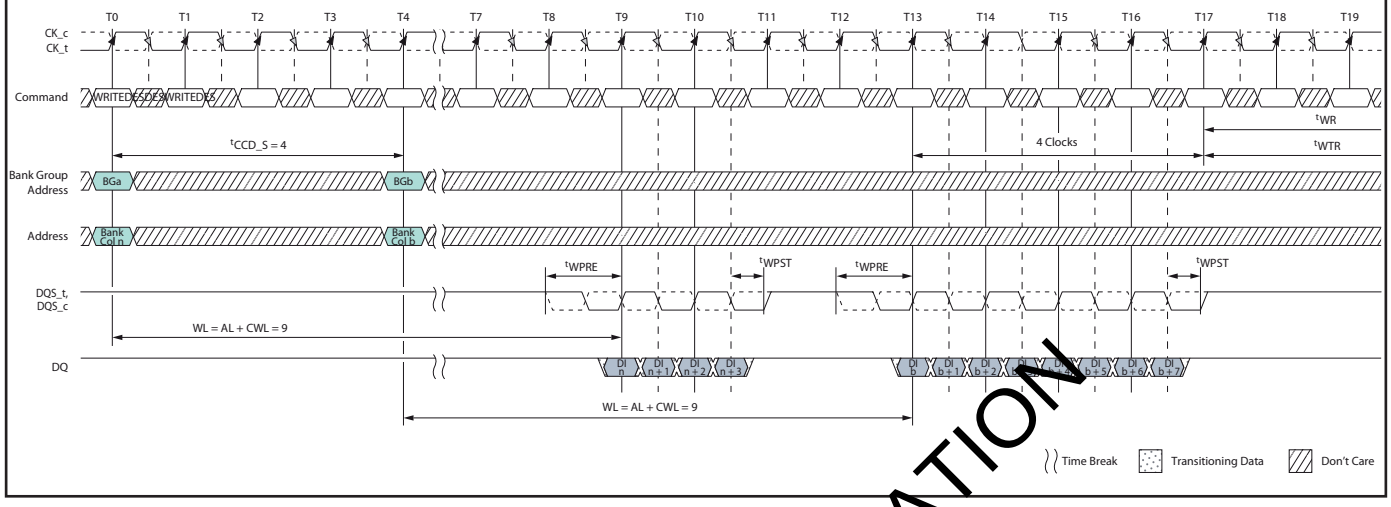
FIGURE 208: WRITE (BL8) TO WRITE (BC4) OTF WITH 1TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.

   BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

Figure 209: WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group

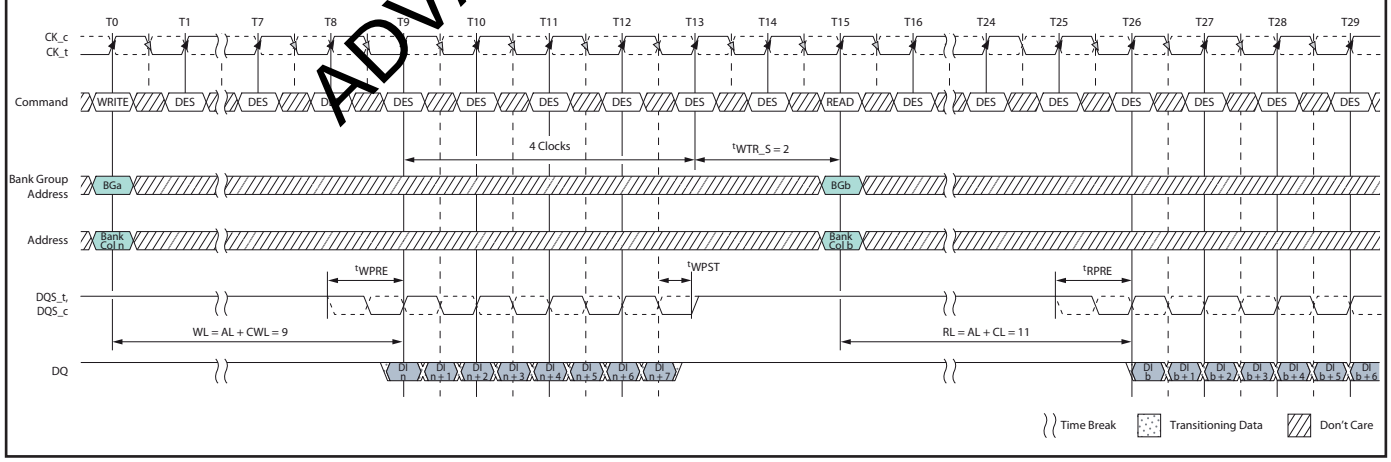


Notes:
1. BL = 8/BC = 4, AL = 0, CL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.

   BL8 setting activated by MR0[1:0] = 01 and A12 = 1 during WRITE command at T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE Operation Followed by READ Operation

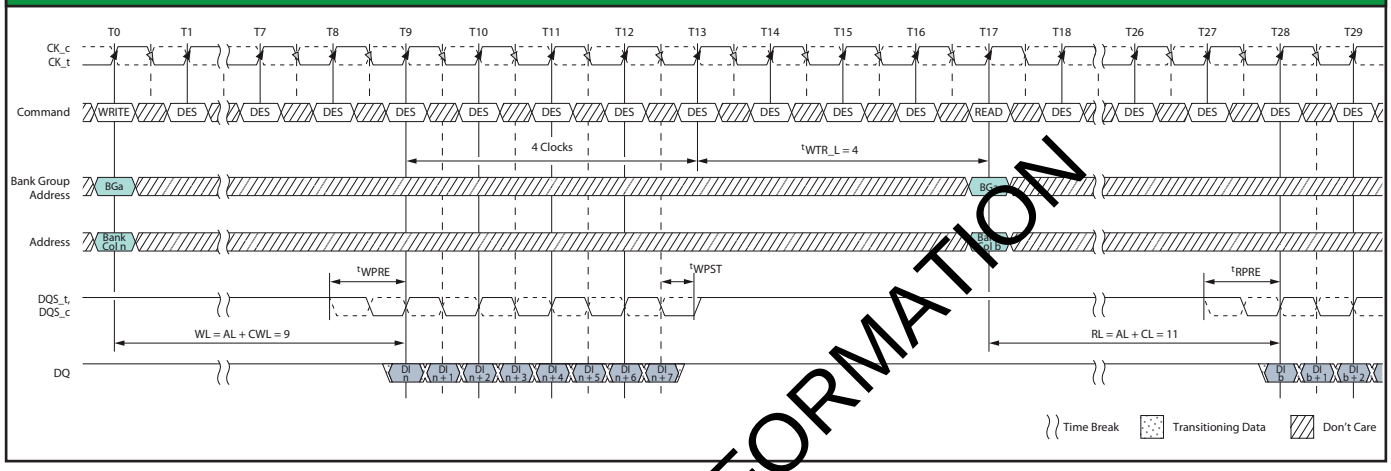
Figure 210: WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



Notes:
1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

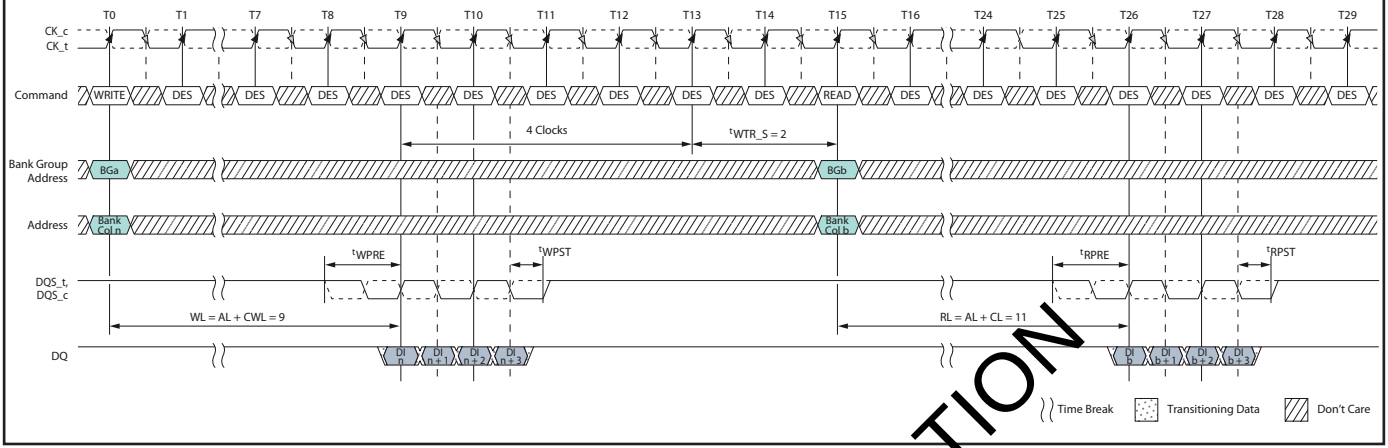
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T15.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

FIGURE 211: WRITE (BL8) TO READ (BL8) WITH 1TCK PREAMBLE IN SAME BANK GROUP



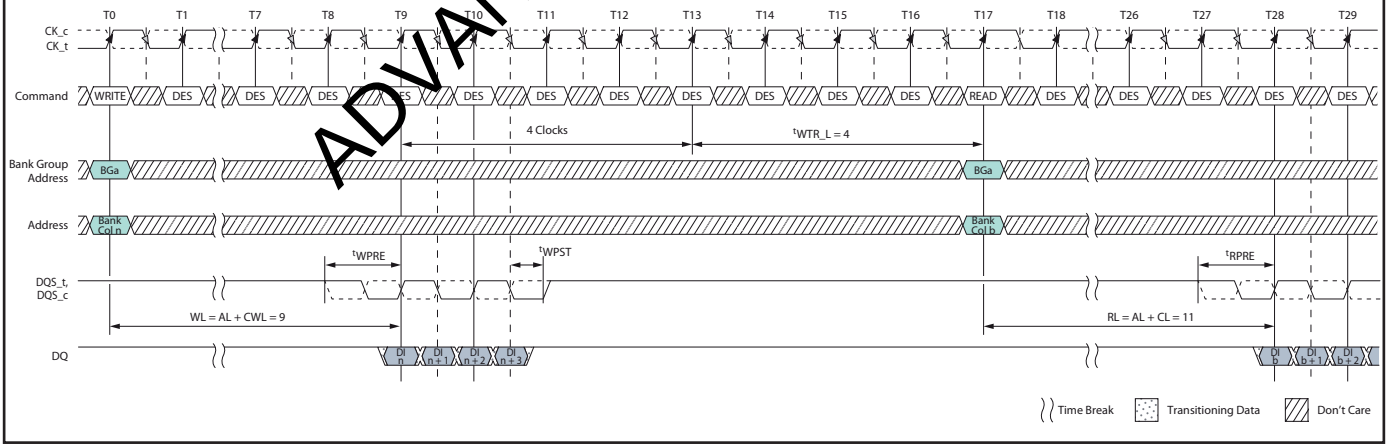
Notes:
1. BL = 8, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_L) is referenced from the first rising clock edge after the last write data shown at T13.

FIGURE 212: WRITE (BC4) OTF TO READ (BC4) OTF WITH 1^TCK PREAMBLE IN DIFFERENT BANK GROUP



Notes:
1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^tCK, WRITE preamble = 1^tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (^tWTR_S) is referenced from the first rising clock edge after the last write data shown at T13.

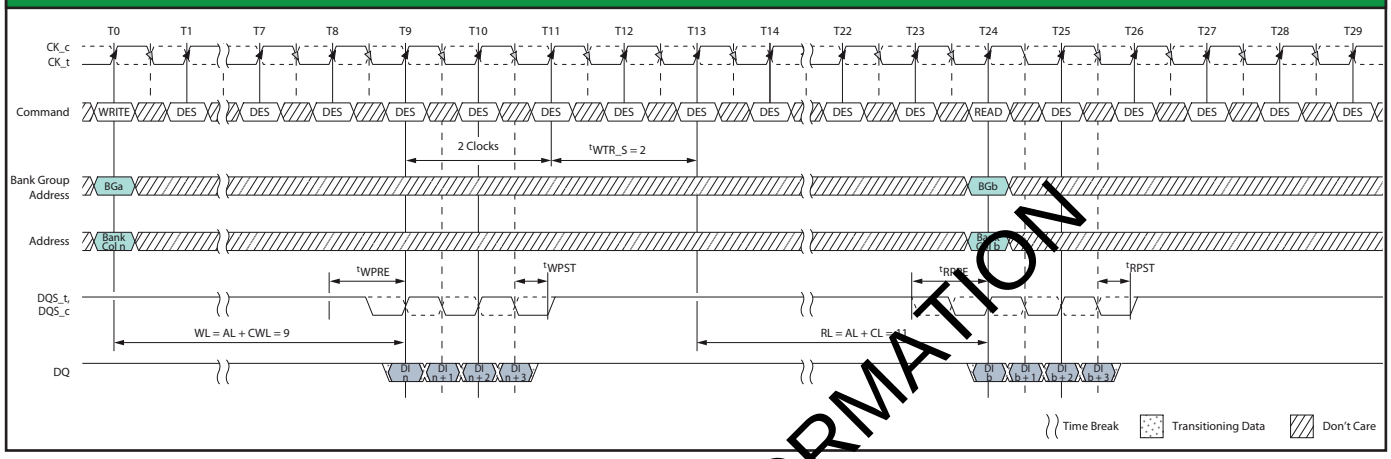
FIGURE 213: WRITE (BC4) OTF TO READ (BC4) OTF WITH 1^TCK PREAMBLE IN SAME BANK GROUP



Notes:
1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1^tCK, WRITE preamble = 1^tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0 and READ command at T17.

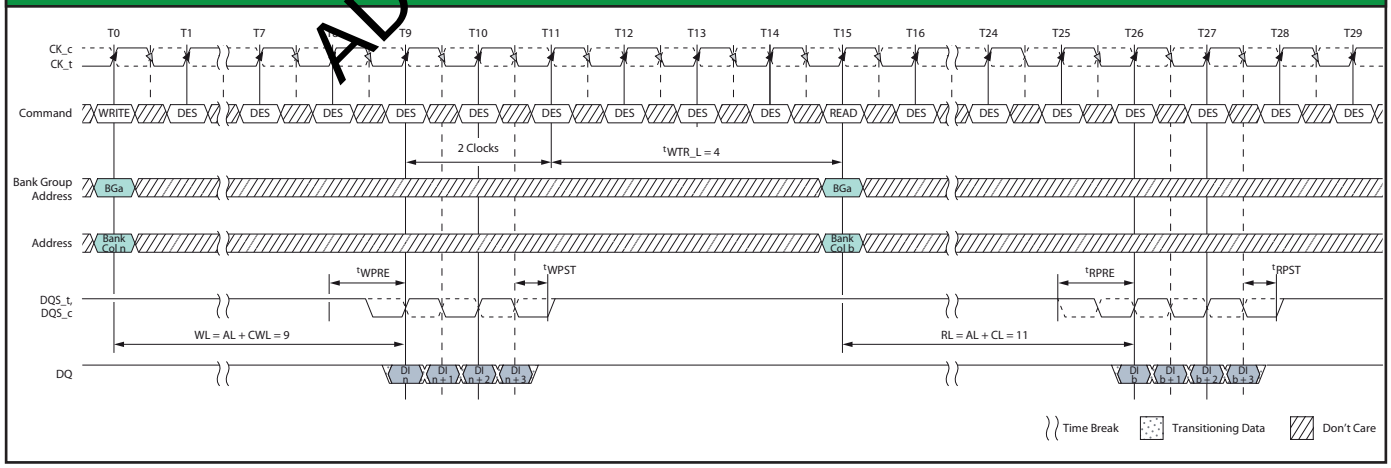
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_L) is referenced from the first rising clock edge after the last write data shown at T13.

Figure 214: WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Different Bank Group



Notes:
1. BC = 4, WL = 9 (CWL = 9, AL = 0), CL = 11, READ preamble = 1 tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (tWTR_S) is referenced from the first rising clock edge after the last write data shown at T11.

Figure 215: WRITE (BC4) Fixed to READ (BC4) Fixed with 1tCK Preamble in Same Bank Group



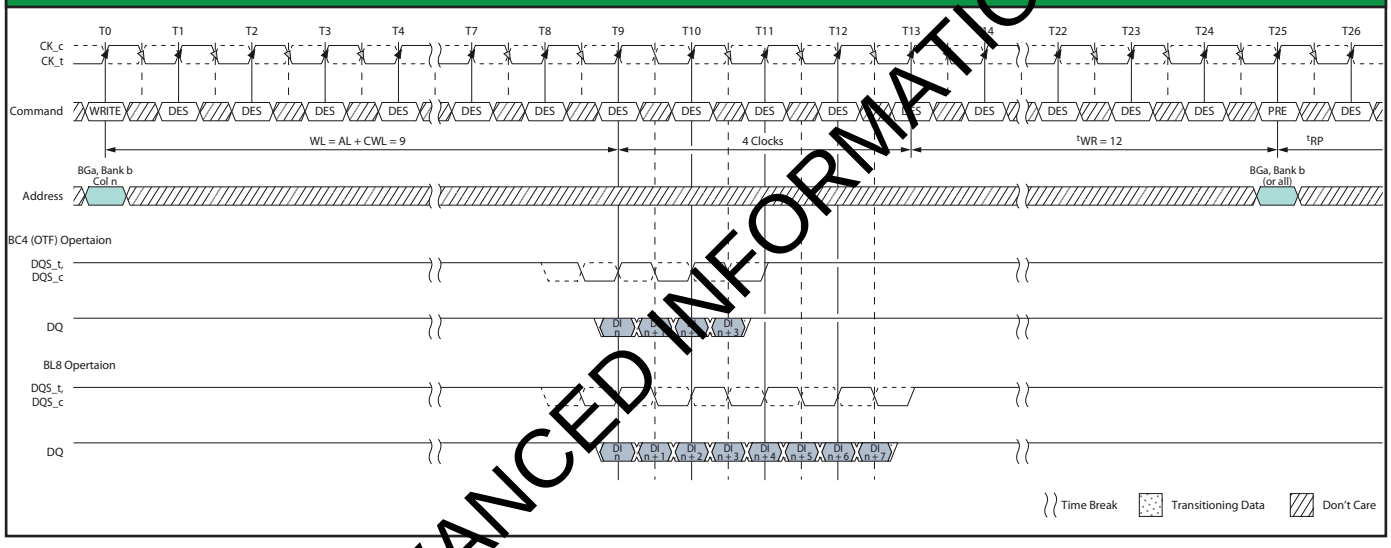
Notes:
1. BC = 4, WL = 9 (CWL = 9, AL = 0), C L = 11, READ preamble = 1tCK, WRITE preamble = 1tCK.
2. DI *b* = data-in from column *b*.

3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.
6. The write timing parameter (^{t}WTR_L) is referenced from the first rising clock edge after the last write data shown at T11.

WRITE Operation Followed by PRECHARGE Operation

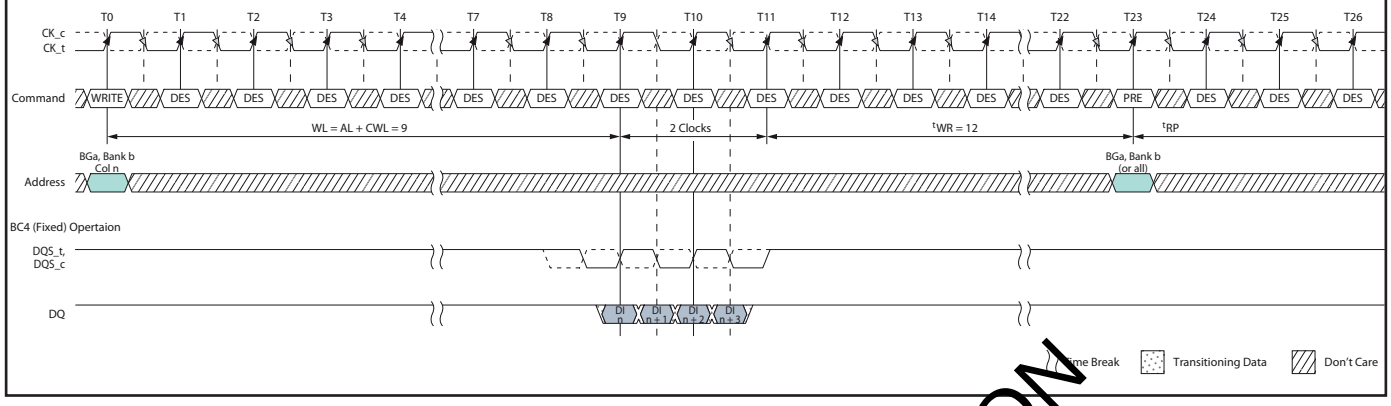
The minimum external WRITE command to PRECHARGE command spacing is equal to WL (AL + CWL) plus either 4^{t}CK (BL8/BC4-OTF) or 2^{t}CK (BC4-fixed) plus ^{t}WR. The minimum ACT to PRE timing, ^{t}RAS, must be satisfied as well.

FIGURE 216: WRITE (BL8/BC4-OTF) TO PRECHARGE WITH 1^{T}CK PREAMBLE



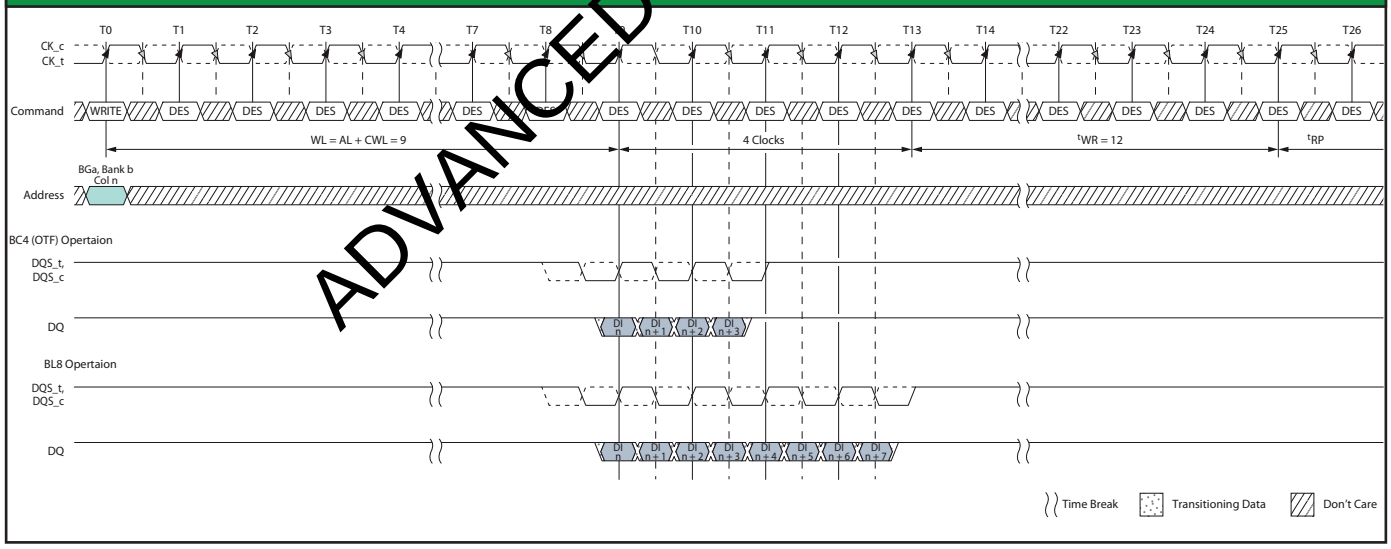
Notes:
1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^{t}CK, ^{t}WR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (^{t}WR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

FIGURE 217: WRITE (BC4-FIXED) TO PRECHARGE WITH 1^TCK PREAMBLE



Notes:
1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^tCK, ^tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (^tWR) is referenced from the first rising clock edge after the last write data shown at T11. ^tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

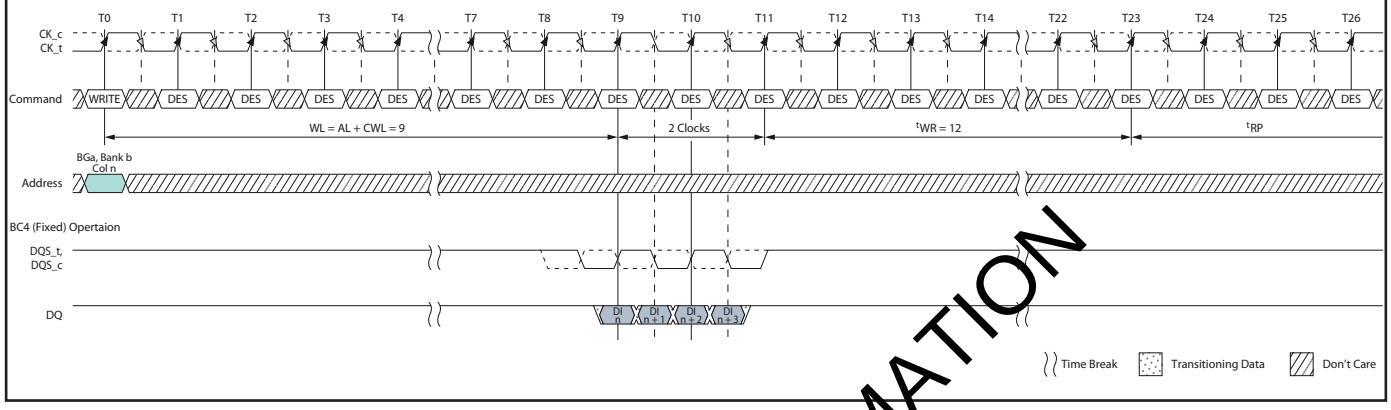
FIGURE 218: WRITE (BL8/BC4-OTF) TO AUTO PRECHARGE WITH 1^TCK PREAMBLE



Notes:
1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^tCK, ^tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, CRC = Disable.

6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

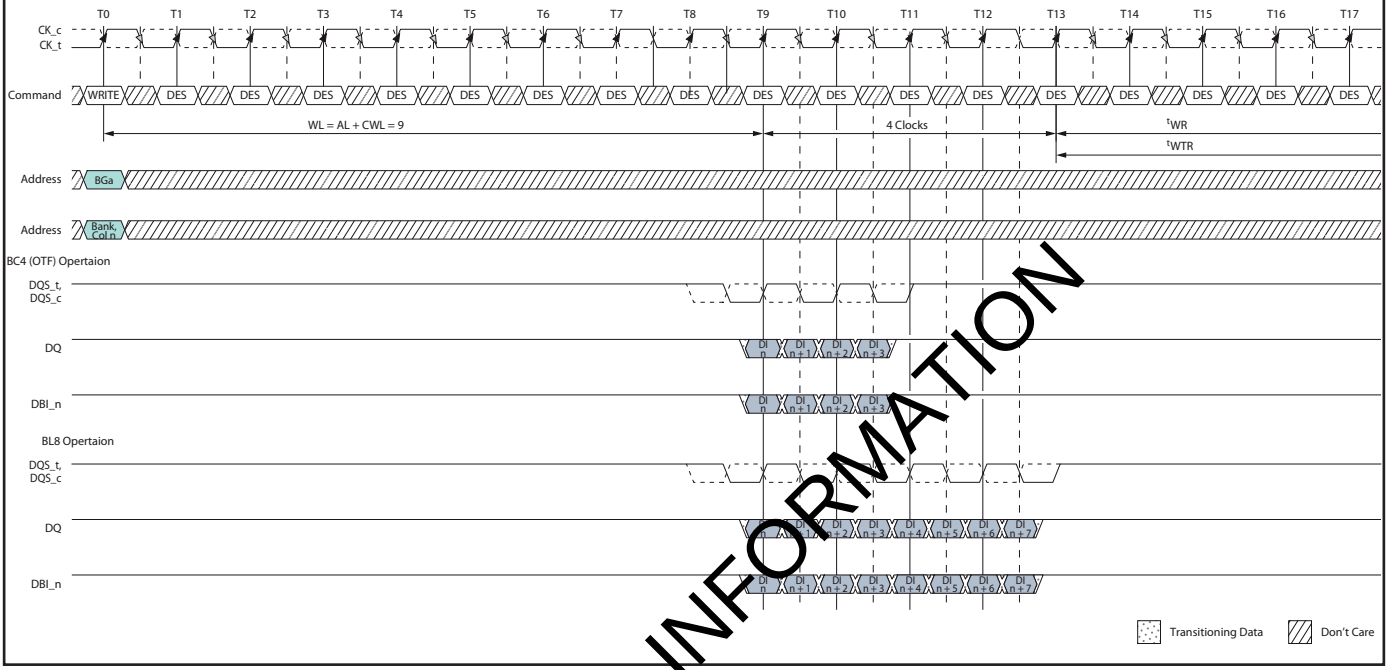
FIGURE 219: WRITE (BC4-FIXED) TO AUTO PRECHARGE WITH 1TCK PREAMBLE



Notes:
1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1tCK, tWR = 12.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, CRC = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11. tWR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.

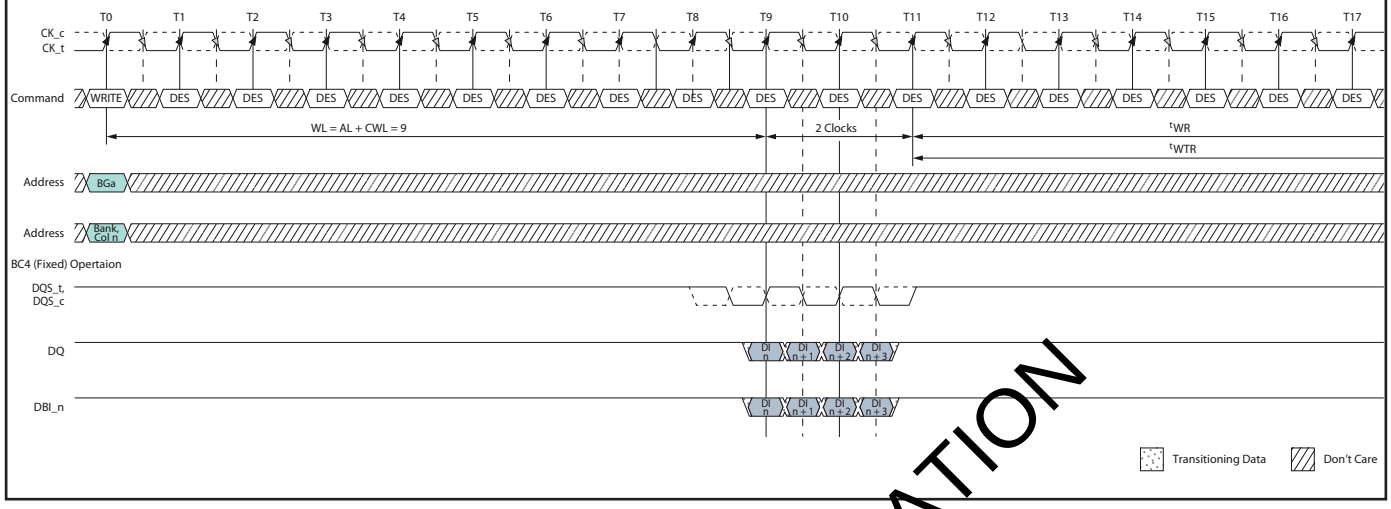
WRITE Operation with WRITE DBI Enabled

FIGURE 220: WRITE (BL8/BC4-OTF) WITH 1^TCK PREAMBLE AND DBI



Notes:
1. BL = 8 with BC4-OTF, WL = 9 (CWL = 9, AL = 0), Preamble = 1^tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE command at T0. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.
6. The write recovery time (^tWR_DBI) is referenced from the first rising clock edge after the last write data shown at T13.

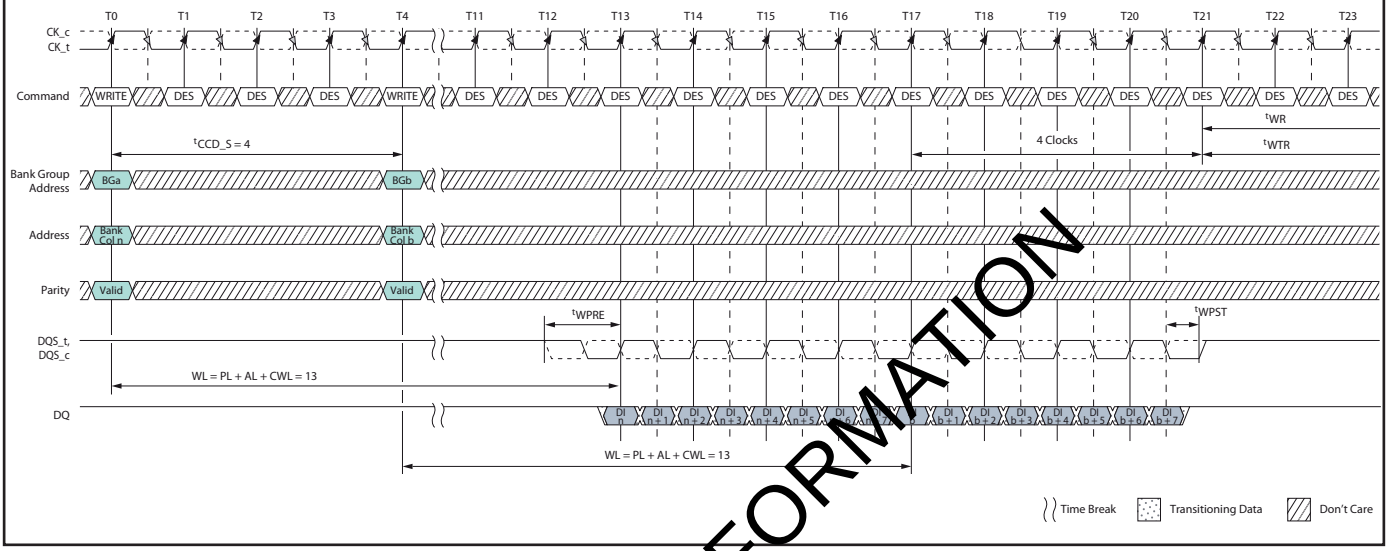
FIGURE 221: WRITE (BC4-FIXED) WITH 1^TCK PREAMBLE AND DBI



Notes:
1. BC4 = fixed, WL = 9 (CWL = 9, AL = 0), Preamble = 1^tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10.
5. CA parity = Disable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disabled.

WRITE Operation with CA Parity Enabled

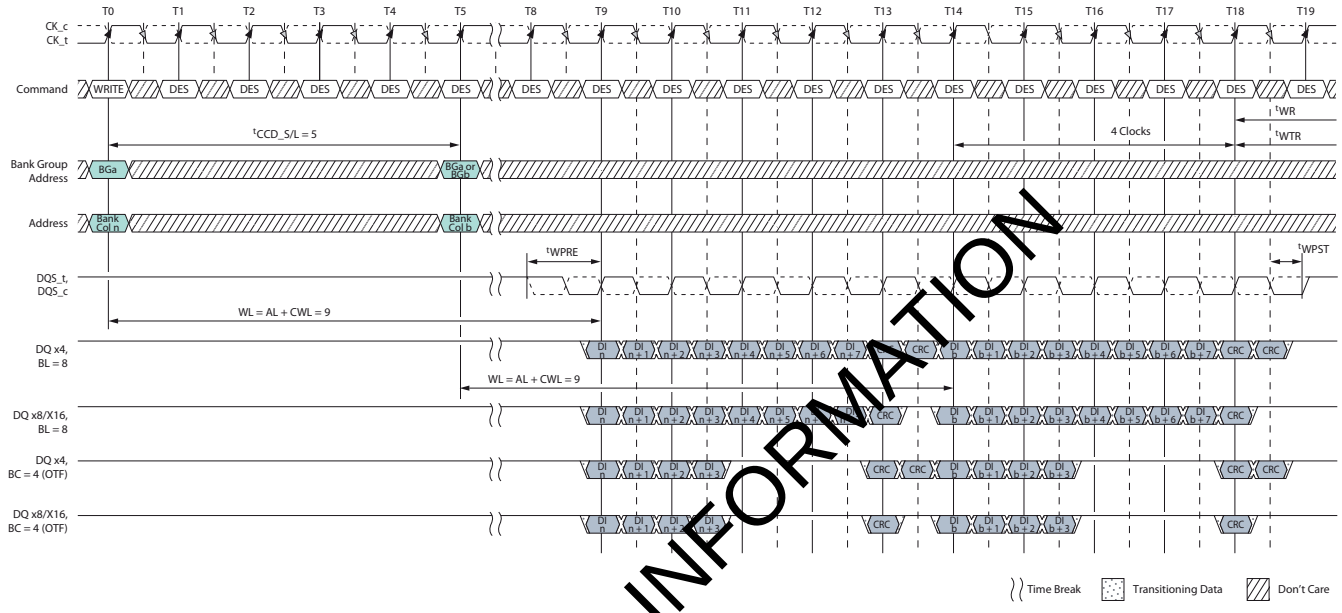
FIGURE 222: CONSECUTIVE WRITE (BL8) WITH 1TCK PREAMBLE AND CA PARITY IN DIFFERENT BANK GROUP



Notes:
1. BL = 8, WL = 9 (CWL = 13, AL = 0), Preamble = 1tCK.
2. DI *n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T4.
5. CA parity = Enable, CS to CA latency = Disable, Write DBI = Enabled, Write CRC = Disable.
6. 6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

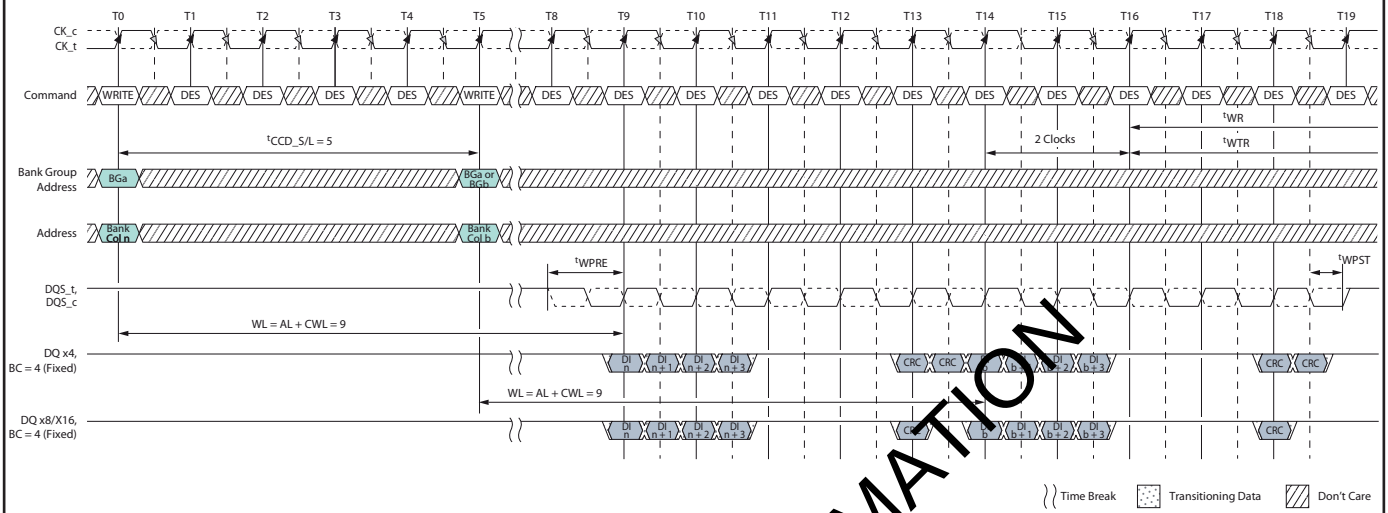
WRITE Operation with Write CRC Enabled

Figure 223: Consecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



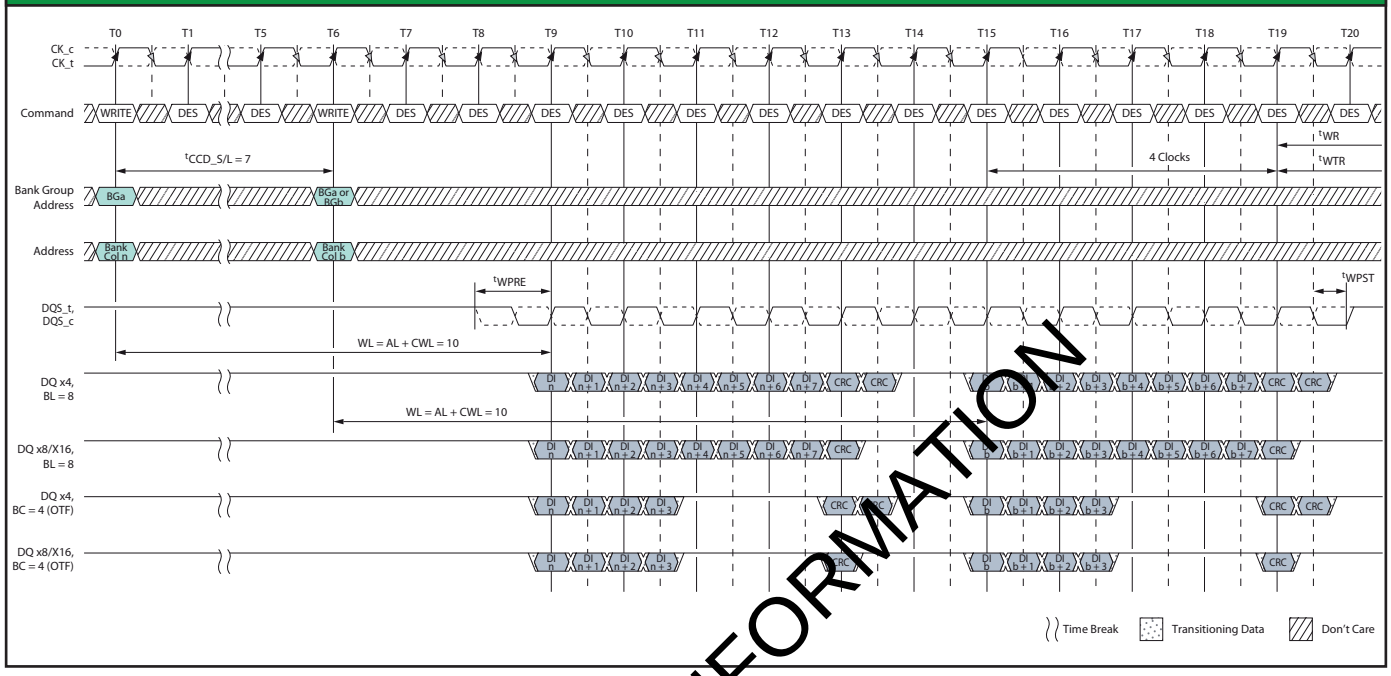
Notes:
1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1tCK, tCDD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T5.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T5.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Figure 224: Consecutive WRITE (BC4-Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



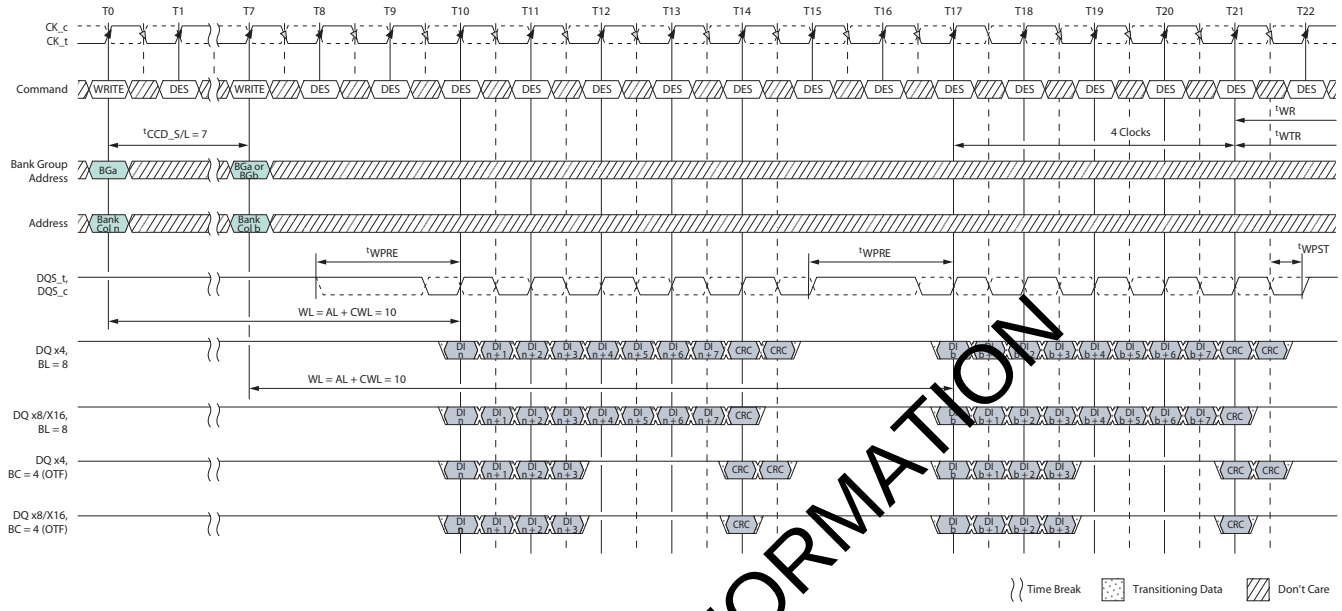
Notes:
1. BC4-fixed, AL = 0, CWL = 9, Preamble = 1tCK, tCDD_S/L = 5tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[1:0] = 10 during WRITE commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Figure 225: Nonconsecutive WRITE (BL8/BC4-OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



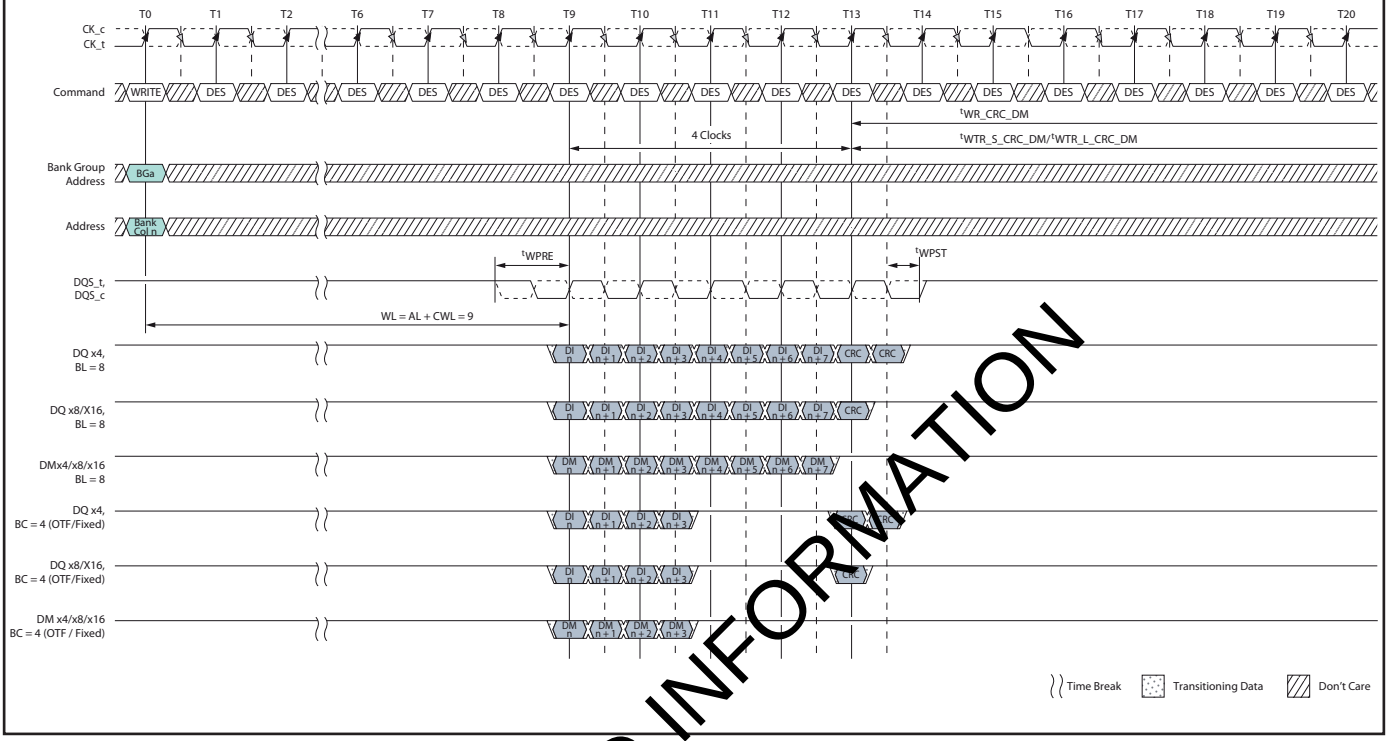
Notes:
1. BL8/BC4-OTF, AL = 0, CWL = 9, Preamble = 1tCK, tCDD_S/L = 6tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T6.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T6.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

Figure 226: Nonconsecutive WRITE (BL8/BC4-OTF) with 2tCK Preamble and Write CRC in Same or Different Bank Group



Notes:
1. BL8/BC4-OTF, AL = 0, CWL = 9, 11 = 10 (see Note 9), Preamble = 2tCK, tCDD_S/L = 7tCK (see Note 7).
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE commands at T0 and T7.
5. BC4 setting activated by MR0[1:0] = 01 and A12 = 0 during WRITE commands at T0 and T7.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Disable.
7. tCDD_S/L = 6tCK is not allowed in 2tCK preamble mode.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK WRITE preamble mode, CWL may need to be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK WRITE preamble mode.

Figure 227: WRITE (BL8/BC4-OTF/Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



Notes:
1. BL8/BC4, AL = 0, CWL = 9, Preamble = 1tCK.
2. DI *n* (or *b*) = data-in from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during WRITE command at T0.
6. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_DM) and write timing parameter (tWTR_S_CRC_DM/tWTR_L_CRC_DM) are referenced from the first rising clock edge after the last write data shown at T13.

Write Timing Violations

Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the device works properly. However, for certain minor violations, it is desirable that the device is guaranteed not to “hang up” and that errors are limited to that specific operation. A minor violation does not include a major timing violation (for example, when a DQS strobe misses in the ^{t}DQSCK window).

For the following, it will be assumed that there are no timing violations with regard to the WRITE command itself (including ODT, and so on) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Violations

If the data-to-strobe timing requirements (^{t}DS, ^{t}DH) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example, the relevant strobe edges for WRITE Burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, and T8.5.

Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise.

Strobe-to-Strobe and Strobe-to-Clock Violations

If the strobe timing requirements (^{t}DQSH, tDQSL, ^{t}WPRE, ^{t}WPST) or the strobe to clock timing requirements (^{t}DSS, ^{t}DSH, ^{t}DQSS) are violated, for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise with the following constraints:

- Both write CRC and data burst OTF are disabled; timing specifications other than ^{t}DQSH, ^{t}DQSL, ^{t}WPRE, ^{t}WPST, ^{t}DSS, ^{t}DSH, ^{t}DQSS are not violated.
- The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the WRITE latency position.
- A READ command following an offending WRITE command from any open bank is allowed.
- One or more subsequent WR or a subsequent WRA (to same bank as offending WR) may be issued ^{t}CCD_L later, but incorrect data could be written. Subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
- One or more subsequent WR or a subsequent WRA (to a different bank group) may be issued ^{t}CCD_S later, but incorrect data could be written. Subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
- After one or more precharge commands (PRE or PREA) are issued to the device after an offending WRITE command and all banks are in precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank will be able to write correct data.

ZQ CALIBRATION Commands

A ZQ CALIBRATION command is used to calibrate DRAM RON and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization and a relatively smaller time to perform periodic calibrations.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, after calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM I/O, which is reflected as an updated output driver and ODT values.

The first ZQCL command issued after reset is allowed a timing period of ^{t}ZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after reset are allowed a timing period of ^{t}ZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter ^{t}ZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ correction) of RON and R_{TT} impedance error within 64 *n*CK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other appli-cation-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature ($T_{driftrate}$) and voltage ($V_{driftrate}$) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQ_{correction}}{R(T_{sens} \times T_{driftrate}) + (V_{sens} \times V_{driftrate})}$$

Where T_{sens} = MAX($dR_{TT}dT$, $dR_{ON}dTM$) and V_{sens} = MAX($dR_{TT}dV$, $dR_{ON}dVM$) define the temperature and voltage sensitivities.

For example, if T_{sens} = 1.5%/°C, V_{sens} = 0.15%/mV, $T_{driftrate}$ = 1 °C/sec and $V_{driftrate}$ = 15 mV /sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

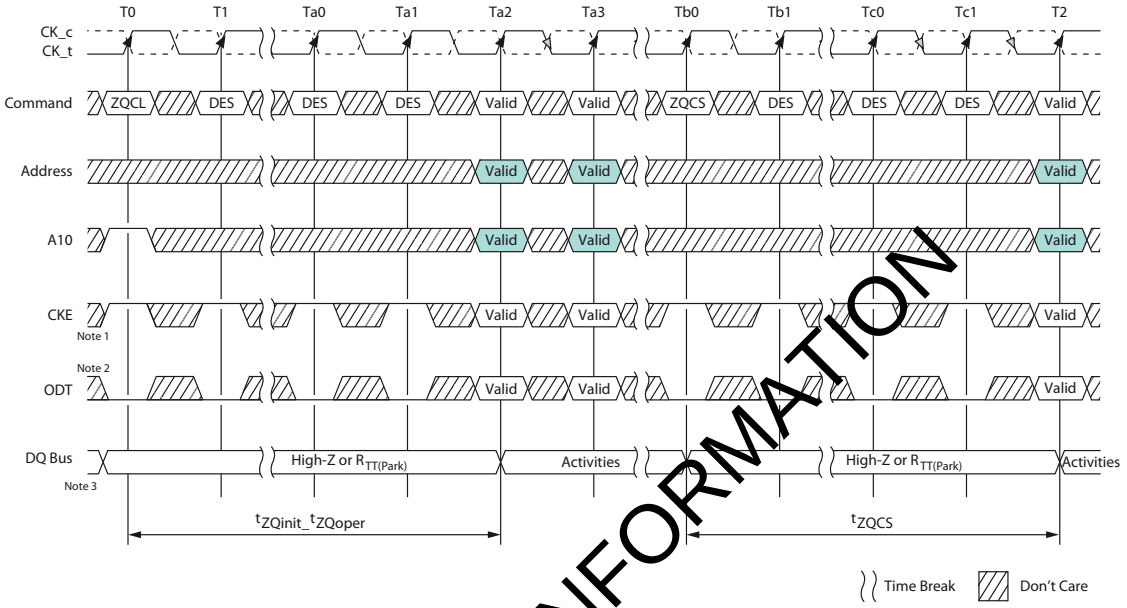
No other activities should be performed on the DRAM channel by the controller for the duration of ^{t}ZQinit, ^{t}ZQoper, or ^{t}ZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. After DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and ^{t}RP met before ZQCL or ZQCS commands are issued by the controller.

ZQ CALIBRATION commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an I/O calibration without an explicit ZQ CALIBRATION command. The earliest possible time for a ZQ CALIBRATION command (short or long) after self refresh exit is ^{t}XSF.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of ^{t}ZQoper, ^{t}ZQinit, or ^{t}ZQCS between the devices.

FIGURE 228: ZQ CALIBRATION TIMING



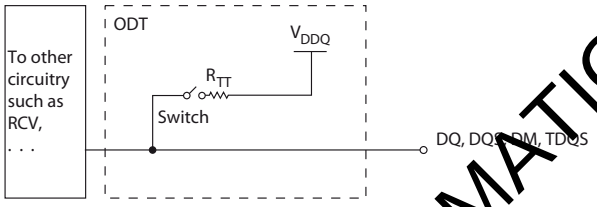
Notes:
1. CKE must be continuously registered HIGH during the calibration procedure.
2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure or the DRAM will automatically disable $R_{TT}1$.
3. All devices connected to the DQ bus should be High-Z during the calibration procedure.

On-Die Termination

On-die termination (ODT) is a feature that enables the device to change termination resistance for each DQ, DQS, and DM_n signal when enabled via A11 = 1 in MR1) via the ODT control pin, WRITE command, or default parking value with MR setting. ODT is applied to each DQU, DQL, DQSU, DQSL, DMU_n, and DML_n signal. The ODT feature is designed to improve the signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further along in this document.

The ODT feature is turned off and not supported in self refresh mode.

FIGURE 229: FUNCTIONAL REPRESENTATION OF ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of R_{TT} is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable $R_{TT(NOM)}$ [MR1[9,6,2] = 0,0,0] and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT mode of the DDR4 device has four states: data termination disable, $R_{TT(NOM)}$, $R_{TT(WR)}$, and $R_{TT(Park)}$. The ODT mode is enabled if any of MR1[10:8] ($R_{TT(NOM)}$), MR2[11:9] ($R_{TT(WR)}$), or MR5[8:6] ($R_{TT(Park)}$) are non-zero. When enabled, the value of R_{TT} is determined by the settings of these bits.

R_{TT} control of each R_{TT} condition is possible with a WR or RD command and ODT pin.

- $R_{TT(WR)}$: The DRAM (rank) that is being written to provide termination regardless of ODT pin status (either HIGH or LOW).
- $R_{TT(NOM)}$: DRAM turns on $R_{TT(NOM)}$ if it sees ODT asserted HIGH (except when ODT is disabled by MR1).
- $R_{TT(Park)}$: Default parked value set via MR5 to be enabled and $R_{TT(NOM)}$ is not turned on.
- The Termination State Table that follows shows various interactions.

The RTT values have the following priority:

- Data termination disable
- $R_{TT(WR)}$
- $R_{TT(NOM)}$
- $R_{TT(Park)}$

ODT Mode Register and ODT State Table

Table 131: Termination State Table

Case	$R_{TT(Park)}$	$R_{TT(NOM)}$ 1	$R_{TT(WR)}$ 2	ODT Pin	ODT READS [3]	ODT Standby	ODT WRITES
A[4]	Disabled	Disabled	Disabled	Don't Care	Off (High-Z)	Off (High-Z)	Off (High-Z)
			Enabled	Don't Care	Off (High-Z)	Off (High-Z)	$R_{TT(WR)}$
B[5]	Enabled	Disabled	Disabled	Don't Care	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(Park)}$
			Enabled	Don't Care	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(WR)}$
C[6]	Disabled	Enabled	Disabled	Low	Off (High-Z)	Off (High-Z)	Off (High-Z)
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(NOM)}$
			Enabled	Low	Off (High-Z)	Off (High-Z)	$R_{TT(WR)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(WR)}$
D[6]	Enabled	Enabled	Disabled	Low	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(Park)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(NOM)}$
			Enabled	Low	Off (High-Z)	$R_{TT(Park)}$	$R_{TT(WR)}$
				High	Off (High-Z)	$R_{TT(NOM)}$	$R_{TT(WR)}$

Notes:
1. If $R_{TT(NOM)}$ MR is disabled, power to the ODT receiver will be turned off to save power.
2. If $R_{TT(WR)}$ is enabled, $R_{TT(WR)}$ will be activated by a WRITE command for a defined period time independent of the ODT pin and MR setting of RTT(Park)/$R_{TT(NOM)}$. This is described in the Dynamic ODT section.
3. When a READ command is executed, the DRAM termination state will be High-Z for a defined period independent of the ODT pin and MR setting of $R_{TT(Park)}$/$R_{TT(NOM)}$. This is described in the ODT During Read section.
4. Case A is generally best for single-rank memories.
5. Case B is generally best for dual-rank, single-slotted memories.
6. Case C and Case D are generally best for multi-slotted memories.

ODT Read Disable State Table

Upon receiving a READ command, the DRAM driving data disables ODT after RL - (2 or 3) clock cycles, where 2 = 1^{t}CK preamble mode and 3 = 2^{t}CK preamble mode. ODT stays off for a duration of BL/2 + (2 or 3) + (0 or 1) clock cycles, where 2 = 1^{t}CK preamble mode, 3 = 2^{t}CK preamble mode, 0 = CRC disabled, and 1 = CRC enabled.

Table 132: Read Termination Disable Window

Preamble	CRC	Start ODT Disable After Read	Duration of ODT Disable
1^{t}CK	Disabled	RL - 2	BL/2 + 2
	Enabled	RL - 2	BL/2 + 3
2^{t}CK	Disabled	RL - 3	BL/2 + 3
	Enabled	RL - 3	BL/2 + 4

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes include the following:

- Any bank active with CKE HIGH
- Refresh with CKE HIGH
- Idle mode with CKE HIGH
- Active power-down mode (regardless of MR1 bit A10)
- Precharge power-down mode

In synchronous ODT mode, $R_{TT(NOM)}$ will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is determined by the programmed values for: CAS WRITE latency (CWL), additive latency (AL), and parity latency (PL), as well as the programmed state of the preamble.

ODT Latency and Posted ODT

The ODT latencies for synchronous ODT mode are summarized in the table below. For details, refer to the latency definitions.

Table 133: ODT Latency at DDR4-1600/-1866/-2133/-2400/-2666/-3200

Note 1 applies to the entire table

Symbol	Parameter	1tCK Preamble	2tCK Preamble	Unit
DODTLon	Direct ODT turn-on latency	CWL + AL + PL - 2	CWL + AL + PL - 3	tCK
DODTLoff	Direct ODT turn-off latency	CWL + AL + PL - 2	CWL + AL + PL - 3	
RODTLoff	READ command to internal ODT turn-off latency	CL + AL + PL - 2	CL + AL + PL - 3	
RODTLon4	READ command to $R_{TT(Park)}$ turn-on latency in BC4-fixed	RODTLoff + 4	RODTLoff + 5	
RODTLon8	READ command to $R_{TT(Park)}$ turn-on latency in BL8/BC4OTF	RODTLoff + 6	RODTLoff + 7	
ODTH4	ODT Assertion time, BC4 mode	4	5	
ODTH8	ODT Assertion time, BL8 mode	6	7	

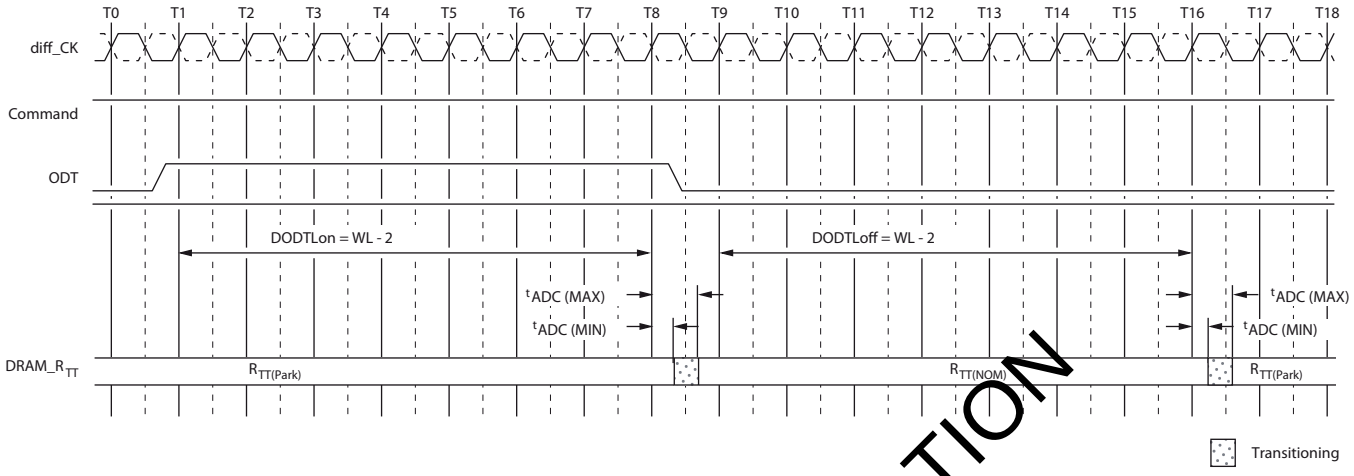
Timing Parameters

In synchronous ODT mode, the following parameters apply:

- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, and tADC (MIN)/(MAX).
- tADC (MIN) and tADC (MAX) are minimum and maximum RTT change timing skew between different termination values. These timing parameters apply to both the synchronous ODT mode and the data termination disable mode.

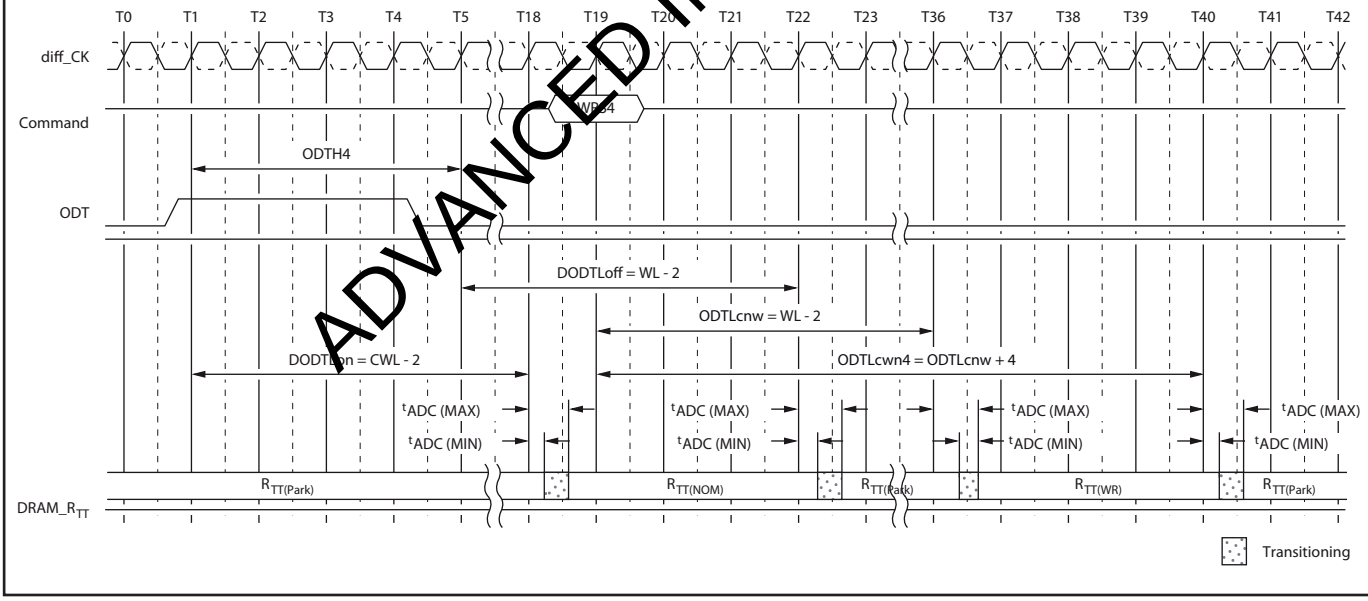
When ODT is asserted, it must remain HIGH until minimum ODTH4 (BC = 4) or ODTH8 (BL = 8) is satisfied. If write CRC mode or 2tCK preamble mode is enabled, ODTH should be adjusted to account for it. ODTHx is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of a WRITE command.

Figure 230: Synchronous ODT Timing with BL8



Notes:
1. Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL + CWL - 2 = 7; DODTLoff = AL + PL + CWL - 2 = 7.
2. ODT must be held HIGH for at least ODTH8 after assertion (T1).

Figure 231: Synchronous ODT with BC4



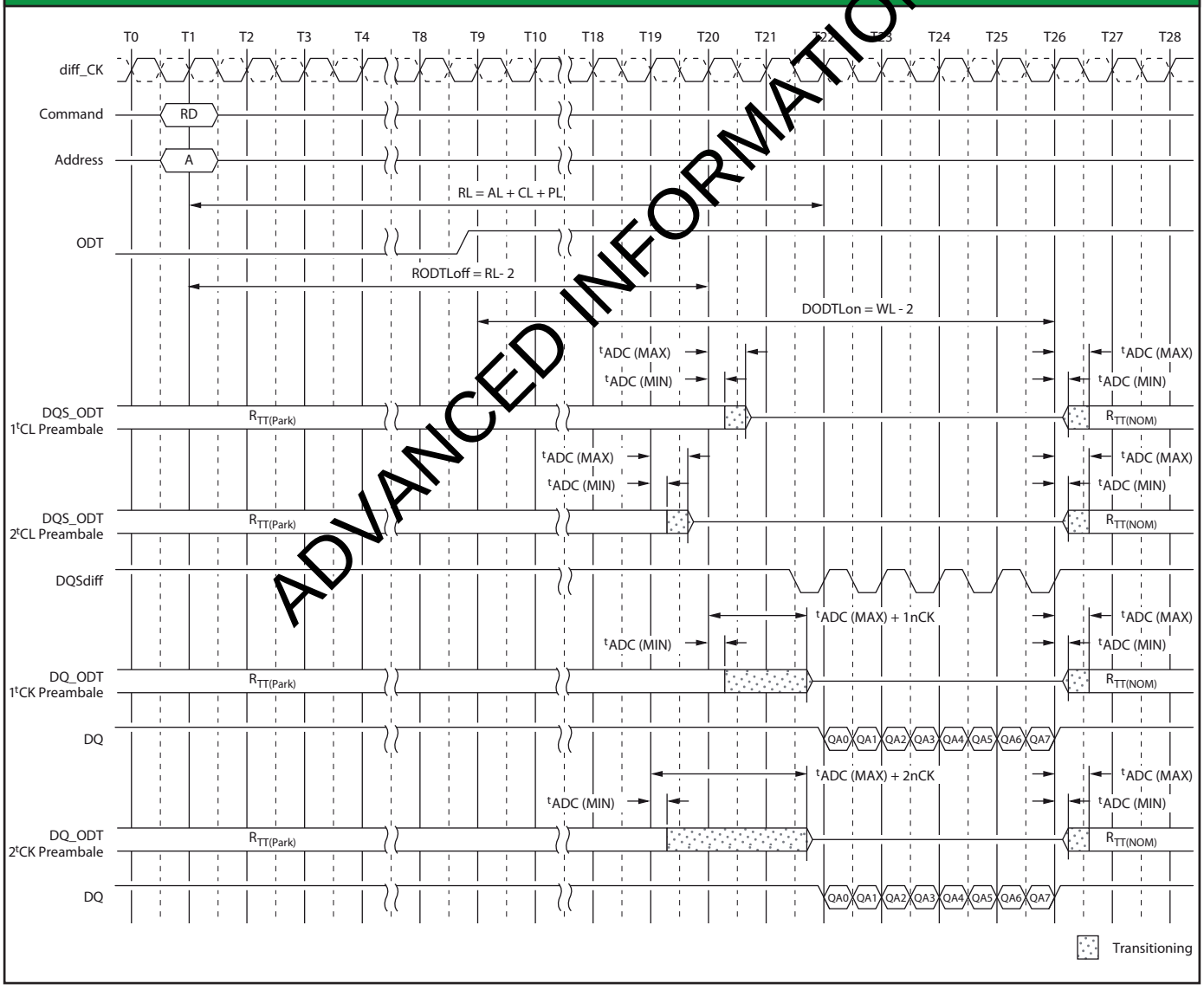
Notes:
1. Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL+ CWL - 2 = 17; ODTcnw = AL + PL+ CWL - 2 = 17.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).

ODT During Reads

Because the DRAM cannot terminate with R_{TT} and drive with R_{ON} at the same time, R_{TT} may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25 the device turns on the termination when it stops driving, which is determined by ^{t}HZ. If the DRAM stops driving early (that is, ^{t}HZ is early), then ^{t}ADC (MIN) timing may apply. If the DRAM stops driving late (that is, ^{t}HZ is late), then the DRAM complies with ^{t}ADC (MAX) timing.

Using CL = 11 as an example for the figure below: PL = 0, AL = CL - 1 = 10, RL = PL + AL + CL = 21, CWL= 9; RODTLoff = RL - 2 = 19, DODTLon = PL + AL + CWL - 2 = 17, 1tCK preamble.

Figure 232: ODT During Reads



In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the device can be changed without issuing an MRS command. This requirement is supported by the dynamic ODT feature.

Functional Description

Dynamic ODT mode is enabled if bit A9 or A10 of MR2 is set to 1.

- Three R_{TT} values are available: $R_{TT(NOM)}$, $R_{TT(WR)}$, and $R_{TT(Park)}$.
  - The value for $R_{TT(NOM)}$ is preselected via bits MR1[10:8].
  - The value for $R_{TT(WR)}$ is preselected via bits MR2[11:9].
  - The value for $R_{TT(Park)}$ is preselected via bits MR5[8:6].
- During operation without WRITE commands, the termination is controlled as fol-lows:
  - Nominal termination strength $R_{TT(NOM)}$ or $R_{TT(Park)}$ is selected.
  - $R_{TT(NOM)}$ on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff, and $R_{TT(Park)}$ is on when ODT is LOW.
- When a WRITE command (WR, WRA, WRS4, WRS8, WRAS4, and WRAS8) is registered, and if dynamic ODT is enabled, the termination is controlled as follows:
  - Latency ODTLcnw after the WRITE command, termination strength $R_{TT(WR)}$ is selected.
  - Latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the WRITE command, termination strength $R_{TT(WR)}$ is de-selected.

One or two clocks will be added into or subtracted from ODTLcwn8 and ODTLcwn4, depending on write CRC mode and/or 2tCK preamble enablement.

The following table shows latencies and timing parameters relevant to the on-die termination control in dynamic ODT mode. The dynamic ODT feature is not supported in DLL-off mode. An MRS command must be used to set $R_{TT(WR)}$ to disable dynamic ODT externally (MR2[11:9] = 000).

TABLE 134: DYNAMIC ODT LATENCIES AND TIMING (1TCK PREAMBLE MODE AND CRC DISABLED)

Name and Description	Abbr.	Defined from	Defined to	Definition for All DDR4 Speed Bins	Unit
ODT latency for change from $R_{TT(Park)}$ /$R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcnw	Registering external WRITE command	Change R_{TT} strength from $R_{TT(Park)}$ /RTT(NOM) to $R_{TT(WR)}$	ODTLcnw = WL - 2	tCK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$ /$R_{TT(NOM)}$ (BC = 4)	ODTLcwn 4	Registering external WRITE command	Change R_{TT} strength from $R_{TT(WR)}$ to $R_{TT(Park)}$ /$R_{TT(NOM)}$	ODTLcwn4 = 4 + ODTLcnw	tCK
ODT latency for change from $R_{TT(WR)}$ to $R_{TT(Park)}$ /$R_{TT(NOM)}$ (BL = 8)	ODTLcwn 8	Registering external WRITE command	Change R_{TT} strength from $R_{TT(NOM)}$ to $R_{TT(WR)}$	ODTLcwn8 = 6 + ODTLcnw	tCK (AVG)
R_{TT} change skew	tADC	ODTLcnw ODTLcwn	R_{TT} valid	tADC (MIN) = 0.3 tADC (MAX) = 0.7	tCK (AVG)

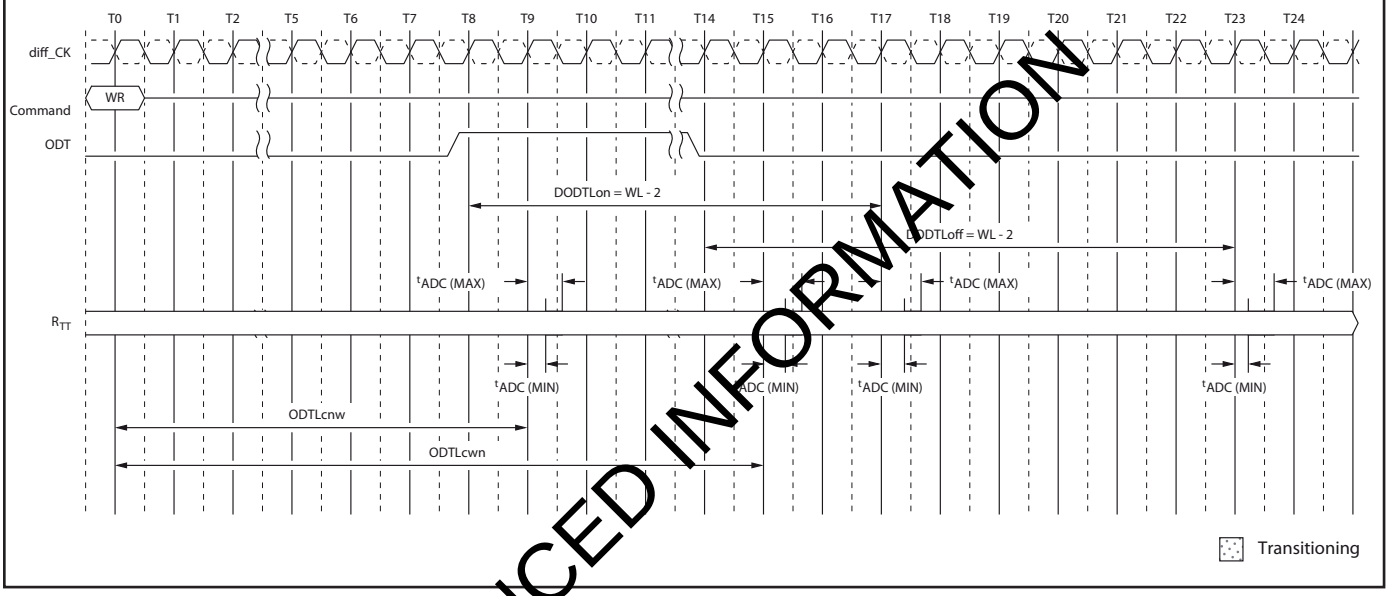
Dynamic ODT

TABLE 135: DYNAMIC ODT LATENCIES AND TIMING WITH PREAMBLE MODE AND CRC MODE MATRIX

Symbol	1tCK Parameter		2tCK Parameter		Unit
	CRC Off	CRC On	CRC Off	CRC On	
ODTLcnw[1]	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw + 4	ODTLcnw + 7	ODTLcnw + 5	ODTLcnw + 8	
ODTLcwn8	ODTLcnw + 6	ODTLcnw + 7	ODTLcnw + 7	ODTLcnw + 8	

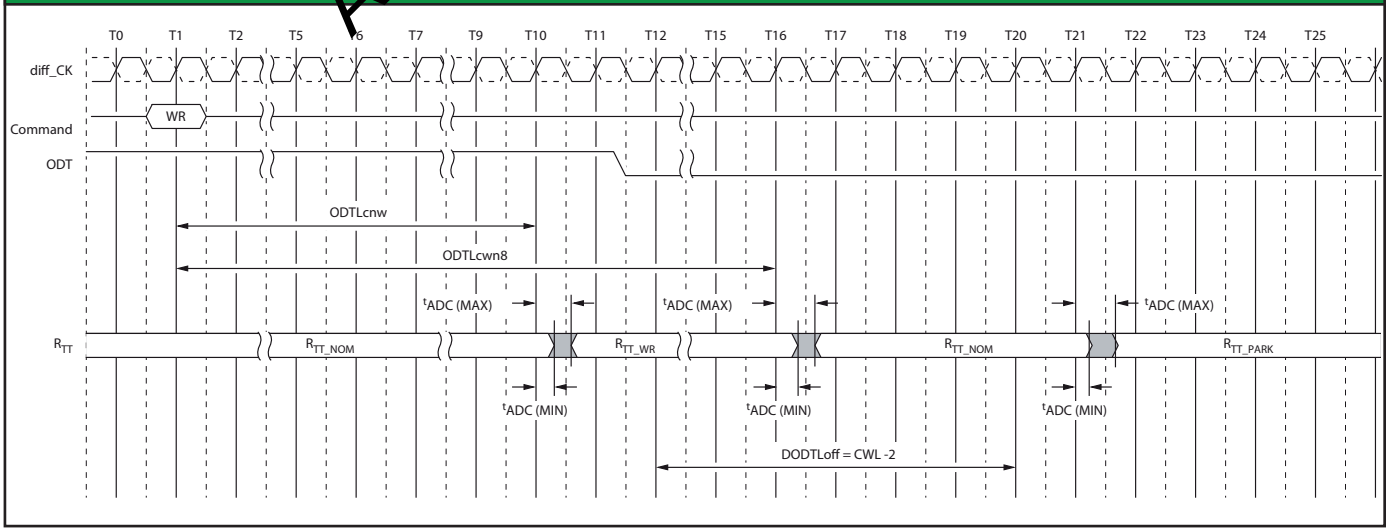
Note: 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).

FIGURE 233: DYNAMIC ODT (1T CK PREAMBLE; CL = 14, CWL = 11, BL = 8, AL = 0, CRC DISABLED)



Notes: 1. ODTLcnw = WL - 2 (1tCK preamble) or WL - 3 (2tCK preamble).
2. If BC4, then ODTLcwn = WL + 4 if CRC disabled or WL + 5 if CRC enabled; If BL8, then ODTLcwn = WL + 6 if CRC disabled or WL + 7 if CRC enabled.

FIGURE 234: DYNAMIC ODT OVERLAPPED WITH $R_{TT(NOM)}$ (CL = 14, CWL = 11, BL = 8, AL = 0, CRC DISABLED)



Note: 1. Behavior with WR command issued while ODT is registered HIGH.

Asynchronous ODT Mode

Asynchronous ODT mode is selected when the DRAM runs in DLL-off mode. In asynchronous ODT timing mode, the internal ODT command is *not* delayed by either additive latency (AL) or the parity latency (PL) relative to the external ODT signal ($R_{TT(NOM)}$). In asynchronous ODT mode, two timing parameters apply: tAONAS (MIN/MAX), and tAOFAS (MIN/MAX).

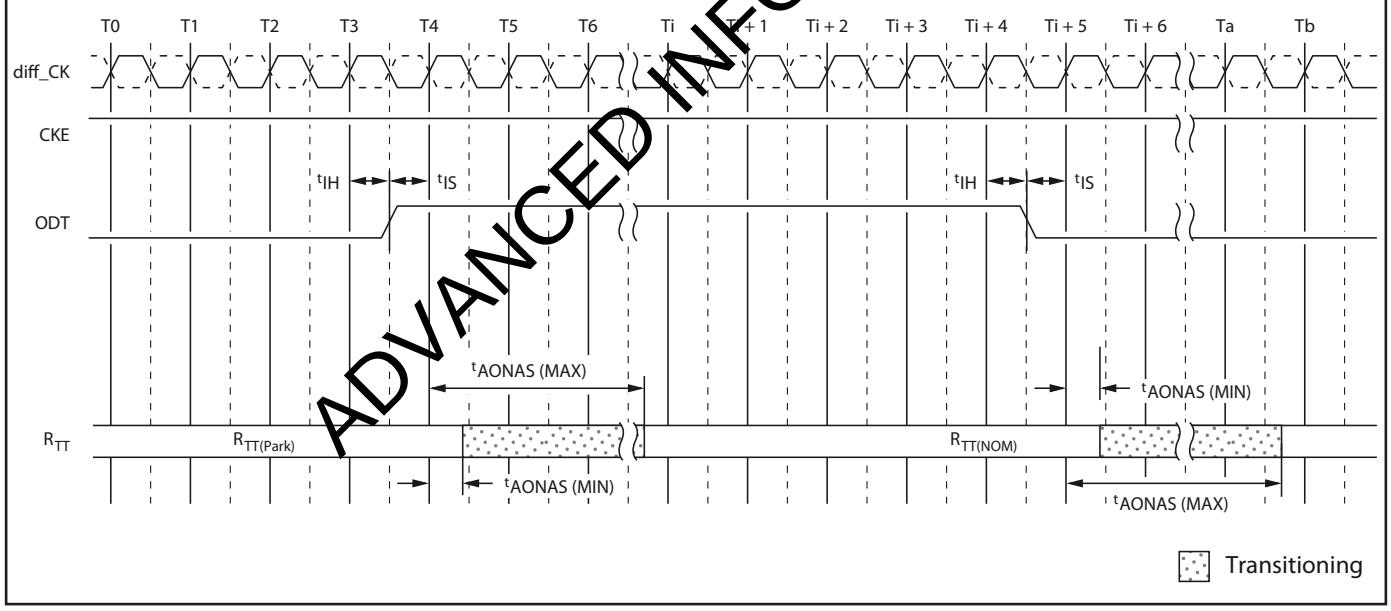
$R_{TT(NOM)}$ Turn-on Time

- Minimum $R_{TT(NOM)}$ turn-on time (^{t}AONAS [MIN]) is when the device termination circuit leaves $R_{TT(Park)}$ and ODT resistance begins to turn on.
- Maximum $R_{TT(NOM)}$ turn-on time (^{t}AONAS [MAX]) is when the ODT resistance has reached $R_{TT(NOM)}$.
- ^{t}AONAS (MIN) and ^{t}AONAS (MAX) are measured from ODT being sampled HIGH.

$R_{TT(NOM)}$ Turn-off Time

- Minimum RTT(NOM) turn-off time (^{t}AOFAS [MIN]) is when the device's termination circuit starts to leave $R_{TT(NOM)}$.
- Maximum $R_{TT(NOM)}$ turn-off time (^{t}AOFAS [MAX]) is when the on-die termination has reached $R_{TT(Park)}$.
- ^{t}AOFAS (MIN) and ^{t}AOFAS (MAX) are measured from ODT being sampled LOW.

FIGURE 235: ASYNCHRONOUS ODT TIMINGS WITH DLL OFF



Options Tables

Table 136: Speed Options

Function	Acronym	Data Rate					
		1600	1866	2133	2400	2666	3200
Write leveling	WL	Yes	Yes	Yes	Yes	TBD	TBD
Temperature controlled refresh	TCR	Yes	Yes	Yes	Yes	TBDs	TBD
Low-power auto self refresh	LPASR	Yes	Yes	Yes	Yes	TBD	TBD
Fine granularity refresh	FGR	Yes	Yes	Yes	Yes	TBD	TBD
Multipurpose register	MR	Yes	Yes	Yes	Yes	TBD	TBD
Data mask	DM	Yes	Yes	Yes	Yes	TBD	TBD
Data bus inversion	DBI	Yes	Yes	Yes	Yes	TBD	TBD
TDQS	–	Yes	Yes	Yes	Yes	TBD	TBD
ZQ calibration	ZQ CAL	Yes	Yes	Yes	Yes	TBD	TBD
V_{REFDQ} calibration	–	Yes	Yes	Yes	Yes	TBD	TBD
Per-DRAM addressability	Per DRAM	Yes	Yes	Yes	Yes	TBD	TBD
Mode regsiter readout	–	Yes	Yes	Yes	Yes	TBD	TBD
Command/Address latency	CAL	Yes	Yes	Yes	Yes	TBD	TBD
Write CRC	CRC	Yes	Yes	Yes	Yes	TBD	TBD
CA parity	–	Yes	Yes	Yes	Yes	TBD	TBD
Gear-down mode	–	No	No	No	No	TBD	TBD
Programmable preamble	–	No	No	No	Yes	TBD	TBD
Maximum power-down mode	–	Yes	Yes	Yes	Yes	TBD	TBD
Connectivity test mode	CT	Yes	Yes	Yes	Yes	TBD	TBD
Additive latency	AL	Yes	Yes	Yes	Yes	TBD	TBD
Target row refresh mode	TRR	Yes	Yes	Yes	Yes	TBD	TBD
Post package repair mode	PPR	Yes	Yes	Yes	Yes	TBD	TBD
Soft post package repair mode	sPPR	Yes	Yes	Yes	Yes	TBD	TBD

Table 137: Width Options

Function	Acronym	
Write leveling	WL	Yes
Temperature controlled refresh	TCR	Yes
Low-power auto self refresh	LPASR	Yes
Fine granularity refresh	FGR	Yes
Multipurpose register	MR	Yes

TABLE 137: WIDTH OPTIONS (CONTINUED)

Function	Acronym	
Data mask	DM	No
Data bus inversion	DBI	No
TDQS	–	No
ZQ calibration	ZQ CAL	Yes
V_{REFDQ} calibration	–	Yes
Per-DRAM addressability	Per DRAM	Yes
Mode regsiter readout	–	Yes
Command/Address latency	CAL	Yes
Write CRC	CRC	Yes
CA parity	–	Yes
Gear-down mode	–	Yes

Options Tables

TABLE 138: DIE REVISION OPTIONS

Function	Acronym	Rev. A
Write leveling	WL	Yes
Temperature controlled refresh	TCR	Yes
Low-power auto self refresh	LPASR	Yes
Fine granularity refresh	FGR	Yes
Multipurpose register	MR	Yes
Data mask	DM	Yes
Data bus inversion	DBI	Yes
TDQS	–	Yes
ZQ calibration	ZQ CAL	Yes
V_{REFDQ} calibration	–	Yes
Per-DRAM addressability	Per DRAM	Yes
Mode regsiter readout	–	Yes
Command/Address latency	CAL	Yes
Write CRC	CRC	Yes
CA parity	–	Yes
Gear-down mode	–	N/A
Programmable preamble	–	Pending
Maximum power-down mode	–	Yes
Connectivity test mode	CT	Yes
Additive latency	AL	Yes
Target row refresh mode	TRR	N/A
Post package repair mode	PPR	Pending

Revision History

Revision	By	Issue Date	Description Of Change
A	BV	5.27.2016	INITIATE
B	BV	9.31.2016	Refine pin-out for x32D, x72S, and x40D
C	BV	10.11.2016	Add Figures 2 and 3 - Block Diagrams; Correct Figure 5
D	DO	3.27.2017	Corrections Pages 19-25 - Ball Descriptions and Ball Locations
E	DO	6.14.2017	Added G suffix to part numbering Figure 1
F	DO	6.23.2017	Simplify Block diagrans at customer request

This data sheet contains initial descriptions of products still under development.